# SEL-287V
# SEL-187V

# VOLTAGE LEVEL RELAY
# VOLTAGE DIFFERENTIAL RELAY
# VOLTAGE CONTROLLER

# INSTRUCTION MANUAL

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# MANUAL CHANGE INFORMATION

The date code at the bottom of each page of this manual reflects the creation or revision date. Date codes are changed only on pages that have been revised and any following pages affected by the revisions (i.e., pagination). If significant revisions are made to a section, the date code on all pages of the section will be changed to reflect the revision date.

Each time revisions are made, both the main table of contents and the affected individual section table of contents are regenerated and the date code is changed to reflect the revision date.

Changes in this manual to date are summarized below (most recent revisions listed at top).

| Revision Date | Summary of Revisions |
|---|---|
| The ***Manual Change Information*** section has been created to begin a record of revisions to this manual. All changes will be recorded in this Summary of Revisions table. | |
| 20011116 | Made typographical correction in ***Section 1: Introduction***; added Terminal Connections specification, deleted Shipping Weight specification, and corrected specifications for Voltage Elements and Voltage Differential Elements in ***Section 2: Specifications***; added explanatory tables for the Externally/Fused Grounded-Wye Capacitor Bank Example in ***Section 5: Applications***; corrected targets and inputs and included updated relay dimension drawing in ***Section 6: Installation***; updated Factory Assistance paragraph in ***Section 7: Maintenance and Testing***. |
| 20010223 | ***Figure 2.1*** in ***Section 2: Specifications*** corrected replacing an OR gate with an AND gate. |
| 20000918 | Manual reissued; added application information to ***Section 5: Applications***. |
| 990312 | Instruction manual was updated to document the new setting range of the RINGS setting and the added functionality of preventing the relay from writing the new year to EEPROM at midnight New Year's Eve.<br>– Documented new RINGS setting range and associated new functionality under the SET command in the ***Section 3: Communications*** and ***Appendix C: SEL-287V-2 Relay Information***.<br>– Updated Settings Sheets in ***Section 5: Applications*** and ***Appendix C: SEL-287V-2 Relay Information***.<br>– Updated ***Appendix A: Firmware Versions*** with the revision numbers that include these modifications. |

| Revision Date | Summary of Revisions |
|---|---|
| 970820 | Instruction manual was changed to include material on new SEL-287V-2 version with special two-zone differential logic. Manual material on SEL-287V/287V-1 versions was updated/corrected in some cases.<br><br>Manual changes:<br><br>(1) Added brief description of new version in ***Introduction***.<br><br>(2) Noted items specific to 287V/287V-1 versions and referred to corresponding 287V-2 items in Appendix C.<br><br>(3) Added new Appendix C to include all specific information on SEL-287V-2 version.<br><br>(4) Updated drawing in Figure 2.3 and related logic expressions in ***Intermediate Logic***, ***Differential Overvoltage Conditions***, both of which apply to the SEL-287V/287V-1 versions. |

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# SECTION 1: INTRODUCTION

## GETTING STARTED

This instruction manual applies to the SEL-187V and SEL-287V family of relays. The SEL-287V Relay and the SEL-187V Relay have identical protection features, but use different hardware designs. See ***Appendix C: SEL-187V Relay Information*** for SEL-187V Relay details.

If you are unfamiliar with these relays, we suggest that you read this introduction, then perform the ***Initial Checkout*** procedure in ***Section 7: Maintenance and Testing***. For a more detailed understanding of the relay, we suggest that you read the following sections in the outlined order:

***Section 2: Specifications*** for a detailed description of the logic and how it works with logic inputs, the Relay Word, and relay outputs.

***Section 5: Applications*** for a description of capacitor banks, an application outline that guides settings selection, and Settings Sheets.

***Section 3: Communications*** for a description of the commands used to set the relay for protection, set the relay for control, obtain target information, obtain metering information, etc.

***Section 4: Event Reporting*** for a description of event report generation, summary event reports, long event reports, and their interpretation.

## OVERVIEW

The SEL-287V Relay provides voltage level relay, voltage differential relay, and voltage controller functionality intended to control and protect grounded-wye shunt capacitor banks.

The relay includes event reporting, local and remote setting via two EIA-232 ports, metering, automatic self-testing, and programmable logic masks.

Programmable logic and numerous voltage elements make the relay suitable for many other voltage control and monitoring purposes.

The SEL-287V Relay accepts voltage inputs from two separate three-phase, four-wire sources of potential, referred to as Source X and Source Y.

For each Source X and Y, the relay provides the following:

- Three single-phase overvoltage elements
- Three single-phase undervoltage elements
- One definite-time overvoltage element that responds to maximum phase voltage
- One three-phase overvoltage element intended for voltage control
- One three-phase undervoltage element intended for voltage control
- Voltage control instability detection logic
- Logic inputs to supervise the voltage control scheme
- Automatic scheme which selects preferred source for voltage control
- Four voltage control timers
- Loss-of-potential logic with timer

The SEL-287V Relay features magnitude-voltage-differential protection:

- Three differential elements per phase
  (six per phase in SEL-287V-2 Relay—alarm, trip, high-set trip; dV ≤ 0 and dV > 0)
- Separate thresholds for each element
- Adjustable pickup/dropout timers
- Separate ratio adjustment constants for each element and phase
- Loss-of-potential supervision with adjustable timers

General features of the SEL-287V Relay include:

- Eleven-cycle event report
- Twelve latest events stored in history buffer
- Programmable Logic Masks
- Two EIA-232 serial communications ports for setting and reporting
- Metering of all six inputs and the magnitude differences for each phase
- Full automatic self-testing to enhance reliability and availability

## MODEL OPTIONS

### SEL-187V Relay

This manual is written for the SEL-287V Relay. For SEL-187V Relays, substitute SEL-187V Relay for each reference to the SEL-287V Relay. See ***Appendix C: SEL-187V Relay Information*** for more details on the SEL-187V Relay.

### SEL-287V Relay

The preceding Overview outlines all the features contained in the basic SEL-287V Relay.

### SEL-287V-1 Relay

The SEL-287V-1 Relay has modified elements to provide faster pickup and dropout response. This change slightly reduces the element accuracy. Otherwise, this relay is functionally identical to the SEL-287V Relay design. The SEL-287V-1 Relay voltage and differential element accuracy is ±0.60 V at 25°C.

### SEL-287V-2 Relay

The SEL-287V-2 Relay differs from the standard SEL-287V Relay in the 87 voltage differential element logic, used for grounded capacitor bank protection. Separately adjustable voltage threshold settings are added for detection of unbalances above and below the tap point for alarm and trip purposes. The sign of the dVA, dVB, and dVC quantities is used to decide which threshold to apply. Independent A-phase, B-phase, and C-phase alarm thresholds have been eliminated.

In the standard SEL-287V Relay, for example, the A-phase difference voltage is calculated as $|dVA| = ||VAX| - KA \cdot |VAY||$, and only this magnitude of dVA is used in the comparison logic. In the SEL-287V-2 Relay, the formula is $dVA = |VAX| - KA \cdot |VAY|$, with the sign of dVA retained. If the value of dVA is greater than zero (positive sign), one set of thresholds is used for

the alarm, trip, and high-set trip functions. If dVA is less than zero (negative sign), another set of thresholds is used. The case dVA = 0 is considered a "negative" value. For detection of a blown fuse or fuses in a series group, a positive dVA occurs if the fuse blowing is above the tap, and a negative dVA occurs for fuse blowing below the tap. If the high-set trip unit is applied for detection and high-speed tripping when a series group flashover occurs, a positive dVA represents a flashover below the tap and a negative dVA represents a flashover above the tap, just the opposite of the signs for fuse blowings.

### Phase Rotation

This manual is written for standard ABC phase rotation applications. If you order your SEL relay with the ACB phase option, note references in the instruction manual to voltage and current phase angle accordingly. The firmware identification number (FID) may be used to verify whether your relay was ordered with ABC ("B") or ACB ("C") rotation.

All voltage inputs are connected to the SEL relay rear panel as shown in this instruction manual.

### System Frequency

This manual is written for relays operating at a nominal system frequency of 60 Hz. For relays that specify a nominal frequency of 50 Hz, substitute 50 Hz for each reference to 60 Hz. Replace references to a sampling time of 1/240 second with a time of 1/200 second.

## APPLICATION IDEAS

### Control and Protect Grounded-Wye Shunt Capacitor Banks

The SEL-287V Relay has instantaneous and definite-time overvoltage elements in addition to voltage-magnitude-differential elements. This combination of elements provides complete voltage-based protection for grounded-wye shunt capacitor banks.

The relay voltage differential elements are sensitive, stable, and precise. In most applications the relay can alarm for a single capacitor fuse operation. The KSET command automatically nulls the voltage differences. Mask-programmable event report triggering tailors relay event report generation to your specific requirements.

### Control Two Devices With One Relay

Two separate voltage control schemes perform voltage-based control of two devices, such as a capacitor bank and a reactor bank.

Independently settable voltage control timers help you coordinate voltage control with other system conditions.

The relay loss-of-potential (LOP) logic prevents voltage control operations in the event of blown bus potential transformer fuses.

## Control One Device With Two Independent Schemes

The two separate voltage control logic schemes can be applied to a single device. For example, you can use a long time delay for small variations in system voltage and a shorter time delay for large voltage excursions.

The two schemes are supervised by optoisolator contact inputs. Enable and disable the schemes by asserting the inputs remotely via SCADA or locally via control switch. You can operate both schemes together or each scheme individually. Thus, you can make your voltage control scheme adapt to system configuration and operating conditions.

## Three-Phase Undervoltage Load Shedding

The SEL-287V Relay can be used to detect three-phase undervoltage conditions and trip off load (after a settable time delay).

A latching bit in the Relay Word provides a remote (SCADA) or local alarm when the scheme operates. The latch bit can also be used with internal logic to restore load automatically when system voltage conditions return to normal.

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# SECTION 2: SPECIFICATIONS

## GENERAL SPECIFICATIONS

**Terminal Connections**

Rear Screw-Terminal Tightening Torque
Minimum: 8 in-lb (0.8 Nm)
Maximum: 12 in-lb (1.4 Nm)
Terminals or stranded copper wire. Ring terminals are recommended. Minimum temperature rating of 105°C.

**AC Input Voltage**

0–150 Vac rms line-to-neutral, 4-wire wye connection

**Output Contact Current Ratings**

30 A make per IEEE C37.90 para 6.7.2
6 A carry continuously
MOV protection provided

**Optoisolated Input Ratings**

The following optoisolated inputs draw 4 mA when nominal control voltage is applied:

| | |
|---|---|
| 24 Vdc: | 15 – 30 Vdc |
| 48 Vdc: | 30 – 60 Vdc |
| 250 Vdc: | 150 –300 Vdc |

Fixed "Level-Sensitive" inputs are provided on relays with 125 Vdc optoisolated inputs. The 125 Vdc optoisolated inputs each draw 6 mA when nominal control voltage is applied.

125 Vdc: on for 100 – 150 Vdc; off below 75 Vdc

**Time Code Input**

Relay accepts demodulated IRIG-B time code

**Communications**

Two EIA-232 serial communications ports

**Power Supply**

| | |
|---|---|
| 24/48 Volt: | 20 – 60 Vdc; < 15 watts |
| 125/250 Volt: | 85 – 350 Vdc or 85 – 264 Vac; < 15 watts |

**Dimensions**

3.5" x 19" x 9" (8.89 cm x 48.2 cm x 22.86 cm) (H x W x D)

**Mounting**

Mounts in standard EIA 19" (48.3 cm) relay rack or panel cutout. Available in horizontal and vertical mounting configurations.

**Dielectric Strength**

Routine tested
V inputs: 2500 Vac for 10 seconds
Other: 3000 Vdc for 10 seconds (excludes EIA-232 ports)

**Operating Temperature**

–40° to +158° F (–40° to +70° C)

**Environmental Test**

IEC 68-2-30 Temperature/Humidity Cycle Test
Six-day (type tested)

**Interference Tests**

IEEE C37.90 SWC Test (type tested)
IEC 255-6 Interference Test (type tested)

**Impulse Tests**

IEC 255-5 0.5 Joule, 5000 Volt Test (type tested)

**RFI Tests**

Type-tested in field from a ¼-wave antenna driven by 20 watts at 150 MHz and 450 MHz, randomly keyed on and off at a distance of 1 meter from relay.

**Electrostatic Discharge Test**

IEC 801-2 (type tested)

**Unit Weight**

12 pounds (5.5 kg)

## RELAY VOLTAGE ELEMENTS

| | | |
|---|---|---|
| **Voltage Control Elements** | 59P1, 59P2, 27P1, 27P2. These elements use the magnitude-average voltage of Source X or Y, depending on the Voltage Scheme Selection setting (VSS). | |
| **Phase Over-Voltage Elements** | X59A, X59B, X59C, Y59A, Y59B, Y59C | |
| **Phase Under-Voltage Elements** | X27A, X27B, X27C, Y27A, Y27B, Y27C | |
| **Definite-Time Over-Voltage Elements** | X59T and Y59T with individual settings for pickup and time delay. X59T operates from the highest magnitude of VAX, VBX, or VCX. Y59T operates from the highest magnitude of VAY, VBY, or VCY. | |
| **Pickup Range** | 0.00–150.00 V | |
| **Pickup Accuracy** | SEL-287V-0, -2 Relays: | ± 0.3 V @ 70 V, 25ºC |
| | SEL-287V-1 Relay: | ± 0.6 V @ 70 V, 25ºC |
| | Temperature Drift: | +6 mV/ºC deviation from 25ºC, 70 V or 79.5 ppm/ºC deviation from 25ºC, 70 V, typical |
| **Time-Delay Range** | 0–64000 cycles, one-cycle steps unless otherwise noted | |
| **Time Delay Accuracy** | ±0.1% ±0.25 cycle | |

## RELAY VOLTAGE DIFFERENTIAL ELEMENTS

| | | |
|---|---|---|
| | These elements test the difference between the magnitudes of like-phase voltages taken from Sources X and Y. | |
| **Elements** | SEL-287V-0, -1 Relays: | 87H, 87AT, 87BT, 87CT, 87AA, 87BA, 87CA |
| | SEL-287V-2 Relay: | 87H, 87T, 87A1, 87A2, 87AA, 87BA, 87CA |
| | In the SEL-287V-2 Relay, the sign of the voltage difference determines one of two thresholds. There are no per-phase alarm threshold settings 87AA, 87BA, and 87CA, as in the SEL-287V-0, -1 Relays. | |
| **Pickup Range** | 0.00–150.00 V | |
| **Calculation Resolution** | 0.03 V | |
| **Pickup Accuracy** | SEL-287V-0, -2 Relays: | ± 0.63 V @ 70 V, 25ºC without KSET adjustment<br>± 0.15 V @ 70 V, 25ºC with KSET adjustment<br>As a result, the minimum setting should be > 0.15 V @ 70 V, 25ºC and higher when the relay is exposed to higher voltages or temperature. |
| | SEL-287V-1 Relay: | ±1.23 V @ 70 V, 25ºC without KSET adjustment<br>± 0.30 V @ 70 V, 25ºC with KSET adjustment<br>As a result, minimum setting should be > 0.30 V |
| | Temperature Drift: | +6 mV/ºC deviation from 25ºC, 70 V or 79.5 ppm/ºC deviation from 25ºC, 70 V, typical |

**Time Delay Range** 0–64000 cycles, one-cycle steps unless otherwise noted

**Time Delay Accuracy** ±0.1% ±0.25 cycle

## LOGIC INPUTS

Six logic inputs control the relay functions. Assert a logic input by applying control voltage to the corresponding rear-panel contact input terminals.

**Table 2.1: Logic Input Functions**

| Input | Description | Function |
|---|---|---|
| RE1 | Raise Enable 1 | Enable Scheme 1 Raise Voltage Function |
| LE1 | Lower Enable 1 | Enable Scheme 1 Lower Voltage Function |
| RE2 | Raise Enable 2 | Enable Scheme 2 Raise Voltage Function |
| LE2 | Lower Enable 2 | Enable Scheme 2 Lower Voltage Function |
| ET1 | External Trigger 1 | External Event Report Trigger 1 / Reset LTCH |
| ET2 | External Trigger 2 | External Event Report Trigger 2 / Set LTCH |

## RELAY OUTPUTS

The SEL-287V Relay has seven outputs. All outputs except the ALARM output are programmed with the LOGIC command. All can be tested with the PULSE n command.

All relay contacts are rated for circuit breaker tripping duty. You may specify form "a" or "b" contacts for any of the programmable outputs or the ALARM contacts when you order the relay. The TRIP output contacts must be form "a."

### TRIP Output

This output closes for any number of conditions selected by the user. The TRIP output never closes for less than the TRIP duration timer interval. After this interval, it opens when the tripping condition vanishes.

### Programmable Outputs (A1, A2, A3, A4, A5)

These five outputs may be assigned to operate for any number of user-selected conditions.

### ALARM Output

The ALARM output closes for the following conditions:

- Three unsuccessful Level 1 access attempts: one-second pulse
- Any Level 2 access attempt: one-second pulse

Self-test failures: permanent contact closure or one-second pulse depending on which self-test fails (see STATUS command).

The ALARM output also closes momentarily when settings and passwords are changed, the KSET command is executed, or a date is entered, if the year stored in EEPROM differs from the year entered (see DATE command).

The standard relay has the ALARM contacts configured as form "b". In this case it is held open during normal relay operation; it closes if control power is lost or any other alarm condition occurs.

## RELAY WORD

The Relay Word consists of six eight-bit rows containing relay elements, timer outputs, and logic outputs. Each bit in the Relay Word is either a logical 1 or logical 0:

- 1 indicates that the element is picked up or logic condition is true
- 0 indicates that the element is dropped out or logic condition is false

The Logic Description defines the logic conditions in the Relay Word.

The relay updates the Relay Word each quarter-cycle.

**Table 2.2: SEL-287V, SEL-287V-1 Relay Word**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Row 1 | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D |
| Row 2 | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 |
| Row 3 | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 |
| Row 4 | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 |
| Row 5 | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A |
| Row 6 | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD |

**Table 2.3: SEL-287V-2 Relay Word**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Row 1 | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D |
| Row 2 | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 |
| Row 3 | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 |
| Row 4 | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 |
| Row 5 | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A |
| Row 6 | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D |

The Relay Word Bit Summary Table explains each bit in the Relay Word.

**Table 2.4: Relay Word Bit Summary Table**

| Row | Bit | Definition |
|---|---|---|
| 1 | X59A | Source X A-Phase Overvoltage |
| | X59B | Source X B-Phase Overvoltage |
| | X59C | Source X C-Phase Overvoltage |
| | 3Y59 | Source Y Three-Phase Overvoltage |
| | Y59A | Source Y A-Phase Overvoltage |
| | Y59B | Source Y B-Phase Overvoltage |
| | Y59C | Source Y C-Phase Overvoltage |
| | 3Y59D | TDDO Source Y Three-Phase Overvoltage |
| 2 | X27A | Source X A-Phase Undervoltage |
| | X27B | Source X B-Phase Undervoltage |
| | X27C | Source X C-Phase Undervoltage |
| | LTCH | Latching Bit Set by Energizing ET2 Input |
| | Y27A | Source Y A-Phase Undervoltage |
| | Y27B | Source Y B-Phase Undervoltage |
| | Y27C | Source Y C-Phase Undervoltage |
| | 3Y27 | Source Y Three-Phase Undervoltage |
| 3 | X59P | Source X Definite-Time Overvoltage Pickup |
| | X59T | Source X Definite-Time Overvoltage Trip |
| | Y59P | Source Y Definite-Time Overvoltage Pickup |
| | Y59T | Source Y Definite-Time Overvoltage Trip |
| | 59P1 | Magnitude-Average Overvoltage, Scheme 1 |
| | 27P1 | Magnitude-Average Undervoltage, Scheme 1 |
| | 59P2 | Magnitude-Average Overvoltage, Scheme 2 |
| | 27P2 | Magnitude-Average Undervoltage, Scheme 2 |
| 4 | VH1 | Voltage Control Scheme 1, Voltage High State |
| | VL1 | Voltage Control Scheme 1, Voltage Low State |
| | VH2 | Voltage Control Scheme 2, Voltage High State |
| | VL2 | Voltage Control Scheme 2, Voltage Low State |
| | VHD1 | Scheme 1, Time-Delayed Voltage High |
| | VLD1 | Scheme 1, Time-Delayed Voltage High |
| | VHD2 | Scheme 2, Time-Delayed Voltage High |
| | VLD2 | Scheme 2, Time-Delayed Voltage Low |

| Row | Bit | Definition |
|---|---|---|
| 5 | 87H | High-Set Instantaneous Differential Overvoltage Trip |
| | 87HD | High-Set Time-Delayed Differential Overvoltage Trip |
| | LOP | Instantaneous Loss-of-Potential, Either Source |
| | LOPD | Time-Delayed Dropout Loss-of-Potential, Either Source |
| | VCI1 | Scheme 1 Voltage Control Instability Detected |
| | VCI2 | Scheme 2 Voltage Control Instability Detected |
| | 87T | Instantaneous Differential Overvoltage Trip |
| | 87A | Instantaneous Differential Overvoltage Alarm |
| 6 | 87AT | A-Phase Differential Overvoltage Trip (SEL-287V, SEL-287V-1) |
| | 87A1 | Differential Overvoltage Alarm, Above Tap Point (SEL-287V-2) |
| | 87AA | A-Phase Differential Overvoltage Alarm |
| | 87BT | B-Phase Differential Overvoltage Trip (SEL-287V, SEL-287V-1) |
| | 87A2 | Differential Overvoltage Alarm, Below Tap Point (SEL-287V-2) |
| | 87BA | B-Phase Differential Overvoltage Alarm |
| | 87CT | C-Phase Differential Overvoltage Trip (SEL-287V, SEL-287V-1) |
| | 87A1D | Time-Delayed Diff. Overvoltage Alarm, Above Tap Point (SEL-287V-2) |
| | 87CA | C-Phase Differential Overvoltage Alarm |
| | 87TD | Time-Delayed Differential Overvoltage Trip |
| | 87AD | Time-Delayed Differential Overvoltage Alarm (SEL-287V, SEL-287V-1) |
| | 87A2D | Time-Delayed Diff. Overvoltage Alarm, Below Tap Point (SEL-287V-2) |

## PROGRAMMABLE LOGIC MASKS

The relay uses programmable logic masks to control tripping, programmable output contacts, and event report generation. Logic masks are saved in nonvolatile memory with the other settings. They are set with the LOGIC command and retained through losses of control power.

Programmable logic masks and their functions appear in Table 2.5.

**Table 2.5: SEL-287V Relay Programmable Logic Masks**

| Mask | Function |
|---|---|
| MT | Controls TRIP output contacts |
| MA1 | Controls A1 output contact |
| MA2 | Controls A2 output contact |
| MA3 | Controls A3 output contact |
| MA4 | Controls A4 output contact |
| MA5 | Controls A5 output contact |
| MER | Triggers Event Report Generation |

## OUTPUT LOGIC

Six of the seven outputs are programmable with masks (MT, MA1, MA2, MA3, MA4, MA5) that select Relay Word bits to control outputs.

The equations for the outputs follow:

TRIP = R * MT (where R is the Relay Word array)

Close TRIP contact = TRIP
Open TRIP contact = NOT(TRIP) * NOT(Minimum Trip Duration timer (TDUR))

A1 = R * MA1
A2 = R * MA2
A3 = R * MA3
A4 = R * MA4
A5 = R * MA5

"*" indicates the bitwise "AND" operator, which "ANDs" each Relay Word bit with the mask bit in the same position in the 6x8 mask array to determine contact operation.

All output relays are rated for tripping duty. The TRIP output relay has two "a" type contacts. Each of the other six relays has a single contact.

## RELAY TARGETS

The relay normally displays the targets identified on the front panel. Under normal operating conditions, the enable (EN) target lamp is lit. If the relay trips, it illuminates the LED corresponding to the element asserted at the time of trip. The target LEDs latch. The target LEDs that illuminated during the last trip remain lit until one of the following occurs:

- Next trip occurs
- Operator presses front-panel TARGET RESET button
- Operator executes TARGET R command

When a new trip occurs, the targets clear and the LEDs display the most recent tripping target.

When you press the TARGET RESET button, all eight indicators illuminate for a one-second lamp test. The relay targets clear and the Enable light (EN) illuminates to indicate that the relay is operational.

Use the TARGET command and display to examine the state of the relay inputs, outputs, and Relay Word elements. For more details, see ***Command Descriptions*** in ***Section 3: Communications***.

## SERIAL INTERFACES

Connectors labelled PORT 1 and PORT 2 are EIA-232 serial data interfaces. Generally, PORT 1 is used for remote communications via a modem, while PORT 2 is used for local communications via a terminal or SEL-PRTU protective relay terminal unit.

The baud rate of each port is set by jumpers near the front of the main board. You can access these jumpers by removing either the top cover or front panel. Available baud rates are 300, 600, 1200, 2400, 4800, and 9600.

The serial data format is:

Eight data bits
Two stop bits (-E2 model) or one stop bit (-E1 model)
No parity

You will receive a relay with two stop bits (-E2 model) unless you specifically request one stop bit (-E1 model). To determine whether your relay has one or two stop bits, look at the last two characters of the relay firmware identification number (FID). Use the EVENT command (see ***Section 4: Event Reporting***) to obtain an event report that includes the firmware identification number.

The serial communications protocol appears in ***Section 3: Communications***.

The SEL-287V Relay includes front- and rear-panel connectors for PORT 2. When a communication device is connected to the front-panel port, the relay ignores input from the rear-panel port. When the front-panel communications cable is removed, the relay resumes normal communications with the device connected to the rear-panel port.

## IRIG-B INPUT DESCRIPTION

The port labelled J201/AUX INPUT receives demodulated IRIG-B time-code input. The IRIG-B input circuit is a 56-ohm resistor in series with an optocoupler input diode. The input diode has a forward drop of about 1.5 V. Driver circuits should put approximately 10 mA through the diode when “on.”

The IRIG-B serial data format consists of a one-second frame containing 100 pulses and divided into fields. The relay decodes second, minute, hour, and day fields and sets the relay clock accordingly.

When IRIG-B data acquisition is activated either manually (with the IRIG command) or automatically, the relay reads two consecutive frames. It updates the older frame by one second and compares the frames. If they do not agree, the relay considers the data erroneous and discards it.

The relay reads the time code automatically about once every five minutes. The relay stops IRIG-B data acquisition 10 minutes before midnight on New Year's Eve so the relay clock may implement the year change without interference from the IRIG-B clock. Ten minutes after midnight, the relay restarts IRIG-B data acquisition.

## SIGNAL PROCESSING

The relay low-pass filters all six voltage channels and samples the channels four times per power system cycle. The microprocessor digitally filters each voltage channel using the CAL digital filter explained below. The relay stores the digital filter output for event reporting and magnitude calculations.

The microprocessor uses the digital filter output to determine the magnitude of each voltage. Magnitudes and differentials are smoothed over one cycle by an averaging function. Relay elements use the filtered and smoothed voltage magnitudes.

The relay uses a simple, effective CAL digital filter with the properties of a double differentiator smoother. Let the latest four samples of one analog channel be X1, X2, X3, and X4. Then the filter is defined:

$$P = X1 – X2 – X3 + X4.$$

This filter eliminates dc offsets. When all samples are set to the same value, the filter output is zero. The filter also eliminates ramps, which you may verify by setting the samples equal to 1, 2, 3, 4. Again, the output is zero.

Every quarter-cycle, the relay computes a new value of x for each input. The current value of x combines with the previous value (renamed y) to form a Cartesian coordinate pair. This pair represents the input signal as a phasor (x, y). The relay processes these phasor representations of the input signals. They also appear with the relay output after an event. You can use the data to construct phasor diagrams of the voltages.

## LOGIC DESCRIPTION

### Overvoltage/Undervoltage Logic

Figure 2.1 shows the logic diagram for the over-/undervoltage elements. The relay compares magnitudes of the six input quantities against user-settable thresholds. The individual phase overvoltage outputs (e.g., X59A, X59B, X59C) provide instantaneous overvoltage protection.

Output 3Y59 indicates a three-phase overvoltage condition on the Source Y inputs. This output drives an instantaneous pickup/time-delay dropout timer to produce output 3Y59D.

Output X27L indicates an undervoltage condition on any one or more phases of the Source X inputs. This output drives an instantaneous pickup/time-delay dropout timer to produce output X27D.

Output 3Y27 indicates a three-phase undervoltage condition on the Source Y inputs. This output drives an instantaneous pickup/time-delay dropout timer to produce output 3Y27D.

Outputs X27D and 3Y27D control selection of voltage sources for the voltage control logic. When the undervoltage elements drop out, the relay declares the input voltages valid for voltage control. The X and Y dropout time delay, LOPD, allows input voltages to stabilize before they are used by the voltage control logic.

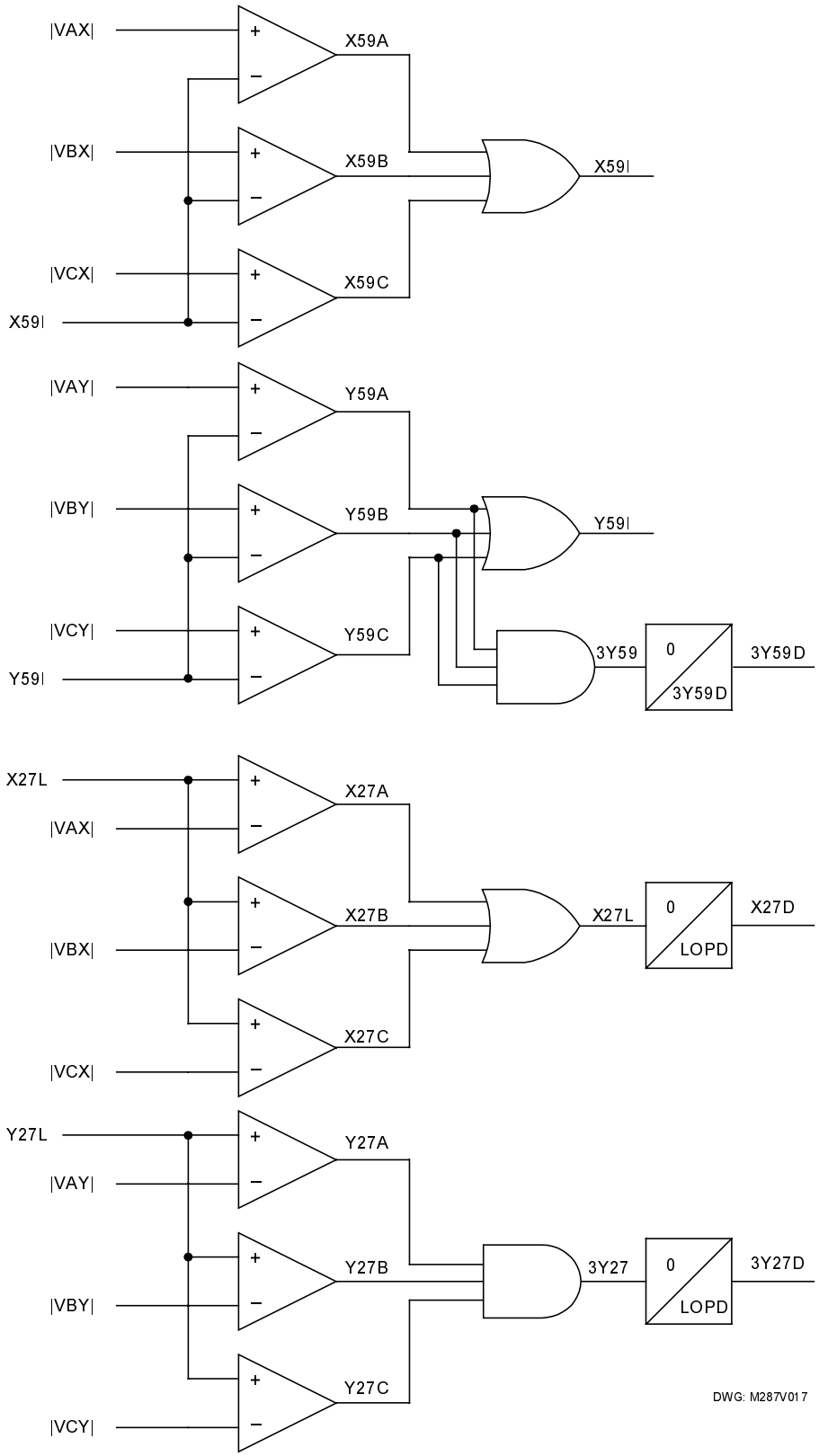


**Figure 2.1: Overvoltage Elements/Undervoltage Elements and Logic**

## Loss-of-Potential Logic

Outputs X27D and 3Y27D are OR-ed together to indicate a loss-of-potential (LOP) condition.

The output of the LOP time-delay dropout timer (LOPD) supervises the differential voltage elements to ensure that they operate only when both three-phase voltage input sources are valid.

The LOPD dropout delay allows voltage sources and elements to stabilize before the differential element outputs are considered valid. This delay permits successful capacitor bank energization.

Setting X27L or Y27L to zero ensures that the corresponding undervoltage elements do not pick up, even for a zero-voltage input condition. This is useful in disabling LOPD for either X or Y potentials.

## Definite-Time Overvoltage Logic

Figure 2.2 shows the logic for the definite-time overvoltage function.

For Source X, when the magnitude of VAX, VBX, or VCX rises above the X59PU setting, the X59P element asserts and starts the X59D timer. When the X59D timer expires, the X59T element asserts. Source Y protection operates similarly.

Instantaneous elements X59P and Y59P and time-delayed elements X59T and Y59T are available in the Relay Word for tripping, alarming, and event report triggering.

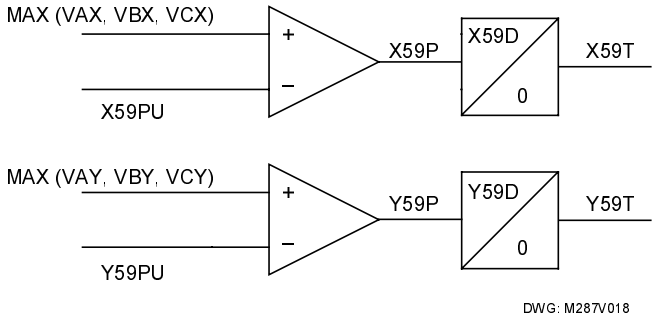


**Figure 2.2: Differential Logic (SEL-287V Relay)**

## Voltage Differential Logic (SEL-287V, SEL-287V-1 Relays)

Figure 2.3 shows the logic for the voltage differential protection scheme. The voltage differential elements provide protection for capacitor bank faults that produce a differential voltage at the bus and tap PT secondaries. The magnitude differences dVA, dVB, and dVC are calculated with independent ratio factors KA, KB, and KC. For example, dVA is calculated:

$$|dVA| = ||VAX| - KA|VAY||$$

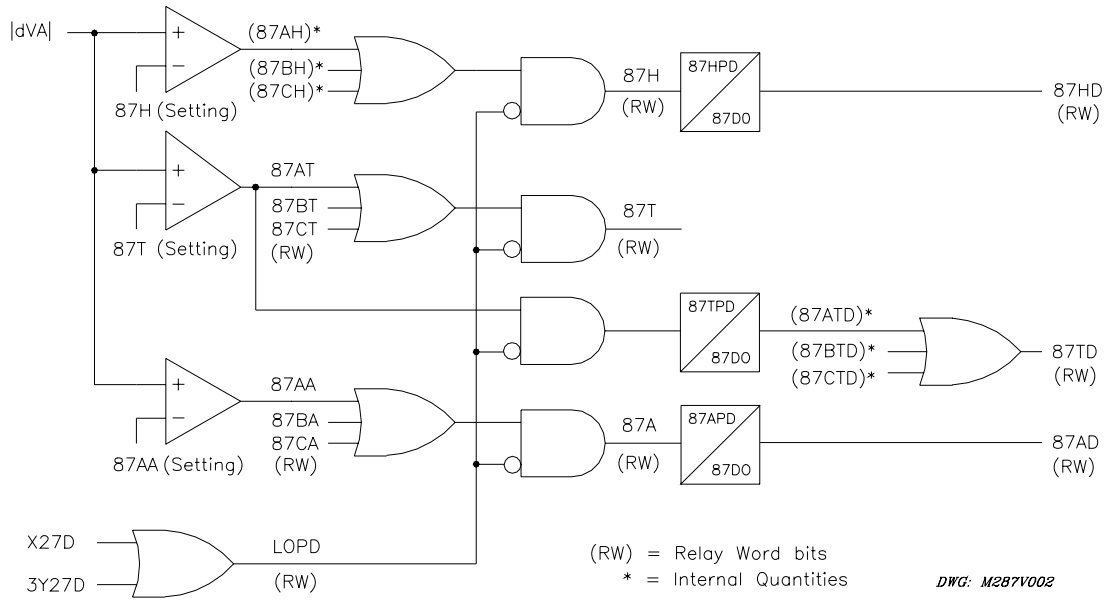


**Figure 2.3: Voltage Differential Protection Logic (Per-Phase)**

The relay tests the magnitude of each difference against user-settable trip and alarm thresholds on a per-phase basis. The three ratio adjustment constants (KA, KB, and KC) are independent, permitting differential relay unbalance nulling on a per-phase basis. There are three independent alarm threshold settings (87AA, 87BA, and 87CA), one per phase. The independent trip threshold settings (87T and 87H) are common for all phase elements.

The METER command output contains signed voltage differences so you can adjust ratio factors to null voltage differences under balanced conditions. You may also use the KSET command to calculate and adjust the ratio factors automatically (see ***KSET n***, ***Section 3: Communications***).

The LOPD (loss-of-potential, delayed dropout) signal supervises the 87A, 87T, and 87H differential elements.

A differential voltage condition on any phase starts the timer for that phase. If the condition continues through the duration of the timer, the timer output (87AD, 87TD, or 87HD) asserts. The output remains asserted for a settable dropout delay after the timer input deasserts.

The 87HD and 87TD logic provides independently operated, identically set time delays for each phase.

The Relay Word contains the single-phase outputs from differential elements 87T and 87A; three-phase LOPD-supervised signals 87A, 87T, and 87H; and the time-delayed outputs 87AD, 87TD, and 87HD.

## Voltage Differential Logic (SEL-287V-2 Relays)

Figure 2.4 shows the logic for the voltage differential protection scheme. The voltage differential elements provide protection for capacitor bank faults that produce a differential voltage at the bus and tap PT secondaries. The differences dVA, dVB, and dVC are calculated with independent ratio factors KA, KB, and KC as shown below:

$$dVA = |VAX| - KA|VAY|$$
$$dVB = |VBX| - KB|VBY|$$
$$dVC = |VCX| - KC|VCY|$$

The independent ratio factors (KA, KB, and KC) permit voltage unbalance nulling on a per-phase basis.

The relay uses the sign of dVA, in Figure 2.4, to determine which group of thresholds to use for comparison. If dVA > 0, it uses thresholds 87H1P, 87T1P, and 87A1P for high-set trip, trip, and alarm, respectively. If dVA ≤ 0, it uses 87H2P, 87T2P, and 87A2P. In either case, the relay compares the absolute value of dVA to the selected thresholds. Identical comparisons are performed for B- and C-phases using dVB and dVC.

Thresholds 87A1P and 87T1P are used for blown-fuse detection above the tap point. 87A1P is set to alarm for one fuse operation and 87T1P to trip for several fuse operations that could produce voltage overstress of the remaining cans in the series group. Thresholds 87A2P and 87T2P serve the same functions for fuse operations below the tap point.

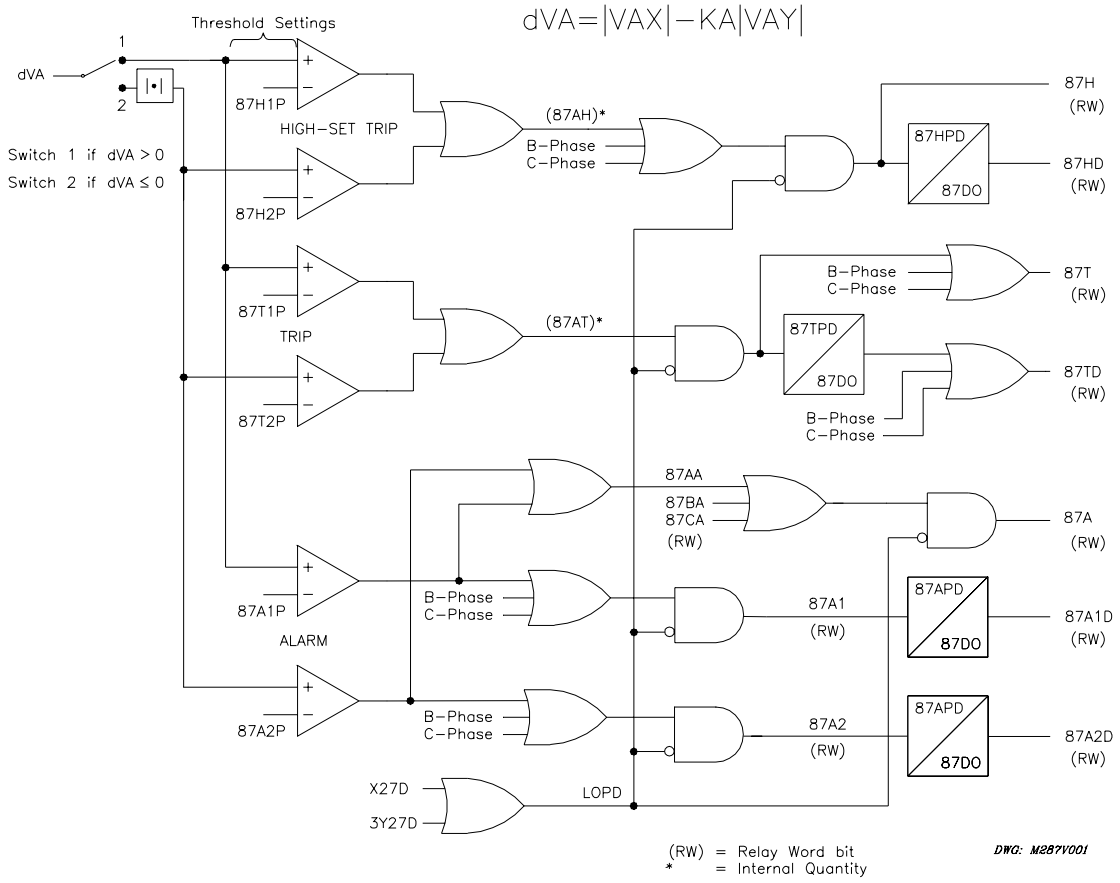


**Figure 2.4: Voltage Differential Protection Logic (Per Phase)**

Thresholds 87H1P (dVA > 0) and 87H2P (dVA ≤ 0) can be used either for high-speed tripping for excessive numbers of fuse operations (much like the regular alarm and trip functions) or for catastrophic events such as a complete series group flashover. If used for fuse detection, 87H1P applies above the tap and 87H2P below the tap. If used for group flashover, 87H1P applies below the tap and 87H2P above the tap.

The METER command output contains signed voltage differences, so you can adjust ratio factors to null voltage differences under balanced conditions. You may also use the KSET command to calculate and adjust the ratio factors automatically (see ***KSET n***, ***Section 3: Communications***).

The LOPD (loss-of-potential, delayed dropout) signal supervises the 87A, 87A1, 87A2, 87T, and 87H differential elements.

A differential voltage condition on any phase starts a timer. If the condition continues through the duration of the timer, the timer output 87A1D, 87A2D, 87TD, or 87HD asserts. For the 87TD output, there are three separate timers, one for each phase. The output remains asserted for a settable dropout delay after the timer input deasserts. The high-set pickup timer value is setting 87HPD; the trip timer pickup for each phase is 87TPD; and the above/below alarm timer pickups are both 87APD. A common dropout timer value 87DO applies to all six timers.

The Relay Word contains outputs from several points in the voltage differential logic. These points are indicated by (RW) below the bit names in Figure 2.4. Logic for the major differential element Relay Word bits is shown below in equation form.

### Differential Overvoltage Conditions

LOPD = X27D + 3Y27D

87H = NOT(LOPD) * (87AH + 87BH + 87CH)
87T = NOT(LOPD) * 87AT + NOT(LOPD) * 87BT + NOT(LOPD) * 87CT
87A = NOT(LOPD) * (87AA + 87BA + 87CA)

87HD = 87H * (87HPD pickup delay, 87DO dropout delay)
87TD = NOT(LOPD) * 87AT * (87TPD pickup delay, 87DO dropout delay)
+ NOT(LOPD) * 87BT * (87TPD pickup delay, 87DO dropout delay)
+ NOT(LOPD) * 87CT * (87TPD pickup delay, 87DO dropout delay)
87A1D = 87A1 * (87APD pickup delay, 87DO dropout delay)
87A2D = 87A2 * (87APD pickup delay, 87DO dropout delay)

## Voltage Control Logic

Figure 2.5 illustrates voltage control logic. The SEL-287V Relay includes two identical three-phase over-/undervoltage measurement and timing networks. One network is driven by V1; the other is driven by V2. V1 and V2 are either VX or VY, depending on the Voltage Selection Scheme chosen and voltage conditions. VX and VY are the magnitude averages of the three-phase source inputs:

VX = 1/3 (|VAX| + |VBX| + |VCX|)
VY = 1/3 (|VAY| + |VBY| + |VCY|)

Consider the scheme for voltage V1. The relay tests the three-phase magnitude average voltage V1 against two thresholds: 59P1 and 27P1. The under-/overvoltage conditions are supervised by signal VV1 (Valid Voltage condition 1, described later) and by external inputs LE1 (Lower Enable 1) or RE1 (Raise Enable 1).

The outputs VH1 and VL1 drive timers with independent time-delay pickup and dropout settings to produce outputs VHD1 and VLD1. Output VHD1 can drive a contact for lowering system voltage (e.g., tripping a capacitor bank or inserting a reactor bank) with the permission of external

input LE1. Output VLD1 is intended to drive a contact for raising system voltage (e.g., inserting a capacitor bank or tripping a reactor bank) with the permission of external input RE1.

The scheme for voltage V2 is identical to that for V1. The two schemes have independent settings and independent raise/lower enable inputs.

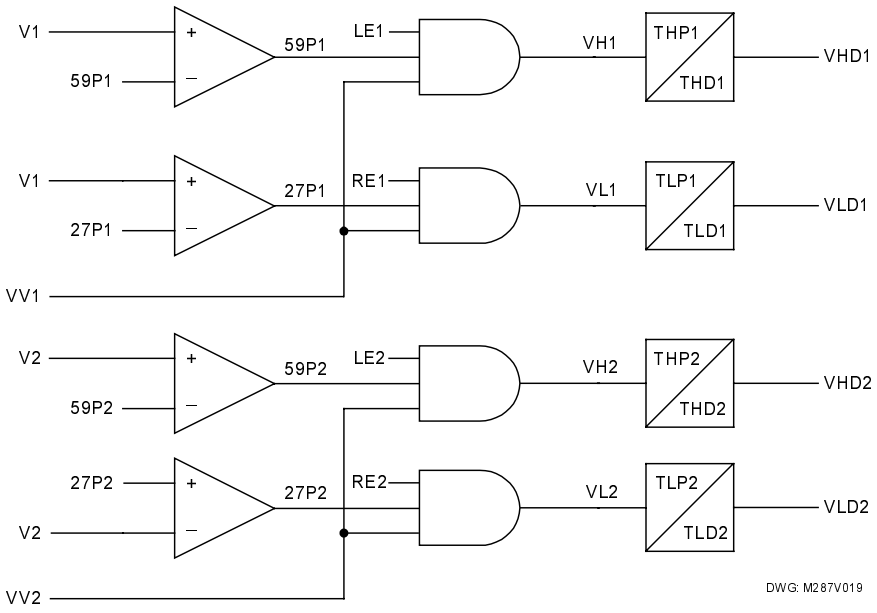


**Figure 2.5: Voltage Control Logic**

## Voltage Selection Scheme

Table 2.6 shows voltage selection settings for the voltage control schemes described above. Setting VSS (Voltage Selection Scheme) selects one of three ways the relay applies magnitude-average input voltages VX and/or VY to voltage control inputs V1 and V2.

VSS = I

If the two voltage control schemes (1 and 2) are to be independent, set VSS=I (independent). With this setting the relay applies VX to the V1 input and VY to the V2 input. This assignment does not depend on the voltage conditions. The valid voltage condition for scheme 1 is VV1 = not(X27D) + not(LOPE1). The voltage control logic requires either no loss-of-potential condition for Source X, or that loss-of-potential checking be disabled by setting LOPE1 = N. A similar logic applies to Scheme 2.

VSS = B

When setting VSS = B (relay selects the better source), the relay normally sets V1 = VX. If Source X is bad (X27D asserts) and Source Y is still good (3Y27D is deasserted), the relay sets V1 = VY, so voltage control Scheme 1 operates from Source Y.

Similarly, the relay normally sets V2 = VY. However, if Source Y is bad while Source X is good, V2 = VX.

When dissimilar nominal secondary voltages are input to Source X and Source Y, do not apply a setting VSS = B.

VSS = X

Under some conditions, you may wish to use Source X for both V1 and V2. To do so, set VSS = X. Then the relay sets V1 = V2 = VX for all conditions. The voltage valid condition is true when X27D is not asserted and depends on LOPE1 when X27D is asserted.

**Table 2.6: Voltage Selection for Voltage Control**

| Setting VSS | Voltage Source | Voltage Conditions | Voltage Control Inputs |
|---|---|---|---|
| VSS=I | X, Y | Independent | V1=VX<br>V2=VY<br>VV1=not(X27D)+not(LOPE1)<br>VV2=not(3Y27D)+not(LOPE2) |
| VSS=B | Better Source | not(X27D) * not(3Y27D) | V1=VX<br>V2=VY VV1=VV2=1 |
| | | not(X27D) * 3Y27D | V1=V2=VX VV1=VV2=1 |
| | | X27D * not(3Y27D) | V1=V2=VY VV1=VV2=1 |
| | | X27D * 3Y27D | V1=VX V2=VY<br>VV1=not(LOPE1)<br>VV2=not(LOPE2) |
| VSS=X | Source X Only | not(X27D) | V1=V2=VX<br>VV1=VV2=1 |
| | | X27D | V1=V2=VX<br>VV1=VV2=not(LOPE1) |

## Voltage Control Instability Logic

The two AND gate outputs in Figure 2.6 indicate voltage control instability. When a signal to decrease voltage (VH1) occurs before the increase-voltage dropout time (TLD1) expires, the relay asserts VCI1. When the relay asserts VCI1 or VCI2 bits, voltage control action probably is causing a voltage change greater than the amount between the raise and lower voltage settings.

Outputs VCI1 and VCI2 are in the Relay Word. They may be used to alarm or lock out voltage control via an external latching relay, or be included in the MT mask to trip and lock the bank out of service when instability conditions occur.

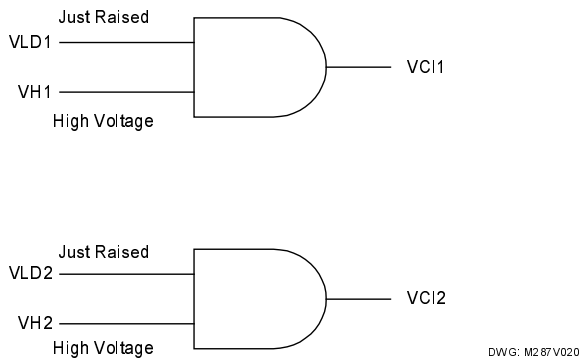


**Figure 2.6: Voltage Control Instability Logic**

## Latching Bit Logic

When relay setting LTCHE = Y, the External Trigger inputs are used to set and reset a latch bit, LTCH, in the Relay Word. Assert LTCH by energizing ET2; LTCH does not reset until ET1 is energized and ET2 is deenergized.

This feature can be used for SCADA alarm indication and enabling the voltage control logic for automatic load restoration.

Note that when LTCHE = Y, ET1 and ET2 do not trigger event records.

When LTCHE = N, assert ET1 and ET2 to trigger event reports. The LTCH bit does not operate when LTCHE = N.

## A1 Through A5 Output Contact Time-Delay Logic

Figure 2.7 illustrates the A1 through A5 output contact time-delay logic. Output from the A1 through A5 contacts can be delayed through A1PD, A2PD, A3PD, A4PD, and A5PD time-delay pickup timers. The A1 through A3 output contacts open as soon as the conditions set in the A1, A2, or A3 logic mask reset. The 87DO time-delay dropout timer holds the contact closed for a set time delay after the condition in the A4 or A5 mask resets.

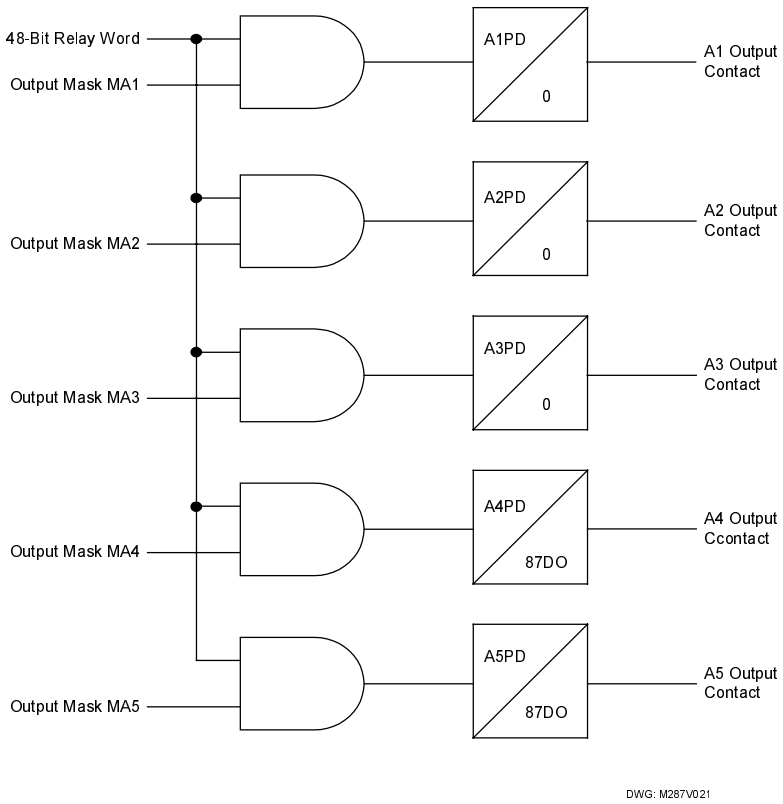


**Figure 2.7: A1 Through A5 Output Contact Time Delay Logic**

## INTERMEDIATE LOGIC

The logic equations shown below represent combinations of the relay elements and other conditions. In the following equations the "*" indicates a logical "AND," while the "+" indicates a logical "OR."

### Instantaneous Overvoltage Elements

X59I = X59A + X59B + X59C

Y59I = Y59A + Y59B + Y59C

3Y59 = Y59A * Y59B * Y59C

**Note:** X59I and Y59I are used for targeting purposes only.

### Time-Delayed Dropout Overvoltage Element

3Y59D = 3Y59 * (inst pickup, 3Y59D dropout delay)

### Definite-Time Overvoltage Elements

X59T = X59P * (X59D pickup delay)
Y59T = Y59P * (Y59D pickup delay)

## Instantaneous Undervoltage Elements

X27L = X27A + X27B + X27C
3Y27 = Y27A * Y27B * Y27C

## Time-Delayed Dropout Undervoltage Elements

X27D = X27L * (inst pickup, LOPD dropout delay)
3Y27D = 3Y27 * (inst pickup, LOPD dropout delay)

## Differential Overvoltage Conditions

**Note:** Relay Word elements displayed in bold type.

**LOPD** = X27D + 3Y27D

87AH = |dVA| > 87Hsetting
87BH = |dVB| > 87Hsetting
87CH = |dVC| > 87Hsetting

**87AT** = |dVA| > 87Tsetting
**87BT** = |dVB| > 87Tsetting
**87CT** = |dVC| > 87Tsetting

**87AA** = |dVA| > 87AAsetting
**87BA** = |dVB| > 87BAsetting
**87CA** = |dVC| > 87CAsetting

**87H** = NOT(**LOPD**) * (87AH + 87BH + 87CH)
**87T** = NOT(**LOPD**) * (**87AT** + **87BT** + **87CT**)
**87A** = NOT(**LOPD**) * (**87AA** + **87BA** + **87CA**)

87ATD = NOT(**LOPD**) * **87AT** * (87TPD pickup delay, 87DO dropout delay)
87BTD = NOT(**LOPD**) * **87BT** * (87TPD pickup delay, 87DO dropout delay)
87CTD = NOT(**LOPD**) * **87CT** * (87TPD pickup delay, 87DO dropout delay)

**87HD** = **87H** * (87HPD pickup delay, 87DO dropout delay)
**87TD** = 87ATD + 87BTD + 87CTD
**87AD** = **87A** * (87APD pickup delay, 87DO dropout delay)

## Voltage Control Logic

VH1= LE1 * 59P1 * VV1
VL1= RE1 * 27P1 * VV1

VH2= LE2 * 59P2 * VV2
VL2= RE2 * 27P2 * VV2

The states of VV1 and VV2 are determined from the VSS setting and the voltage conditions as shown in Table 2.6.

VHD1 = VH1 * (THP1 pickup delay, THD1 dropout delay)
VLD1 = VL1 * (TLP1 pickup delay, TLD1 dropout delay)

VHD2 = VH2 * (THP2 pickup delay, THD2 dropout delay)
VLD2 = VL2 * (TLP2 pickup delay, TLD2 dropout delay)

### Voltage Control Instability Logic

VCI1 = VLD1 * VH1
VCI2 = VLD2 * VH2

### Latching Bit Logic

Set LTCH = ET2
Reset LTCH = ET1 * NOT(ET2)

This logic is enabled when LTCHE = Y. When LTCHE = N, ET1 and ET2 act as external event triggers.

### A1 Through A5 Output Contact Time-Delay Logic

A1TD = A1 * (A1PD Pickup delay, instantaneous dropout delay)
A2TD = A2 * (A2PD Pickup delay, instantaneous dropout delay)
A3TD = A3 * (A3PD Pickup delay, instantaneous dropout delay)
A4TD = A4 * (A4PD pickup delay, 87DO dropout delay)
A5TD = A5 * (A5PD pickup delay, 87DO dropout delay)

## PROGRAMMABLE LOGIC MASK CONCEPT

Figure 2.8 illustrates the programmable logic mask concept by comparing it to the connections of discrete relay elements. At the top, the figure shows relay element contacts X, Y, and Z connected to a common reference, such as the positive pole of the battery. The ends of these contacts are connected to knife switches, and the other side of each switch connects to drive an auxiliary relay labelled A1. The knife switch positions select which relay elements can pick up the auxiliary relay. In the figure switches SX and SY are closed, so closure of contact X or contact Y causes A1 to pick up. This is expressed in Boolean terms next to the A1 output contact by the notation X + Y, where "+" indicates the logical "OR" operation.

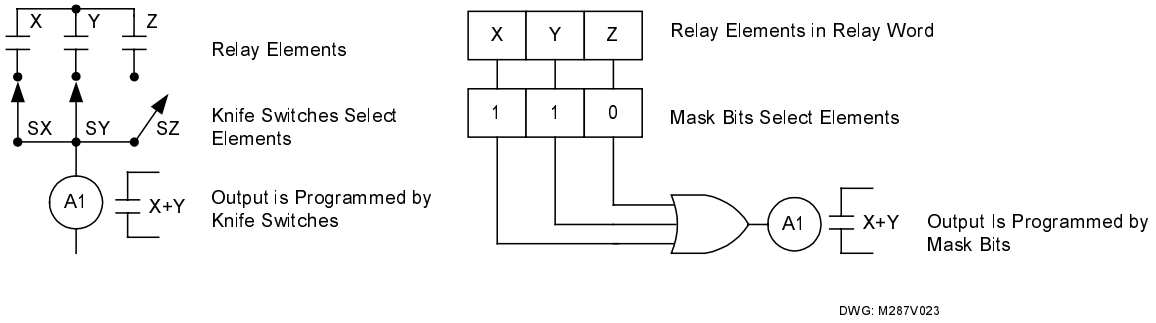


**Figure 2.8: Basic Concept of Programmable Logic Masks**

This logic scheme may be modified by setting switches SX, SY, and SZ to other positions. If an application requires combinations of contacts X, Y, and Z to control other auxiliary relays, diodes must be used in each contact path. These diodes ensure that the logic settings for this scheme do not affect other auxiliary relays.

In programmable mask logic the states of all relay elements are collected into a single group of binary digits called the Relay Word. Each bit reports the state of one relay element. A zero indicates that the element is not picked up; a one indicates that the element is picked up.

Figure 2.8 shows a three-bit Relay Word with elements X, Y, and Z. Each bit corresponds to one relay element contact in the contact-logic equivalent. The operator sets or clears bits in the mask for the A1 output rather than using switches to select which elements control the A1 output (see ***Section 3: Communications***, ***LOGIC n***). In the figure the operator selected the X and Y elements and deselected the Z element by setting the mask bits to (1, 1, 0). The computer ANDs each bit in the Relay Word with the corresponding bit set in the mask. Next, it ORs all three outputs together, forming the condition that drives the output relay A1. A convenient shorthand way of expressing this bitwise AND followed by an OR operation is:

A1 = R * MA1

where R is the Relay Word (X, Y, Z), MA1 is the mask (1, 1, 0), and "*" indicates the operation of bitwise ANDing followed by the OR operation.

While the mask elements are fixed, the Relay Word updates each quarter-cycle. In this example, if the X or Y element is set to (1) in the Relay Word, the A1 contact closes. The state of the A1 contact is independent of the Z element in the Relay Word because the corresponding Z element in the mask equals zero.

The relay has user-programmable logic masks that control tripping, programmable output contacts, and event report generation. The logic masks are saved in nonvolatile memory with the other settings and retained through losses of control power.

## EVENT REPORTING

The relay retains a data record for each of the 12 most recent events. The record includes input voltages, Relay Word elements, input contacts, and output contacts. The relay saves a report when any of the following occur:

- The relay trips
- User-selected Relay Word bits assert
- User executes the TRIGGER command
- ET1 or ET2 input is asserted (if LTCHE = N)

***Section 4: Event Reporting*** has further information regarding the generation, content, and analysis of event reports saved by the relay.

## METERING

The meter function shows the current value of ac voltage input magnitudes and phase differential voltage magnitudes (see ***Section 3: Communications***, ***METER n***). You can execute this command locally or remotely to check bus and bank conditions.

## SELF-TESTING

The relay runs a variety of self-tests. Some tests have warning and failure states; others only have failure states. The relay generates a status report after any self-test warning or failure.

The relay closes the ALARM contacts after any self-test fails. When the relay detects certain failures, it disables the breaker control functions and places the output relay driver port in an input mode. No outputs may be asserted when the relay is in this configuration. The relay runs all self-tests at least every five minutes.

### Offset

The relay measures the dc offset voltage of each analog input channel and compares the value against fixed limits. If an offset measurement is outside the fixed limits, the relay declares a warning or failure.

### Power Supply

The relay measures the internal power supply voltages and compares the values against fixed limits. If a voltage measurement is outside the limits, the relay declares a warning or failure.

**Table 2.7: Power Supply Self-Test Limits**

| Supply | Warning Thresholds | | Failure Thresholds | |
|---|---|---|---|---|
| +5 V | 5.3 V | 4.7 V | 5.4 V | 4.6 V |
| +15 V | 15.8 V | 14.2 V | 16.2 V | 13.8 V |
| –15 V | –15.8 V | –14.2 V | –16.2 V | –13.8 V |

### Random-Access Memory

The relay completely checks the random-access memory (RAM) every 35 seconds. If a byte cannot be written to or read from, the relay declares a RAM failure. There is no warning state for this test.

### Read-Only Memory

The relay checks the read-only memory (ROM) by computing a checksum. If the computed value does not agree with the stored value, the relay declares a ROM failure. There is no warning state for this test.

### Analog-to-Digital Converter

The relay verifies the A/D converter function by checking the A/D conversion time. The test fails if conversion time is excessive or a conversion starts and never finishes. There is no warning state for this test.

## Master Offset

The master offset (MOF) test checks the dc offset in the multiplexer/analog to digital converter circuit. The relay selects a grounded input to sample for dc offset.

## Settings

Every time you set the relay, it calculates a checksum for the settings. The checksum is stored in nonvolatile memory with the settings. The relay recalculates and compares the checksum at least every five minutes. If the checksums disagree, the setting test fails and the relay disables all protective and control functions.

Table 2.8 shows relay actions for any self-test condition: warning (W) or failure (F).

**Table 2.8: Self-Test Summary**

| Self-Test | Limits | Status Message | Protection Disabled | Control Disabled | Alarm Output |
|---|---|---|---|---|---|
| RAM | ---- | F | YES | YES | permanent closure |
| ROM | ---- | F | YES | YES | permanent closure |
| Settings | ---- | F | YES | YES | permanent closure |
| A/D | ---- | F | YES | no | permanent closure |
| +5 V | ±0.3 V<br>±0.4 V | W<br>F | no<br>YES | no<br>YES | no ALARM closure<br>permanent closure |
| ±15 V | ±0.8 V<br>±1.2 V | W<br>F | no<br>YES | no<br>no | no ALARM closure<br>permanent closure |
| Channel Offsets | ±50 mV<br>±75 mV | W<br>F | no<br>no | no<br>no | no ALARM closure<br>one-second pulse |
| Master Offset | ±50 mV<br>±75 mV | W<br>F | no<br>no | no<br>no | no ALARM closure<br>one-second pulse |

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# FIGURES

# SECTION 3: COMMUNICATIONS

## INTRODUCTION

The relay is set and operated via serial communications interfaces connected to a computer terminal and/or modem or the SEL-PRTU. Communication serves these purposes:

- Relay responds to commands spanning all functions, e.g., setting, metering, and control operations.
- Relay generates an event record for assertions of the TRIP output, either External Trigger input, and any element set in the programmable logic mask MER.
- Relay transmits messages in response to changes in system status, e.g., self-test warning.

Two password-protected access levels provide security against unauthorized access and setting changes.

It is impossible to disable any relaying or control functions via communications, unless a user enters erroneous or improper settings with the SET or LOGIC commands.

**Note:** In this manual, commands to type appear in bold/upper case: **OTTER**. Keys to press appear in bold/upper case/brackets: **<ENTER>**.

Relay output appears in the following format and font:

```
Example Settings                  Date: 6/1/92  Time: 01:01:01
```

## SERIAL PORT CONNECTIONS AND CONFIGURATIONS

The SEL-287V Relay is equipped with two EIA-232 serial communications ports. PORT 2 has 9-pin connectors on both the front and rear panels, designated PORT 2F and PORT 2R, respectively.

PORT 2R, located on the relay rear panel, typically is used with an SEL-DTA Display/ Transducer Adapter, or local printer. PORT 2F is always available for short-term local communications with a portable computer or printing terminal. Simply plug the device into the front-panel port. The relay automatically discontinues communications with PORT 2R and addresses PORT 2F. When testing or data retrieval is complete, unplug the temporary device from PORT 2F. The relay automatically resumes communication with the device connected to PORT 2R.

Serial communications PORT 1 and the Auxiliary Input for demodulated IRIG-B time-code input are located on the relay rear panel.

Communications port baud rate jumpers are located along the front edge of the circuit board. To select a baud rate for PORT 1 or PORT 2, remove the relay front panel. The jumpers are visible near the center of the relay drawout assembly, to the right of the target LEDs. Carefully move the jumpers using needle-nosed pliers. Available rates are 300, 600, 1200, 2400, 4800, and 9600 baud.

**CAUTION**

Do not select two baud rates for the same port, because this can damage the relay baud rate generator. The relay is shipped with PORT 1 set to 300 baud and PORT 2F/2R set to 2400 baud.

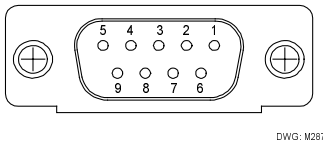
The serial data format is:

Eight data bits

Two stop bits (-E2 model) or one stop bit (-E1 model)

No parity bit

This format cannot be altered.




(female chassis connector, as viewed from outside panel)

**Figure 3.1: SEL-287V Relay Nine-Pin Connector Pin Number Convention**

Table 3.1 lists port pin assignments and signal definitions.

**Table 3.1: SEL-287V Relay Serial Port Connector Pin Assignments**

| Pin | PORT 1, PORT 2R | PORT 2F | Description |
|---|---|---|---|
| 1 | +5 Vdc | N/C | |
| 2 | RXD | RXD | Receive data input. |
| 3 | TXD | TXD | Transmit data output. |
| 4 | +12 Vdc | N/C | |
| 5 | GND | GND | |
| 6 | –12 Vdc | N/C | |
| 7 | RTS | RTS | The relay asserts this line under normal conditions. When its received-data buffer is full, the line is deasserted. It asserts again when the buffer has sufficient room to receive more data. Connected devices should monitor RTS (usually with their CTS input) and stop transmission whenever the line deasserts. If transmission continues, data may be lost. |
| 8 | CTS | CTS | The relay monitors CTS, and transmits characters only if CTS is asserted. |
| 9 | GND | GND | Ground for ground wires and shields. |

## COMMUNICATIONS PROTOCOL

The communications protocol consists of hardware and software features. Hardware protocol includes the control line functions described above. The following software protocol is designed for manual and automatic communications.

1. All commands received by the relay must be of the form:

   <command><CR> or <command><CRLF>

   Thus, a command transmitted to the relay should consist of the command followed by either a carriage return or a carriage return and line feed. You may truncate commands to the first three characters. Thus, **EVENT 1 <ENTER>** would become **EVE 1 <ENTER>**. Upper- and lower-case characters may be used without distinction, except in passwords.

   **Note:** The ENTER key on most keyboards is configured to send the ASCII character 13 (^M) for a carriage return. This manual instructs you to press the ENTER key after commands, which should send the proper ASCII code to the relay.

2. The relay transmits all messages in the following format:

   <STX> <MESSAGE LINE 1><CRLF>
   <MESSAGE LINE 2><CRLF>
   .
   .
   <LAST MESSAGE LINE><CRLF><PROMPT><ETX>

   Each message begins with the start-of-transmission character (ASCII 02) and ends with the end-of-transmission character (ASCII 03). Each line of the message ends with a carriage return and line feed.

3. The relay indicates the volume of data in its received-data buffer through an XON/XOFF protocol.

   The relay transmits XON (ASCII hex 11) and asserts the RTS output when the buffer drops below one-fourth full.

   The relay transmits XOFF (ASCII hex 13) when the buffer is over three-fourths full. The relay deasserts the RTS output when the buffer is approximately 95 percent full. Automatic transmission sources should monitor for the XOFF character so they do not overwrite the buffer. Transmission should terminate at the end of the message in progress when XOFF is received and may resume when the relay sends XON.

4. You can use an XON/XOFF procedure to control the relay during data transmission. When the relay receives XOFF during transmission, it pauses until it receives an XON character. If there is no message in progress when the relay receives XOFF, it blocks transmission of any message presented to its buffer. The relay accepts messages after it receives XON.

   The CAN character (ASCII hex 18) aborts a pending transmission. This is useful in terminating an unwanted transmission.

5. Control characters can be sent from most keyboards by using the following keystrokes:

| | | |
|---|---|---|
| XON: | **<CTRL>Q** | (hold down the Control key and press Q) |
| XOFF: | **<CTRL>S** | (hold down the Control key and press S) |
| CAN: | **<CTRL>X** | (hold down the Control key and press X) |

## COMMAND CHARACTERISTICS

The relay responds to commands sent to either serial communications interface. A two-level password system provides security against unauthorized access.

When the power is first turned on, the relay is in Access Level 0 and honors only the ACCESS command. It responds "Invalid command" or "Invalid access level" to any other entry.

You may enter Access Level 1 with the ACCESS command and first password. The Level 1 password is set to OTTER at the factory; change it with the PASSWORD command in Access Level 2. Most commands may be used in Access Level 1.

Critical commands such as SET operate only in Access Level 2. You may enter Access Level 2 with the 2ACCESS command and second password. The Level 2 password is set to TAIL at the factory; change it with the PASSWORD command.

### Startup

Immediately after power is applied, the relay transmits the following message to the port(s) designated automatic:

```
Example Settings                    Date: 6/1/92   Time: 01:01:01

SEL-187V

=
```

The ALARM relay should pull in.

The = sign represents the Access Level 0 prompt.

The relays are shipped with PORT 2 designated automatic; use the SET command if you want to change this designation (see SET command, AUTO setting). This allows you to select PORT 1, PORT 2, or both ports to transmit automatic responses from the relay.

To enter Level 1, type the following on a terminal connected to PORT 2:

```
=ACCESS <ENTER>
```

The response is:

```
Password: ? @@@@@@
```

Enter the Level 1 password **OTTER** and press **<ENTER>**. The response is:

```
Example Settings                 Date: 6/1/92    Time: 01:01:01

Level 1
=>
```

The Access Level 1 prompt is =>. Now you can execute any Level 1 command.

Use a similar procedure to enter Access Level 2:

Type **2ACCESS <ENTER>**. The relay pulses the ALARM relay contacts closed for approximately one second to indicate a Level 2 access attempt. Enter the password TAIL when prompted. After you enter the second password, the relay opens access to Level 2, as indicated by the following message and Level 2 prompt (**=>>**):

```
=>2ACCESS <ENTER>
Password:  @@@@@@


Example Settings                   Date: 6/1/92   Time: 01:01:01

Level 2
=>>
```

You can enter any command at this prompt.

### Command Format

Commands consist of three or more characters; only the first three characters of any command are required. You may use upper- or lower-case characters without distinction, except in passwords.

Separate arguments from the command by spaces, commas, semicolons, colons, or slashes.

You can enter commands any time after the terminal displays an appropriate prompt.

## COMMAND DESCRIPTIONS

### Access Level 0 Command

### ACCESS

ACCESS allows you to enter Access Level 1. The password is required unless you install jumper JMP103. The first password is set to OTTER at the factory; use the Level 2 command PASSWORD to change passwords.

The following display indicates successful access:

```
=ACCESS <ENTER>
Password:  @@@@@@


Example Settings                   Date: 6/1/92   Time: 14:03:57

Level 1
=>
```

The => prompt indicates Access Level 1.

If you enter wrong passwords during three consecutive attempts, the relay pulses the ALARM contacts closed for one second. This feature can alert personnel to an unauthorized access attempt if ALARM contacts are connected to a monitoring system.

## Access Level 1 Commands

### 2ACCESS

2ACCESS allows you to enter Access Level 2. The password is required unless you install jumper JMP103. The second password is set to TAIL at the factory; use the Level 2 command PASSWORD to change passwords.

The following display indicates successful access:

```
=>2ACCESS <ENTER>
Password:  @@@@@@


Example Settings                   Date: 6/1/92   Time: 14:12:01

Level 2
=>
```

You may use any command from the =>> prompt. The relay pulses the ALARM contacts closed for one second after any Level 2 access attempt, successful or otherwise (unless an alarm condition exists).

### DATE mm/dd/yy

DATE displays the date stored by the internal calendar/clock. To set the date, type **DATE mm/dd/yy <ENTER>**.

To set the date to June 20, 1992, enter:

```
=>DATE 6/20/92 <ENTER>
6/20/92

=>
```

The relay sets the date, pulses the ALARM relay closed as it stores the year in EEPROM (if year input differs from year stored), and displays the new date.

## EVENT n

EVENT displays an event report. Type **EVENT n <ENTER>** to display an event report for the nth event. The parameter n ranges from 1 for the newest event through 12 for the oldest event stored in the relay memory. If n is not specified, the default value is 1 and the relay displays the newest event report.

You can control relay transmissions with the following keystrokes:

- **<CTRL>S** Pause transmission
- **<CTRL>Q** Continue transmission
- **<CTRL>X** Terminate command

The following incidents clear the event buffers:

- Interruption of control power
- Change of any relay setting
- Change of any logic mask setting

All event data are lost when event buffers are cleared. If an event buffer is empty when you request an event, the relay returns an error message:

```
=>EVENT 12 <ENTER>
Invalid event

=>
```

***Section 4: Event Reporting*** explains the generation and analysis of event reports.

## HISTORY

HISTORY displays the date, time, and type of event for each of the last 12 events.

```
=>HISTORY <ENTER>

Example Settings                    Date: 6/1/92   Time: 14:20:40

#  DATE        TIME        EVENT  TARGETS

1  6/20/91  09:03:01.092  TRIP   EN,X59T
2  6/20/91  09:02:13.041         EN
3  6/19/91  02:45:39.962         EN
4  6/18/91  17:00:13.345  TRIP   EN,87AT
5
6
7
8
9
10
11
12

=>
```

Note that only four events have occurred since the relay was set or powered on.

The time is saved to the nearest quarter-cycle (4.17 ms) and referenced to the 16th row of data in the report. All reports trigger at row 16. If a long fault triggers two event reports, you can still determine its duration. Simply calculate the time difference between the report generated at fault inception and the report generated at the TRIP.

The EVENT column provides an abbreviated indication of the event type. This is the same data presented under EVENT in the summary generated for each fault.

The EVENT indication shows the relay function that triggered the event report. This is true for all EVENT indicators except TRIP. If the TRIP output asserts anytime during the event report, event type is TRIP.

**Table 3.2: Event Type Selection**

| Event | Triggered By |
|---|---|
| TRIP | TRIP output asserted during event report |
| MER | MER programmable mask |
| ET1 | Assertion of ET1 input |
| ET2 | Assertion of ET2 input |
| TRI | TRIGGER command execution |

TARGETS indicates relay targets asserted at the instant TRIP was asserted.

## IRIG

IRIG directs the relay to read the demodulated IRIG-B time-code input at J201 on the rear panel, if a time-code signal is input.

If the relay reads the time code successfully, it updates the internal clock/calendar time and date to the time-code reading and the relay transmits a message with relay ID string, date, and time.

```
=>IRIG <ENTER>
Example Settings                    Date: 6/1/92   Time: 01:45:40

=>
```

If no signal is present or the code cannot be read successfully, the relay sends the error message "IRIGB DATA ERROR."

**Note:** Normally, it is not necessary to synchronize using this command because the relay performs it automatically every few minutes. The command is provided to prevent delays during testing and installation.

## METER n

METER displays the Source X and Y voltage magnitudes and the phase differential voltages in secondary volts rms.

```
=>METER <ENTER>

Example Settings                    Date: 6/1/92   Time: 14:10:14

   VAX      VBX      VCX      VAY      VBY      VCY      dVA      dVB      dVC
 67.03    67.03    66.94    67.00    67.03    67.00     0.03     0.00    -0.06

=>
```

The phase differential voltages are defined:

dVA = |VAX| – KA|VAY|
dVB = |VBX| – KB|VBY|
dVC = |VCX| – KC|VCY|

The optional parameter n selects the number of times meter data are displayed. To display a series of eight meter readings, type **METER 8 <ENTER>**.

## QUIT

QUIT returns control to Access Level 0 from Level 1 or 2 and resets targets to the Relay Targets (TAR 0). The command displays the relay I.D., date, and time of QUIT command execution.

Use this command when you finish communicating with the relay to prevent unauthorized access. Control returns to Access Level 0 automatically after a settable interval of no activity (see the TIME1 and TIME2 settings of the SET command).

```
=>QUIT <ENTER>

Example Settings                    Date: 6/1/92   Time: 01:45:40

=
```

## SHOWSET

SHOWSET displays the current relay and logic settings. You cannot enter or modify settings with this command. The SET command description provides complete information about settings. The following screen capture shows the Example Settings for the SEL-287V and SEL-287V-1 Relays.

```
=>SHOWSET <ENTER>

Settings for: Example Settings

X27L = 50.00  X59I = 80.00  Y27L = 50.00  Y59I = 80.00  3Y59D= 60
X59PU= 75.00  X59D = 1800   Y59PU= 75.00  Y59D = 1800   VSS  = X
59P1 = 70.00  THP1 = 60     THD1 = 60
27P1 = 65.00  TLP1 = 60     TLD1 = 60
59P2 = 70.00  THP2 = 60     THD2 = 60
27P2 = 65.00  TLP2 = 60     TLD2 = 60
KA   = 1.012  KB   = 1.012  KC   = 1.012
87AA = 0.50   87BA = 0.50   87CA = 0.50   87T  = 1.00   87H  = 2.00
87APD= 60     87TPD= 60     87HPD= 30     87DO = 60
A1PD =O       A2PD = O      A3PD = O      A4PD = O      A5PD = O
TDUR = 4      LTCHE= N      LOPE1= Y      LOPE2= Y      LOPD = 60
TIME1= 5      TIME2= O      AUTO = 2      RINGS= 3

Logic settings:

MT  MA1  MA2  MA3  MA4  MA5  MER
EE  00   EE   00   EE   00   EE
00  00   00   00   00   00   00
50  00   50   00   50   00   F0
08  04   00   01   02   00   08
40  00   40   00   40   1D   60
02  00   02   00   02   01   03

=>
```

The following screen capture shows Example Settings for the SEL-287V-2 Relay.

```
=>SHOWSET <ENTER>

Settings for: SEL-287V-2 Default Settings

X27L = 50.00  X59I = 80.00  Y27L = 50.00  Y59I = 80.00  3Y59D= 60
X59PU= 75.00  X59D = 1800   Y59PU= 75.00  Y59D = 1800   VSS  = X
59P1 = 70.00  THP1 = 60     THD1 = 60
27P1 = 65.00  TLP1 = 60     TLD1 = 60
59P2 = 70.00  THP2 = 60     THD2 = 60
27P2 = 65.00  TLP2 = 60     TLD2 = 60
KA   = 1.012  KB   = 1.012  KC   = 1.012
87A1P= 0.50   87A2P= 0.50   87T1P= 1.00   87T2P= 1.00
87H1P= 2.00   87H2P= 2.00
87APD= 60     87TPD= 60     87HPD= 30     87DO = 60
A1PD =O       A2PD = O      A3PD = O      A4PD = O      A5PD = O
TDUR = 4      LTCHE= N      LOPE1= Y      LOPE2= Y      LOPD = 60
TIME1= 5      TIME2= O      AUTO = 2      RINGS= 3

Logic settings:

MT  MA1  MA2  MA3  MA4  MA5  MER
EE  00   EE   00   EE   00   EE
00  00   00   00   00   00   00
50  00   50   00   50   00   F0
08  04   00   01   02   00   08
40  00   40   00   40   1D   60
02  00   02   00   02   09   0B

=>
```

The LOGIC command description includes a detailed explanation of the logic settings. Each column in the logic settings display shows the masks for six rows of the Relay Word. The LOGIC command description later in this section contains Relay Word tables for both the SEL-287V Relay and the SEL-287V-2 Relay.

Logic settings appear in hexadecimal format. Table 3.3 provides equivalencies between hexadecimal (hex) and binary numbers. Use the table when you examine logic settings in event reports and the SHOWSET display.

**Table 3.3: Hexadecimal/Binary Conversion**

| Binary | Hexadecimal | Binary | Hexadecimal |
|---|---|---|---|
| 0000 | 0 | 1000 | 8 |
| 0001 | 1 | 1001 | 9 |
| 0010 | 2 | 1010 | A |
| 0011 | 3 | 1011 | B |
| 0100 | 4 | 1100 | C |
| 0101 | 5 | 1101 | D |
| 0110 | 6 | 1110 | E |
| 0111 | 7 | 1111 | F |

For example, consider row 5 of mask MA5, which is set to 1D hex format. Using the table, convert 1D to binary:

1D – > 0001 1101.

Now, build the Relay Word for row 5 of mask MA5 as follows:

```
87H     87HD    LOP     LOPD    VCI1    VCI2    87T     87A
 0       0       0       1       1       1       0       1
  _______    1    _______         _______    D    _______
```

## STATUS

STATUS allows inspection of self-test status. The relay automatically executes the STATUS command whenever a self-test enters warning or failure state. If this occurs, the relay transmits a STATUS report from the port(s) designated automatic (see SET command, AUTO setting).

The STATUS report format appears below.

```
=>STATUS <ENTER>

Example Settings                    Date: 6/1/92   Time: 14:10:31

SELF TESTS

W=Warn F=Fail
      VAX   VBX   VCX   VAY   VBY   VCY
OS     0     0     0     0     0     0
PS     5.07     14.91    -14.99
RAM    ROM    A/D    MOF    SET
OK     OK     OK     OK     OK

=>
```

The OS row indicates measured dc offset voltages for the six analog channels. An out-of-tolerance offset is indicated by a W (warning) or F (failure) following the displayed gain or offset value.

The PS row indicates voltages for the three power supply outputs.

If a RAM or ROM test fails, the IC socket number of the defective part appears in place of OK.

The A/D self-test checks the analog-to-digital conversion time.

The MOF test checks the dc offset in the MUX-PGA-A/D circuit when a grounded input is selected.

The SET self-test calculates the checksum of the settings stored in nonvolatile memory and compares it to the checksum calculated when the settings were last changed.

***Section 2: Specifications*** provides full definitions of the self-tests, their warning and failure limits, and the results of test warnings and failures.

## TARGET n k

TARGET selects the information displayed on the front-panel target LEDs and communicates the state of the selected elements.

When the relay power is on, the LED display indicates the functions marked on the front panel. The default display shows fault information from the RELAY TARGETS row of Table 3.4, which applies to the SEL-287V and SEL-287V-1 Relays.

Using the TARGET command, you may select any one of the following nine sets of data to print and display on the LEDs.

**Table 3.4: Target LED Assignment (SEL-287V, SEL-287V-1 Relays)**

| LED: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| **N** | | | | | | | | | |
| **0** | EN | 87A | 87B | 87C | X59T | Y59T | X59I | Y59I | RELAY TARGETS |
| **1** | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | RELAY WORD row 1 |
| **2** | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | RELAY WORD row 2 |
| **3** | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | RELAY WORD row 3 |
| **4** | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | RELAY WORD row 4 |
| **5** | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | RELAY WORD row 5 |
| **6** | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD | RELAY WORD row 6 |
| **7** | . | . | ET2 | ET1 | LE2 | RE2 | LE1 | RE1 | CONTACT INPUTS |
| **8** | . | TRIP | A1 | A2 | A3 | A4 | A5 | ALRM | CONTACT OUTPUTS |

**Table 3.5: Target LED Assignment (SEL-287V-2 Relay)**

| LED: | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| **N** | | | | | | | | | |
| **0** | EN | 87A | 87B | 87C | X59T | Y59T | X59I | Y59I | RELAY TARGETS |
| **1** | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | RELAY WORD row 1 |
| **2** | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | RELAY WORD row 2 |
| **3** | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | RELAY WORD row 3 |
| **4** | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | RELAY WORD row 4 |
| **5** | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | RELAY WORD row 5 |
| **6** | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D | RELAY WORD row 6 |
| **7** | . | . | ET2 | ET1 | LE2 | RE2 | LE1 | RE1 | CONTACT INPUTS |
| **8** | . | TRIP | A1 | A2 | A3 | A4 | A5 | ALRM | CONTACT OUTPUTS |

These selections are useful in testing, checking contact states, and remotely reading the targets. "1" indicates an asserted element; "0" indicates a deasserted element.

The optional command parameter k selects the number of times the relay displays target data for parameter n. The example below shows a series of 10 target readings for Relay Word row four. Target headings repeat every eight rows.

```
=>TARGET 4 10 <ENTER>

 VH1   VL1   VH2   VL2   VHD1  VLD1  VHD2  VLD2
 0     1     0     0     0     0     0     0
 0     1     0     0     0     0     0     0
 0     1     0     0     0     0     0     0
 0     1     0     0     0     0     0     0
 0     0     0     0     0     0     0     0
 0     0     0     0     0     0     0     0
 0     0     0     0     0     0     0     0
 0     0     0     0     0     0     0     0

 VH1   VL1   VH2   VL2   VHD1  VLD1  VHD2  VLD2
 0     0     0     0     0     0     0     0
 0     0     0     0     0     0     0     0

=>
```

When finished, type **TAR 0 <ENTER>** to display the relay targets so field personnel do not misinterpret displayed data.

When a serial port times out (see TIME1, TIME2 settings), the relay automatically displays the TAR 0 data. The relay also displays TAR 0 data when it sends an automatic message to a timed-out port.

Press the TARGET RESET button on the front panel to clear the TAR 0 data and illuminate all target LEDs for a one-second lamp test.

You can reset the front-panel targets to TAR 0 and clear them remotely or locally with the TARGET command. Type **TARGET R <ENTER>** to reset and clear the targets as shown below.

```
=>TARGET R <ENTER>
Targets reset

EN   87A   87B   87C   X59T  Y59T  X59I  Y59I
 1    0     0     0     0     0     0     0

=>
```

### TIME hh:mm:ss

TIME checks the internal clock. To set the clock, type **TIME** and the desired setting, then press **<ENTER>**. Separate the hours, minutes, and seconds with colons, semicolons, spaces, commas, or slashes. To set the clock to 23:30:00, enter:

```
=>TIME  23:30:00 <ENTER>
23:30:00

=>
```

A quartz crystal oscillator provides the time base for the internal clock. You can set the time clock automatically with the relay time-code input and a source of demodulated IRIG-B time code.

### TRIGGER

TRIGGER generates an event record. After command entry, the relay responds "Triggered," and displays a record summary.

```
=>TRIGGER <ENTER>
Triggered

=>

Example Settings                 Date: 6/1/92    Time: 14:05:00.670

Event   : TRI  TARGETS: EN

=>
```

Use TRIGGER to inspect the input voltages. For example, when the relay is first installed, execute the TRIGGER command, draw the phasors (***Section 4: Event Reporting*** explains how to do this), and check for the proper polarity and phase sequence of the inputs.

## Access Level 2 Commands

While all commands are available from Access Level 2, the commands below are available only from Access Level 2. Remember: the relay pulses the ALARM contacts closed for one second after any Level 2 access attempt, successful or otherwise.

### KSET n

KSET automatically calculates the voltage ratio adjustment factors, KA, KB, and KC. These factors null the differential voltages under balanced conditions:

$$dV = |VX| - K|VY| = 0$$

Thus:

$$KA = |VAX|/|VAY|$$

$$KB = |VBX|/|VBY|$$

$$KC = |VCX|/|VCY|$$

KSET calculates KA, KB, and KC and averages the values over n samples of phase voltage magnitude data. The default value of n is 60 samples. KSET uses phase voltage data collected approximately twice per system cycle.

The command output displays the present ratio adjustment factor settings. The display also contains the minimum, maximum, and average values of the sample group.

Answer **Y** at the prompt to enter the average KA, KB, and KC values as settings. The relay clears the event buffer and pulses the ALARM contacts closed when the new ratio adjustment factors

are set. If you answer **n** at the prompt, no new K factors are set and the event buffer is not cleared.

The relay calculates new ratio adjustment factors only if all phase voltage magnitudes exceed 20 volts.

You can also set the ratio adjustment factors manually with the SET command.

KSET command example:

```
=>>KSET<ENTER>

Ratio adjustment factor settings:
KA =  0.983  KB =  0.997  KC =  0.988

Calculated values:
      KA      KB      KC
MAX   0.982   0.996   0.986
AVE   0.982   0.996   0.986
MIN   0.982   0.996   0.986

Use calculated averages(Y/N)?  Y <ENTER>
Please wait...
Enabled

=>>
```

## LOGIC n

The LOGIC command programs the masks that control outputs and event report triggering.

The parameter n specifies a mask to program.

| **n** | **Mask** |
|---|---|
| MT | - Mask for trip |
| MA1 | - Mask for A1 relay control |
| MA2 | - Mask for A2 relay control |
| MA3 | - Mask for A3 relay control |
| MA4 | - Mask for A4 relay control |
| MA5 | - Mask for A5 relay control |
| MER | - Mask for event report triggering |

The logic programming procedure requires you to enter changes to the mask or press **<ENTER>** to indicate no change. Each mask listed above is split into sections that correspond to the six rows of the SEL-287V and SEL-287V-1 Relay Word as follows:

| SEL-287V, SEL-287V-1 Relay Word | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Row 1 | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D |
| Row 2 | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 |
| Row 3 | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 |
| Row 4 | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 |
| Row 5 | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A |
| Row 6 | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD |

The LOGIC command displays a header and settings for each row of the Relay Word. Next, it displays a question mark prompt and waits for input. Enter only ones and zeros as input; one selects and zero deselects a member of the Relay Word. Press **<ENTER>** when a group is satisfactory. If you wish to change any member of a group, you must re-enter all eight members, even if some remain the same. The relay displays existing settings and the question mark prompt after entry to allow corrections.

When all data are entered for each row, the relay displays the new settings and prompts for approval to enable the relay with them. **Y** enters the new data, pulses the ALARM contacts closed momentarily, and clears the event buffers. **N** retains the old settings.

LOGIC command example for the MT mask (SEL-287V and SEL-287V-1 Relays):

```
=>>LOGIC MT <ENTER>

1 selects, 0 deselects.

X59A X59B X59C 3Y59 Y59A Y59B Y59C 3Y59D
 1    1    1    0    1    1    1    0
?<ENTER>
X27A X27B X27C LTCH Y27A Y27B Y27C 3Y27
 0    0    0    0    0    0    0    0
?<ENTER>
X59P X59T Y59P Y59T 59P1 27P1 59P2 27P2
 0    1    0    1    0    0    0    0
?01000000<ENTER>
 0    1    0    0    0    0    0    0
?<ENTER>
VH1  VL1  VH2  VL2  VHD1 VLD1 VHD2 VLD2
 0    0    0    0    0    0    0    0
?<ENTER>
87H  87HD LOP  LOPD VCI1 VCI2 87T  87A
 0    0    0    0    0    0    0    0
?<ENTER>
87AT 87AA 87BT 87BA 87CT 87CA 87TD 87AD
 0    0    0    0    0    0    1    0
?<ENTER>
```

(continued on next page)

```
                                   (continued from previous page)
New MT :

X59A X59B X59C 3Y59 Y59A Y59B Y59C 3Y59D
 1    1    1    0    1    1    1    0
X27A X27B X27C LTCH Y27A Y27B Y27C 3Y27
 0    0    0    0    0    0    0    0
X59P X59T Y59P Y59T 59P1 27P1 59P2 27P2
 0    1    0    0    0    0    0    0
VH1  VL1  VH2  VL2  VHD1 VLD1 VHD2 VLD2
 0    0    0    0    0    0    0    0
87H  87HD LOP  LOPD VCI1 VCI2 87T  87A
 0    0    0    0    0    0    0    0
87AT 87AA 87BT 87BA 87CT 87CA 87TD 87AD
 0    0    0    0    0    0    1    0

OK (Y/N) ? Y <ENTER>
Enabled

Example Settings                    Date: 7/1/92   Time: 14:13:36

=>>
```

Operation is similar for the SEL-287V-2 Relay. Following is the SEL-287V-2 Relay Word and example for the MT mask.

| SEL-287V-2 Relay Word | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Row 1 | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D |
| Row 2 | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 |
| Row 3 | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 |
| Row 4 | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 |
| Row 5 | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A |
| Row 6 | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D |

The following is the LOGIC command example for the MT mask (SEL-287V-2 Relay):

```
=>>LOGIC MT <ENTER>

1 selects, 0 deselects.

X59A X59B X59C 3Y59 Y59A Y59B Y59C 3Y59D
 1    1    1    0    1    1    1    0
?<ENTER>
X27A X27B X27C LTCH Y27A Y27B Y27C 3Y27
 0    0    0    0    0    0    0    0
?<ENTER>
X59P X59T Y59P Y59T 59P1 27P1 59P2 27P2
 0    1    0    1    0    0    0    0
?01000000<ENTER>
 0    1    0    0    0    0    0    0
?<ENTER>
VH1  VL1  VH2  VL2  VHD1 VLD1 VHD2 VLD2
 0    0    0    0    0    0    0    0
?<ENTER>
87H  87HD LOP  LOPD VCI1 VCI2 87T  87A
 0    0    0    0    0    0    0    0
?<ENTER>

                                   (continued on next page)
```

```
                                  (continued from previous page)

87A1 87AA 87A2 87BA 87A1D 87CA 87TD 87A2D
 0    0    0    0    0    0    1    0
?<ENTER>

New MT :

X59A X59B X59C 3Y59 Y59A Y59B Y59C 3Y59D
 1    1    1    0    1    1    1    0
X27A X27B X27C LTCH Y27A Y27B Y27C 3Y27
 0    0    0    0    0    0    0    0
X59P X59T Y59P Y59T 59P1 27P1 59P2 27P2
 0    1    0    0    0    0    0    0
VH1  VL1  VH2  VL2  VHD1 VLD1 VHD2 VLD2
 0    0    0    0    0    0    0    0
87H  87HD LOP  LOPD VCI1 VCI2 87T  87A
 0    0    0    0    0    0    0    0
87A1 87AA 87A2 87BA 87A1D 87CA 87TD 87A2D
 0    0    0    0    0    0    1    0

OK (Y/N) ? Y <ENTER>
Enabled

Example Settings                   Date: 7/1/92   Time: 14:13:36

=>>
```

The examples above disable tripping for assertion of the Source Y definite-time overvoltage element, Y59T.

These setting examples cause the relay to trip for assertions of Source X and Source Y instantaneous overvoltage elements, the definite-time overvoltage element (X59T), and time-delayed phase differential overvoltage trip element (87TD).

**Note:** You must set the programmable logic masks properly for your application.

## PASSWORD (1 or 2) password

PASSWORD allows you to inspect or change existing passwords. To inspect passwords, type **PASSWORD <ENTER>** as shown below.

```
=>>PASSWORD <ENTER>
1: OTTER
2: TAIL

=>>
```

To change the password for Access Level 1 to BIKE enter the following:

```
=>>PASSWORD 1 BIKE <ENTER>
Set

=>>
```

The relay sets the password, pulses the ALARM relay closed, and transmits the response “Set.”

After entering new passwords, type **PASS <ENTER>** to inspect them. Make sure they are what you intended and record the new passwords.

Passwords can be any length up to six numbers, letters, or any other printable characters except delimiters (space, comma, semicolon, colon, slash). Upper- and lower-case letters are treated as different characters. Examples of valid, distinct passwords include:

OTTER otter Ot3456 +TAIL+ !@#$%^ 123456 12345. 12345

If the passwords are lost or you wish to operate the relay without password protection, install JMP103 on the main board. With no password protection, you may gain access without knowing the passwords and view or change the current passwords and settings.

## PULSE n

PULSE n closes the selected output contact for one second if jumper JMP104 is in place. The parameter n can be any of the following:

| n | Closes Contact |
|---|---|
| T | TRIP |
| 1 | A1 |
| 2 | A2 |
| 3 | A3 |
| 4 | A4 |
| 5 | A5 |
| A | ALARM |

If you do not specify n or jumper JMP104 is not in place, the command aborts and the relay displays an error message.

Use the PULSE command to control the capacitor bank locally or remotely and to verify relay connections during commissioning.

The relay generates an event report when you execute the PULSE T command.

PULSE command error messages:

| Error | Message |
|---|---|
| n not specified | Command Aborted: must specify T,1,2,3,4,5, or A |
| JMP104 not in place | Command Aborted |

## SET n

SET allows entry of relay settings. At the setting procedure prompts, enter new data or press **<ENTER>** to indicate no change. You can jump to a specific setting by entering the setting name as parameter n. If no setting is entered as an argument, the procedure initiates at the first setting, Relay ID.

The relay prompts you for each setting and checks new settings against established limits. If the setting is within range, the relay prompts you for the next setting. Press **<ENTER>** to retain an existing setting.

When you finish entering setting changes, it is not necessary to scroll through the remaining settings. Type **END** after your last change to display the new settings and enable prompt. Do not use the END statement at the Relay ID setting; use **<CTRL>X** to abort the SET procedure from this point.

After you enter all data, the relay displays the new settings and prompts for approval to enable them. Answer **Y** to approve the new settings. Error messages notify you when entries result in out-of-range settings. If all settings are acceptable, the relay enables them, closes the ALARM contacts momentarily, and clears the event buffer.

Element setting ranges:

Voltage elements: 0.00–150.00 V rms per-phase secondary in approximately 0.03-volt steps.

Timers: 0–64000 cycles in one-cycle steps unless otherwise noted.

A list of relay settings follows:

| | |
|---|---|
| ID | 39-character string to identify relay in event reports. |
| X27L | Phase undervoltage threshold for Source X. |
| X59I | Phase overvoltage threshold for Source X. |
| Y27L | Phase undervoltage threshold for Source Y. |
| Y59I | Phase overvoltage threshold for Source Y. |
| 3Y59D | Dropout delay for Source Y three-phase overvoltage condition. |
| X59PU | Pickup threshold of definite-time overvoltage element for Source X. |
| X59D | Time delay of definite-time overvoltage element for Source X. |
| Y59PU | Pickup threshold of definite-time overvoltage element for Source Y. |
| Y59D | Time delay of definite-time overvoltage element for Source Y. |
| VSS | Voltage Selection Scheme: I=independent, B=better, X= X only. |
| 59P1 | Voltage-control overvoltage setting for Scheme 1. |
| THP1 | Overvoltage control time-delay pickup. |
| THD1 | Overvoltage control time-delay dropout. |
| 27P1 | Voltage-control undervoltage setting. |
| TLP1 | Undervoltage control time-delay pickup. |
| TLD1 | Undervoltage control time-delay dropout. |
| 59P2 | Voltage-control overvoltage setting for Scheme 2. |
| THP2 | Overvoltage control time-delay pickup. |
| THD2 | Overvoltage control time-delay dropout. |
| 27P2 | Voltage-control undervoltage setting. |
| TLP2 | Undervoltage control time-delay pickup. |
| TLD2 | Undervoltage control time-delay dropout. |
| KA | 87A ratio adjustment factor (0.000–1.999). |
| KB | 87B ratio adjustment factor (0.000–1.999). |
| KC | 87C ratio adjustment factor (0.000–1.999). |
| 87AA | 87A alarm threshold (SEL-287V, SEL-287V-1). |
| 87A1P | 87 alarm threshold above tap (SEL-287V-2). |
| 87BA | 87B alarm threshold (SEL-287V, SEL-287V-1). |
| 87A2P | 87 alarm threshold below tap (SEL-287V-2). |
| 87CA | 87C alarm threshold (SEL-287V, SEL-287V-1). |
| 87T1P | 87 trip threshold above tap (SEL-287V-2). |

87T 87A, 87B, and 87C trip threshold (SEL-287V, SEL-287V-1).
87T2P 87 trip threshold below tap (SEL-287V-2).
87H 87A, 87B, and 87C high-set trip threshold (SEL-287V, SEL-287V-1).
87H1P 87 high-set trip threshold (dV>0) (SEL-287V-2).
87H2P 87 high-set trip threshold (dV≤0) (SEL-287V-2).
87APD Pickup delay for 87A differential overvoltage condition.
87TPD Pickup delay for 87T differential overvoltage condition.
87HPD Pickup delay for 87H differential overvoltage condition.
87DO Dropout delay for 87A, 87T, and 87H differential overvoltage condition and A4 and A5 output contacts.

A1PD Pickup delay for A1 output contact.
A2PD Pickup delay for A2 output contact.
A3PD Pickup delay for A3 output contact.
A4PD Pickup delay for A4 output contact.
A5PD Pickup delay for A5 output contact.

TDUR Minimum Trip Duration timer (0–255 cycles)
LTCHE Latch Bit (LTCH) enable
LOPE1 Loss-of-potential enable for Scheme 1 voltage control logic (Y or N).
LOPE2 Loss-of-potential enable for Scheme 2 voltage control logic (Y or N).
LOPD Loss-of-potential dropout delay for Source X or Y.

TIME1 Timeout for PORT 1 communications (0–30 minutes).
TIME2 Timeout for PORT 2 communications (0–30 minutes).
AUTO Destination for automatic messages (1 = Port 1; 2 = Port 2; 3 = both ports).
RINGS Number of rings after which modem on PORT 1 answers (-30 to 30 rings; excluding 0).*

**Refer to the functional description and be sure the settings you choose result in relay performance appropriate to your application.**

The AUTO setting selects PORT 1, PORT 2, or both serial ports for automatically transmitted messages. The table below shows the effect of each possible setting:

| Auto Setting | Automatic Message Destination Port |
|---|---|
| 1 | 1 |
| 2 | 2 |
| 3 | 1 and 2 |

Event summaries and self-test warning and failure reports are automatically transmitted from port(s) designated automatic regardless of access level if the designated port is not timed out. Enter zero as the timeout setting of the appropriate port if automatic transmissions will be monitored by a dedicated channel or printed on a dedicated printer.

***Note:** When the RINGS setting is negative, the setting operates on the absolute value of the setting and the new year **is not** written to EEPROM at midnight on New Year's Eve. When the RINGS setting is positive, the new year **is** written to EEPROM at midnight on New Year's Eve, disabling the relay for approximately 12 cycles.

# SEL-287V VOLTAGE DIFFERENTIAL RELAY COMMAND SUMMARY

## ACCESS LEVEL 0 COMMANDS

**ACCESS** Answer password prompt (if password protection is enabled) to enter Access Level 1. Three unsuccessful attempts pulse ALARM relay closed for one second.

## ACCESS LEVEL 1 COMMANDS

**2ACCESS** Answer password prompt (if password protection is enabled) to enter Access Level 2. This command always pulses the ALARM relay.

**DATE m/d/y** Show or set date. DAT 2/3/90 sets date to Feb. 3, 1990. IRIG-B time-code input overrides existing month and date settings. ALARM contacts pulse when year entered differs from year stored.

**EVENT** Show event record. EVE 1 shows newest event; EVE 12 shows oldest.

**HISTORY** Show DATE, TIME, EVENT, TARGETS for the last 12 events.

**IRIG** Force immediate attempt to synchronize internal relay clock to time-code input.

**METER** Display secondary and difference voltages.

**QUIT** Return control to Access Level 0; return target display to relay targets.

**SHOWSET** Display settings without affecting them.

**STATUS** Show self-test status.

**TARGET n k** Show data and set target lights as follows:

| | |
|---|---|
| TAR 0: Relay Targets | TAR 1: Relay Word #1 |
| TAR 2: Relay Word #2 | TAR 3: Relay Word #3 |
| TAR 4: Relay Word #4 | TAR 5: Relay Word #5 |
| TAR 6: Relay Word #6 | TAR 7: Contact Input States |
| TAR 8: Contact Output States | TAR R: Test and Reset targets |

Option k displays target data k times.

**TIME h/m/s** Show or set time. TIM 13/32/00 sets clock to 1:32:00 PM. IRIG-B overrides this setting.

**TRIGGER** Trigger and save an event record (event type is TRI).

## ACCESS LEVEL 2 COMMANDS

**KSET n** Calculate ratio adjustment k values (allows user to set them directly); n selects number of samples to average over, default = 60. When calculated values are set, relay pulses ALARM contacts closed and clears event buffers.

**LOGIC n** Show or set logic masks MT, MER, MA1–MA5. ALARM contacts pulse and event buffers are cleared when new settings are stored.

**PASSWORD** Show or set passwords. Command pulses ALARM relay closed momentarily after new passwords are set. PAS 1 OTTER sets Level 1 password to OTTER. PAS 2 TAIL sets Level 2 password to TAIL.

**PULSE n** Close specified output contact for one second with JMP104 installed; n= T,1,2,3,4,5, or A.

**SET n** Initiate set procedure. Optional n selects first setting. SET VSS initiates setting procedure at VSS setting. SET initiates setting procedure at beginning. ALARM contacts pulse and event buffers clear when new settings are stored.

# EXPLANATION OF EVENT REPORT

```
Example Settings                              Date: 6/1/92      Time: 10:18:54.362
FID=SEL-187V-R401-V65p-D91061-E2


  Voltage PHASOR COMPONENTS, volts secondary      Relay Word     Outputs  Inputs
                                                                TAAAAAA  RLRLEE
  VAX     VBX     VCX     VAY     VBY     VCY    R1R2 R3R4 R5R6  P12345L  EEEETT
                                                                         112212

  12.06   12.28   12.03   12.19   12.13   12.81  0000 0000 03C1  .....*.  ......
  65.94   65.97   65.97   66.19   65.13   65.00  0000 0000 03C1  .....*.  ......
 -12.03  -12.28  -12.00  -12.19  -12.13  -12.81  0000 0000 03C1  .....*.  ......
 -65.97  -65.97  -66.00  -66.19  -65.13  -64.97  0000 0000 03C1  .....*.  ......

  12.06   12.31   12.00   12.19   12.09   12.78  0000 0000 03C1  .....*.  ......
  65.94   65.94   66.00   66.19   65.13   64.97  0000 0000 03C1  .....*.  ......
 -12.09  -12.31  -12.00  -12.19  -12.03  -12.75  0000 0000 03C1  .....*.  ......
 -65.94  -65.94  -66.00  -66.22  -65.16  -65.00  0000 0000 03C3  *.*.**.  ......

Event   :TRIP  TARGETS: EN,87A
X27L = 50.00    X59I = 80.00    Y27L = 50.00    Y59I = 80.00    3Y59D= 60
X59PU= 75.00    X59D = 1800     Y59PU= 75.00    Y59D = 1800     VSS  = X
59P1 = 70.00    THP1 = 60       THD1 = 60
27P1 = 65.00    TLP1 = 60       TLD1 = 60
59P2 = 70.00    THP2 = 60       THD2 = 60
27P2 = 65.00    TLP2 = 60       TLD2 = 60
KA   = 1.012    KB   = 1.012    KC   = 1.012
87AA = 0.50     87BA = 0.50     87CA = 0.50     87T  = 1.00     87H  = 2.00
87APD= 60       87TPD= 60       87HPD= 30       87DO = 60
A1PD = 0        A2PD = 0        A3PD = 0        A4PD = 0        A5PD = 0
TDUR = 4        LTCHE= N        LOPE1= Y        LOPE2= Y        LOPD = 60
TIME1= 5        TIME2= 0        AUTO = 2        RINGS= 3
```

Voltages are in secondary volts. Rows are quarter-cycle apart. Time runs down page. Obtain phasor RMS value and angle using any entry as Q-component, and the entry immediately underneath as the P-component. For example, from top rows, VAX(Q) = 12.06, VAX(P) = 65.94. Therefore, VAX = 67.03 volts RMS secondary, at an angle of ATAN(12.00/65.94) = 10.40 with respect to the sampling clock.

| | |
|---|---|
| <FID> | Firmware Identification Data |
| <Relay Word> | Row 1 through Row 6 of the Relay Word, each row in hexadecimal representation. |
| <Outputs> | Columns show states of output contacts: ON = "*", OFF = "." TP=TRIP, A1-A5=PROGRAMMABLE, AL=ALARM |
| <Inputs> | Columns show states of input contacts RE1=Raise Enable 1, LE1=Lower Enable 1, RE2=Raise Enable 2, LE2=Lower Enable 2, ET1=External Event Report Trigger 1, ET2=External Event Report Trigger 2 |
| <Event> | Indicates function which triggered event report. TRIP=TRIP output asserted during event report MER= Assertion of an element in MER mask TRI= TRIGGER command execution ET1= ET1 input assertion ET2= ET2 input assertion |
| <Targets> | Indicates front panel targets asserted at instant event report was triggered. |
| X59I,X27L | Source X overvoltage and undervoltage settings |
| Y59I,Y27L | Source Y overvoltage and undervoltage settings |
| 3Y59D | Source Y three-phase overvoltage dropout delay |
| X59PU,X59D | Source X definite-time overvoltage pickup and time delay |
| Y59PU,Y59D | Source Y definite-time overvoltage pickup and time delay |
| VSS | Voltage Control Scheme Selection |
| 59P1,THP1,THD1 | Voltage Control Scheme 1 overvoltage pickup and time delays |
| 27P1,TLP1,TLD1 | Voltage Control Scheme 1 undervoltage pickup and time delays |
| 59P2,THP2,THD2 | Voltage Control Scheme 2 overvoltage pickup and time delays |
| 27P2,TLP2,TLD2 | Voltage Control Scheme 2 undervoltage pickup and time delays |
| KA,KB,KC | Differential overvoltage ratio adjustment factors |
| 87AA,87AB,87AC | A-phase,B-phase,C-phase differential overvoltage alarm thresholds |
| 87T | Differential overvoltage trip threshold |
| 87H | High-set differential overvoltage trip threshold |
| 87APD,87TPD,87HPD | Differential overvoltage alarm and trip pickup delays |
| 87DO | Differential overvoltage alarm, trip, A4 and A5 output dropout delays |
| A1PD-A5PD | Output contact pickup delays |
| TDUR | Minimum trip duration timer |
| LTCHE | Enable Latch Bit function |
| LOPE1,LOPE2 | Loss-of-Potential enables for Voltage Control Schemes 1 and 2 |
| LOPD | Differential overvoltage supervisory LOP condition dropout time delay |

```
TIME1,2              Communications port timeout intervals (automatic log-off)
AUTO                 Port assignment for automatic message transmissions
RINGS                Number of rings to wait before modem answers telephone
<Logic Settings>     See LOGIC command for a description of mask settings
```

# TABLE OF CONTENTS



# TABLES



# FIGURES

# SECTION 4: EVENT REPORTING

## EVENT REPORT GENERATION

The relay generates an 11-cycle event report in response to the following:

- All TRIP output assertions
- External Trigger input assertions (if LTCHE = N)
- Assertion of any element set in the MER (mask for Event Report Trigger) logic mask
- Execution of the TRIGGER command

Relay elements set in the MER mask trigger the event report generator in a level-sensitive manner. The relay does not generate multiple event reports when additional relay elements pick up. Only the first relay element of any continuous sequence triggers an event report.

Trip and External Trigger (ET1 or ET2) events are rising-edge sensitive. For these events, additional reports are generated even while any or all relay elements remain picked up. The relay triggers a second report for the same event if the trip occurs after the first report ends. Thus the relay records the beginning and end of each event for which it trips. The relay does not provide a second event report if the first TRIP output assertion at or less than seven cycles after the first report is triggered.

Triggering is recorded to the nearest quarter-cycle (4.17 ms) and referenced to the 16th row of data in the report. All reports trigger at row 16. The system also allows you to determine the duration of a long event that triggers two event reports. Simply calculate the time difference between the report generated at event inception and the report generated at the TRIP.

When the report is generated, the relay transmits a summary event report and saves the full event report in its memory. The summary report includes the identifier message entered at the beginning of the setting procedure, date, time, type of event, and relay targets asserted at the time of trip.

The summary report automatically is transmitted from the port(s) designated automatic with the AUTO setting, regardless of access level, as long as the designated port is not timed out. Enter zero for the timeout setting of the appropriate port if the automatic transmissions are monitored by a dedicated channel or printed on a dedicated printer.

Due to the length of the full report, it is not automatically transmitted. You can display the full report with the EVENT command.

The full report contains voltage information in secondary volts. You can use this information to construct phasor diagrams of the voltages. The full report also contains the states of all Relay Word elements, inputs, and outputs. These are useful in reviewing event duration, relay element responses, etc.

The 12 most recent events are stored in volatile memory. You may quickly review stored events with the HISTORY command.

The relay clears the event report buffer after the following conditions:

- Loss of control power
- Entry of a new setting via the SET, KSET, or LOGIC commands

## INTERPRETATION OF VOLTAGE DATA

The relay receives secondary quantities via the rear panel, completes the processes listed below, and stores the data for event reporting:

1. Input analog signals are filtered by two-pole, low-pass filters with cutoff frequencies of about 85 Hz.

2. Filtered analog signals are sampled four times per power system cycle and converted to numerical values.

3. A digital filter processes the sample data and removes dc and ramp components. The unit sample response of this filter is:

   1, -1, -1, 1

   This filter has the property of a double differentiator-smoother.

4. The latest four samples are processed through the digital filter every quarter-cycle. Successive outputs of the filter arrive every 90°. With respect to the present value of the filter output, the previous value was taken one-quarter cycle earlier and appears to be leading the present value by 90°.

These filter output values can be used to represent the signals as phasors:

The previous value of the output is the y-component.
The present value of the output is the x-component.

It may seem confusing to refer to the older data as the leading component of the phasor. The following example may help.

Consider a sinewave having zero phase shift with respect to t=0 and a peak amplitude of 1. Now consider two samples, one taken at t=0, the other taken 90° later. They have values 0 and 1, respectively. By the above rules, the phasor components are (x,y) = (1,0).

Now consider a cosine function. Its samples taken at t=0 and t+90° are 1 and 0; its phasor representation is (0,1). The phasor (0,1) leads the phasor (1,0) by 90°. This coincides with a 90° lead of the cosine function over the sine function.

To construct a phasor diagram of voltages and currents, select a pair of adjacent rows from an area of interest in the event report. On Cartesian coordinates, plot the lower row (newer data) as the x-components and the upper row (older data) as the y-components. Rotate the completed diagram to any angle of reference. The magnitude of any phasor equals the square root of the sum of its components squared.

Note that moving forward a quarter-cycle rotates all phasors 90°. You can verify this by plotting the phasor diagram with rows 1 and 2, then rows 2 and 3 of an event report.

For example, two consecutive filter outputs of a voltage channel could be:

Row y: 65.98 volts
Row x: 11.63 volts

Convert these to polar form (magnitude and angle):

$|V| = \text{sqrt}(x^2 + y^2)$
$/V = \arg(y/x)$

$|V| = 67$ volts rms
$/V = 80°$

## CONNECTION CHECK

The following procedure is a method for quickly checking the voltage connection polarity with event report data. Consider Figure 4.1, below.

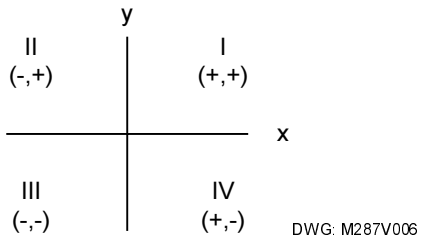



**Figure 4.1: Coefficients of the Rectangular Coordinates of Phasors in Each Quadrant**

If a phasor is expressed in rectangular coordinate format (x,y), you can determine the phasor quadrant from the signs of the rectangular coordinates which represent it. For example, a phasor whose rectangular coordinates (x,y) are both positive lies in quadrant I. A phasor with rectangular coordinate signs (+,–) lies in quadrant IV.

This fact may help you check the polarity and sequence of voltage connections to the relay.

1. With voltages connected to the relay, type **TRIGGER <ENTER>** to execute the trigger command.

2. Type **EVENT <ENTER>** to view the event report generated, and press **<CTRL>S** to stop the event report before the first two rows of data scroll off the screen.

3. Using the first two rows of the event report (Row 1 = y, Row 2 = x), determine the quadrant of the A-phase voltage using the signs of the x and y voltage samples.

4. Take note of the A-phase voltage quadrant, then determine the quadrants of the B- and C-phase voltages. No two phase voltages should lie in the same quadrant. You can also use this information to check phase rotation. Compare Source X and Source Y voltages to ensure that sources are compatibly wired.

## RELAY WORD

The three columns headed “Relay Word” indicate the states of Relay Word elements. These columns list the state of each row in the Relay Word for a given quarter-cycle. Row 1 is under the heading R1, row 2 under R2, etc. You can decode the two-digit hexadecimal representation to check the states of all Relay Word elements. The SHOWSET command description in

***Section 3: Communications*** includes a table to help you decode Relay Word information in the event report.

## CONTACT OUTPUTS AND INPUTS

The next two columns (headed "Outputs" and "Inputs") show the states of all output and input contacts. The report indicates assertion of any output or input contact with an asterisk (*) in the corresponding column; deassertion is indicated with a period. The following list shows the contents of these columns.

OUTPUTS

TP : TRIP output
A1 : Programmable output #1
A2 : Programmable output #2
A3 : Programmable output #3
A4 : Programmable output #4
A5 : Programmable output #5
AL : ALARM output

INPUTS

RE1: Raise Enable 1
LE1: Lower Enable 1
RE2: Raise Enable 2
LE2: Lower Enable 2
ET1: External Trigger 1/LTCH Reset
ET2: External Trigger 2/LTCH Set

## EVENT

The EVENT indication shows the relay function that triggered the event report. This is true for all EVENT indicators except TRIP. If the TRIP output asserts anytime during the event report, the EVENT type is TRIP.

**Table 4.1: Event Type Selection**

| Event | Triggered By |
|---|---|
| TRIP | TRIP output asserted during event report |
| MER | MER programmable mask |
| ET1 | Assertion of ET1 input |
| ET2 | Assertion of ET2 input |
| TRI | TRIGGER command execution |

## TARGETS

TARGETS indicates relay targets which were asserted the quarter-cycle when TRIP was asserted. IF TRIP did not assert during the event report, TARGETS shows the relay targets asserted when the relay triggered the event report.

The enable target, EN, is set when the relay is enabled. The instantaneous overvoltage X59I and Y59I targets operate from the OR-ed output of the X and Y source phase overvoltage elements. The definite-time overvoltage X59T and Y59T targets operate directly from their Relay Word elements. Differential overvoltage targets operate from the logical "AND" combination of the phase differential overvoltage trip elements and the LOPD supervised 87T and 87H bits, as shown below:

87A = (87AT * 87T) + (87AH * 87H)
87B = (87BT * 87T) + (87BH * 87H)
87C = (87CT * 87T) + (87CH * 87H)

In this manner, if the 87AT element picks up but LOPD is asserted when tripping occurs, 87T does not assert, and the relay does not set the 87AT target. Note that 87AH, 87BH, and 87CH are internal quantities used for targeting and are not available for use in masks. The other quantities are Relay Word bits.

## EXAMPLE EVENT REPORT

An example event report appears on the following page. The event report was generated in response to a simulated differential overvoltage condition on Phase A.

**Example Event Report**

```
Example Settings                          Date: 6/1/92       Time: 10:18:54.362
FID=SEL-187V-R401-V65p-D910612-E2

  Voltage PHASOR COMPONENTS, volts secondary      Relay Word     Outputs  Inputs
                                                                TAAAAAA  RLRLEE
  VAX     VBX     VCX     VAY     VBY     VCY    R1R2 R3R4 R5R6  P12345L  EEEETT
                                                                         112212

   11.53   11.75   11.47   11.66   11.53   12.25  0000 0000 03C0  .......  ......
   66.03   66.00   66.03   66.31   65.22   65.13  0000 0000 03C0  .......  ......
  -11.53  -11.75  -11.50  -11.69  -11.59  -12.34  0000 0000 03C0  .......  ......
  -66.03  -66.03  -66.03  -66.34  -65.19  -65.13  0000 0000 03C0  .......  ......

   11.53   11.78   11.53   11.75   11.66   12.41  0000 0000 03C0  .......  ......
   66.06   66.06   66.06   66.31   65.19   65.09  0000 0000 03C0  .......  ......
  -11.63  -11.84  -11.59  -11.78  -11.69  -12.44  0000 0000 03C0  .......  ......
  -66.03  -66.06  -66.06  -66.28  -65.22  -65.06  0000 0000 03C0  .......  ......

   11.72   11.94   11.69   11.81   11.75   12.47  0000 0000 03C0  .......  ......
   66.00   66.03   66.03   66.28   65.22   65.03  0000 0000 03C0  .......  ......
  -11.81  -12.03  -11.78  -11.88  -11.84  -12.50  0000 0000 03C0  .......  ......
  -66.00  -66.03  -66.03  -66.28  -65.19  -65.06  0000 0000 03C0  .......  ......

   11.97   12.19   11.91   11.97   11.94   12.63  0000 0000 03C0  .......  ......
   65.97   66.00   66.03   66.28   65.19   65.06  0000 0000 03C0  .......  ......
  -12.09  -12.31  -12.03  -12.13  -12.06  -12.78  0000 0000 03C0  .......  ......
  -65.91  -65.94  -65.97  -66.22  -65.16  -65.00  0000 0000 03C1  .....*.  ......

                                    (continued on next page)
```

```
                                  (continued from previous page)
  12.06   12.28   12.03   12.19   12.13   12.81  0000 0000 03C1  .....*.  ......
  65.94   65.97   65.97   66.19   65.13   65.00  0000 0000 03C1  .....*.  ......
 -12.03  -12.28  -12.00  -12.19  -12.13  -12.81  0000 0000 03C1  .....*.  ......
 -65.97  -65.97  -66.00  -66.19  -65.13  -64.97  0000 0000 03C1  .....*.  ......

  12.06   12.31   12.00   12.19   12.09   12.78  0000 0000 03C1  .....*.  ......
  65.94   65.94   66.00   66.19   65.13   64.97  0000 0000 03C1  .....*.  ......
 -12.09  -12.31  -12.00  -12.19  -12.03  -12.75  0000 0000 03C1  .....*.  ......
 -65.94  -65.94  -66.00  -66.22  -65.16  -65.00  0000 0000 03C3  *.*.**.  ......

  12.13   12.31   12.00   12.22   12.03   12.75  0000 0000 03C3  *.*.**.  ......
  65.94   65.94   66.00   66.22   65.16   65.00  0000 0000 03C3  *.*.**.  ......
 -12.13  -12.31  -12.03  -12.22  -12.06  -12.78  0000 0000 03C3  *.*.**.  ......
 -65.94  -65.97  -66.00  -66.22  -65.13  -65.00  0000 0000 03C3  *.*.**.  ......

  12.16   12.38   12.13   12.22   12.09   12.84  0000 0000 03C3  *.*.**.  ......
  65.94   65.97   65.97   66.25   65.13   65.00  0000 0000 03C3  *.*.**.  ......
 -12.22  -12.44  -12.19  -12.28  -12.13  -12.91  0000 0000 03C3  *.*.**.  ......
 -65.94  -65.94  -65.97  -66.25  -65.16  -65.00  0000 0000 03C3  *.*.**.  ......

  12.28   12.47   12.25   12.38   12.19   12.97  0000 0000 03C3  *.*.**.  ......
  65.94   65.94   65.97   66.22   65.16   65.00  0000 0000 03C3  *.*.**.  ......
 -12.34  -12.56  -12.31  -12.47  -12.28  -13.03  0000 0000 03C3  *.*.**.  ......
 -65.91  -65.91  -65.94  -66.19  -65.13  -64.97  0000 0000 03C3  *.*.**.  ......

  12.38   12.63   12.34   12.56   12.38   13.09  0000 0000 03C3  *.*.**.  ......
  65.88   65.88   65.91   66.16   65.09   64.91  0000 0000 03C3  *.*.**.  ......
 -12.41  -12.66  -12.38  -12.63  -12.44  -13.13  0000 0000 03C3  *.*.**.  ......
 -65.91  -65.88  -65.91  -66.13  -65.06  -64.91  0000 0000 03C3  *.*.**.  ......

  12.53   12.75   12.47   12.63   12.47   13.19  0000 0000 03C3  *.*.**.  ......
  65.91   65.84   65.91   66.13   65.06   64.91  0000 0000 03C3  *.*.**.  ......
 -12.63  -12.81  -12.59  -12.66  -12.53  -13.25  0000 0000 03C3  *.*.**.  ......
 -65.88  -65.81  -65.88  -66.13  -65.03  -64.88  0000 0000 03C3  *.*.**.  ......

Event   :TRIP  TARGETS: EN,87A
X27L = 50.00    X59I = 80.00    Y27L = 50.00    Y59I = 80.00    3Y59D= 60
X59PU= 75.00    X59D = 1800     Y59PU= 75.00    Y59D = 1800     VSS  = X
59P1 = 70.00    THP1 = 60       THD1 = 60
27P1 = 65.00    TLP1 = 60       TLD1 = 60
59P2 = 70.00    THP2 = 60       THD2 = 60
27P2 = 65.00    TLP2 = 60       TLD2 = 60
KA   = 1.012    KB   = 1.012    KC   = 1.012
87AA = 0.50     87BA = 0.50     87CA = 0.50     87T  = 1.00     87H  = 2.00
87APD= 60       87TPD= 60       87HPD= 30       87D0 = 60
A1PD = 0        A2PD = 0        A3PD = 0        A4PD = 0        A5PD = 0
TDUR = 4        LTCHE= N        LOPE1= Y        LOPE2= Y        LOPD = 60
TIME1= 5        TIME2= 0        AUTO = 2        RINGS= 3

Logic settings:
MT  MA1  MA2  MA3  MA4  MA5  MER
EE   00   EE   00   EE   00   EE
00   00   00   00   00   00   00
50   00   50   00   50   00   F0
08   04   00   01   02   00   08
40   00   40   00   40   1D   60
02   00   02   00   02   01   03
```

The following is the first six cycles of the Example Event Report, showing pretrip and trip data recorded by the relay.

```
   Voltage PHASOR COMPONENTS, volts secondary      Relay Word     Outputs  Inputs
                                                                 TAAAAAA  RLRLEE
   VAX     VBX     VCX     VAY     VBY     VCY    R1R2 R3R4 R5R6 P12345L  EEEETT
                                                                         112212
                                                                              Quarter-Cycle

    11.53   11.75   11.47   11.66   11.53   12.25  0000 0000 03C0 .......  ......      1
    66.03   66.00   66.03   66.31   65.22   65.13  0000 0000 03C0 .......  ......      2
   -11.53  -11.75  -11.50  -11.69  -11.59  -12.34  0000 0000 03C0 .......  ......      3
   -66.03  -66.03  -66.03  -66.34  -65.19  -65.13  0000 0000 03C0 .......  ......      4

    11.53   11.78   11.53   11.75   11.66   12.41  0000 0000 03C0 .......  ......      5
    66.06   66.06   66.06   66.31   65.19   65.09  0000 0000 03C0 .......  ......      6
   -11.63  -11.84  -11.59  -11.78  -11.69  -12.44  0000 0000 03C0 .......  ......      7
   -66.03  -66.06  -66.06  -66.28  -65.22  -65.06  0000 0000 03C0 .......  ......      8

    11.72   11.94   11.69   11.81   11.75   12.47  0000 0000 03C0 .......  ......      9
    66.00   66.03   66.03   66.28   65.22   65.03  0000 0000 03C0 .......  ......     10
   -11.81  -12.03  -11.78  -11.88  -11.84  -12.50  0000 0000 03C0 .......  ......     11
   -66.00  -66.03  -66.03  -66.28  -65.19  -65.06  0000 0000 03C0 .......  ......     12

    11.97   12.19   11.91   11.97   11.94   12.63  0000 0000 03C0 .......  ......     13
    65.97   66.00   66.03   66.28   65.19   65.06  0000 0000 03C0 .......  ......     14
   -12.09  -12.31  -12.03  -12.13  -12.06  -12.78  0000 0000 03C0 .......  ......     15
   -65.91  -65.94  -65.97  -66.22  -65.16  -65.00  0000 0000 03C1 .....*.  ......     16

    12.06   12.28   12.03   12.19   12.13   12.81  0000 0000 03C1 .....*.  ......     17
    65.94   65.97   65.97   66.19   65.13   65.00  0000 0000 03C1 .....*.  ......     18
   -12.03  -12.28  -12.00  -12.19  -12.13  -12.81  0000 0000 03C1 .....*.  ......     19
   -65.97  -65.97  -66.00  -66.19  -65.13  -64.97  0000 0000 03C1 .....*.  ......     20

    12.06   12.31   12.00   12.19   12.09   12.78  0000 0000 03C1 .....*.  ......     21
    65.94   65.94   66.00   66.19   65.13   64.97  0000 0000 03C1 .....*.  ......     22
   -12.09  -12.31  -12.00  -12.19  -12.03  -12.75  0000 0000 03C1 .....*.  ......     23
   -65.94  -65.94  -66.00  -66.22  -65.16  -65.00  0000 0000 03C3 *.*.**.  ......     24
```

The outline below lists observed incidents in the Example Event Report on a quarter-cycle basis.

**Quarter Cycle** **Event Report Shows:**

1–15 Pretrip conditions; differential overvoltage condition:

- The hexadecimal representation of Relay Word Row 5 (R5) is 03. This shows that the 87T and 87A elements are picked up, which indicates that there is a voltage unbalance condition above the trip and alarm levels and that no LOP condition is detected. This also indicates that the 87APD and 87TPD pickup-delays are timing.

- The hexadecimal representation of Relay Word Row 6 (R6) is C0. This shows that the 87AT and 87AA elements are picked up, which indicates that a voltage unbalance condition exists on A-phase that is greater then the settings of 87T and 87AA.

16–23 Alarm condition detected:

- The A5 output column indicates that the alarm contact (A5 output contact) has closed. This is caused by the assertion of the 87AD bit that has been set in the MA5 logic mask. The 87AD bit in Relay Word remains asserted until the end of the event.
- The hexadecimal representation of Relay Word Row 5 (R5) is 03. This shows that the 87T and 87A elements are picked up, which indicates that there is a voltage unbalance condition above the trip and alarm levels and that no LOP condition is detected.
- The hexadecimal representation of Relay Word Row 6 (R6) is C1. This shows that the 87AT and 87AA elements are picked up, which indicates that a voltage unbalance condition exists on A-phase that is greater then the settings of 87T and 87AA and that the 87APD timer has timed out, asserting the 87AD bit in the Relay Word.

24–44

- The TP and A2 output columns indicate that the trip output contact and reset automatic control output contact have closed. This is caused by assertion of the 87TD that has been set in the MT and MA2 logic masks. TP (trip output contact) issues a trip to the circuit breaker and A2 (A2 output contact) sets the automatic voltage control scheme to the manual mode so that the relay does not reinsert the bank. The 87TD bit remains asserted until the end of the event.
- The hexadecimal representation of Relay Word Row 5 (R5) is 03. This shows that the 87T and 87A elements are picked up, which indicates that there is a voltage unbalance condition above the trip and alarm levels and that no LOP condition is detected.
- The hexadecimal representation of Relay Word Row 6 (R6) is C3. This shows that the 87AT and 87AA elements are picked up, which indicates that a voltage unbalance condition exists on A-phase that is greater then the settings of 87T and 87AA, the 87APD timer has timed out and asserted the 87AD bit in the Relay Word, and the 87PD timer has timed out and asserted the 87TD bit in the Relay Word.

Note that the time-delayed differential overvoltage alarm element (87AD) times out before the time-delayed differential overvoltage trip element. Since the 87A setting is set at a lower pick-up value than the 87T setting, the 87A will operate faster than the 87T. The 87APD and 87TPD timers are both set at 60 cycles, so that any difference in element pickup times will show in the event report.

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# SECTION 5: APPLICATIONS

## CAPACITOR BANK PROTECTION AND CONTROL

Shunt capacitors provide reactive support to transmission and distribution systems under high load conditions that may cause decreased system voltage. Insertion of a shunt capacitor at a substation bus results in a proportional voltage rise based upon the shunt bank size (MVAR rating) and the redistribution of the reactive power flow in the system.

Because it is difficult to manufacture a single shunt capacitor for typical transmission voltages (115 kV and greater), capacitor banks can consist of tens or hundreds of capacitor units (capacitor cans) in series-parallel groups. These can withstand the system voltage and provide the specified VAR rating. Each of the individual units consists of a number of elements connected in series/parallel combination. The series connection forms a voltage divider; the number of capacitors in series is a function of the individual capacitor can rated voltage and the system rated voltage. The parallel connection provides the necessary VAR for the bank.

Earlier can designs used a PCB-impregnated, highly refined paper as the solid dielectric material. This paper, however, had many voids or flaws that resulted in concentrated electric stress points. Use of several layers of paper helped to avoid weak spots in the unit and to ensure high insulation strength. The design, however, resulted in higher dielectric losses that caused high temperature spots and deterioration of dielectric strength. Charring, arcing, and gassing occurred in the event of dielectric puncture, resulting in the eventual rupturing of the can.

Modern day design uses polypropylene film, which is a higher quality dielectric material than the paper in earlier can designs. This results in fewer flaws or voids and decreased dielectric losses, because the latest design typically uses only two layers of very thin film. Dielectric punctures now result in no arcing, but rather welding of the aluminum foil electrodes. For the earlier units, prompt disconnection of the failed capacitor can by blowing the appropriate fuse was an essential requirement for achieving an acceptably low probability of can rupture. Because there is a much lower probability of can rupture, capacitors manufactured with the new technology have no fuses.

Capacitor cans on shunt capacitor banks are, therefore, either fused internally or externally. Later designs are fuseless. The SEL-287V Relay provides fast and reliable protection for all three capacitor can types. The voltage differential elements in the SEL-287V Relay are immune to system unbalances, allowing more sensitive settings and faster operating times. This reduces the overvoltage stress on shunt capacitors. The SEL-287V Relay includes all elements necessary for switching the bank in and out automatically for specified voltage ranges. It also provides definite-time and instantaneous overvoltage elements to trip the bank when a system overvoltage condition could stress the capacitors beyond the capacitor voltage ratings.

### Internally Fused Capacitor Bank

In internally fused capacitors there is a fusible link in series with each capacitor element inside the can. A capacitor unit has a large number of elements connected in parallel with only a few connected in series. If an element fails in an internally fused capacitor unit, the fuse isolates the faulty element. The voltage across the remaining healthy elements in that series group increases, thereby increasing the probability of subsequent failures in the same group. Blowing of a fuse following an element failure results in removal of only a small part of the capacitor unit, allowing the capacitor unit and bank to remain in service. In general, internally fused capacitor banks are

configured with fewer parallel groups, but more series groups, as opposed to banks with externally fused capacitor units.

Advantages:

- There is no need for external fuses, fuse rail assemblies, or insulators.
- This design is suitable for smaller banks.
- The bank construction is very compact and requires less space.
- The bank design reduces the exposure to faults from animals and increases reliability and availability.

Disadvantages:

- There is no visible indication of failure.
- This design requires very sensitive unbalance protection, especially in large banks.
- Capacitor voltage rating is limited.
- Testing is difficult.

## Externally Fused Capacitor Bank

An individual, external fuse protects each capacitor unit. This design has many elements in series within the capacitor unit. Each series group consists of a few elements in parallel. Despite the fact that a fault in one capacitor element shorts out an entire parallel group, it does not always result in the fuse blowing. Such a fault causes overvoltage on the remaining elements, which increases the possibility of them failing. Within a relatively short period of time, another element failure occurs, typically resulting in the fuse blowing.

An externally fused capacitor bank consists of many capacitor units in parallel within each series group. The minimum number of capacitor units per group depends on overvoltage considerations when the fuse blows on any one of the capacitor units in the group. Generally, the isolation of any one capacitor unit in a group should not cause a voltage rise to more than 110 percent of rated voltage on the remaining units in the group. This is because the capacitor cans have a maximum continuous overvoltage rating of 110 percent. The maximum number of capacitor units placed in parallel per series group is limited by a high frequency transient current that flows from discharging capacitors in the same parallel group through the faulted unit and its fuse. The fuse holder and the failed capacitor unit should withstand this discharge current.

Advantages:

- A higher unbalance current means that this design requires less sensitive unbalance protection.
- The blown fuse provides a visible means to identify a faulty unit.
- Field checking is easy.
- This design provides protection for flashover on the bushing of the capacitor unit.

- The availability of this design in higher voltage units simplifies the construction of EHV banks.

Disadvantages:

- This design is unsuitable for smaller sized banks, because a single unit represents a large portion of the total VAR of the bank.
- Fuse clearance distance causes the bank to need more space.
- Pollution, corrosion, and fluctuating climatic conditions reduce the reliability of fuses.
- Because the bank connections are not isolated, small animals can climb on the bank and cause flashovers.

## Fuseless Capacitor Bank

Fuseless capacitor units eliminate fuses altogether. High-quality insulating materials used in present day capacitors, combined with low dielectric partial discharge, eliminate the fear of can rupture and the corresponding need for fuses. Fuseless capacitor units consist of a few elements in parallel and many in series, similar to the construction of externally fused capacitor units. The capacitor bank consists of a number of individual strings of capacitor units connected in series without parallel cross-connection between them. Failure of an individual capacitor element shorts the complete parallel group of elements, but produces a very small voltage increase on the remaining series elements in the string. All series elements divide the small voltage increase equally, so that subsequent element failure in the same string is unlikely.

Advantages:

- Elimination of fuse energy dissipation results in lower power losses.
- This design offers improved flexibility and standardization.
- Reduced exposure to animals increases reliability and availability.
- A smaller physical bank size provides the same KVAR rating.
- This design is suitable for any size capacitor bank.
- Can rupture is less likely.

Disadvantages:

- Failure of one element results in an overvoltage on all remaining elements in the same string.
- Because there is no visual indication of fault position, you must measure all units should the unbalance protection operate.

## Application Using the SEL-287V Relay

The SEL-287V Relay provides low cost, high accuracy and very sensitive protection for grounded shunt capacitor banks. You can apply the relay to all types of capacitor units (with or

without fuses) and for different capacitor bank configurations. The next sections discuss the best ways to use the relay in different applications.

### Grounded Single Wye-Connected Bank

In this configuration the X input to the voltage differential element of the SEL-287V Relay comes from the busbar (line) voltage transformer or CVT. The relay uses this quantity for both overvoltage and undervoltage bank protection. The second differential element voltage input can be from one of two sources:

1) A PT at the midpoint of the capacitor bank, or as close as possible in the case of an odd number of series groups. This connection is common for fused capacitor units and fuseless capacitor banks with only one string per phase. The tap voltage connection to the midpoint ensures the same differential voltage for faults in the top and bottom halves of the bank (see Note). This method works fairly well for externally fused capacitor banks, but it should not be used for large internally fused banks and larger fuseless applications. Apply the second method for the latter cases.

**Note:** The SEL-287V-2 Relay is an enhanced version of the standard SEL-287V Relay. The voltage differential function was modified to provide separate voltage thresholds for detection of failures above and below the tap point. The voltage differential quantity for each phase (dVA, dVB, and dVC) has been changed from a magnitude-only variable to a signed variable. With this modification, faults above and below the tap point have the same sensitivity, independent of the tap point position. In case of failures in the capacitor bank, the relay indicates the relative location of the faulty unit (above or below the tap point). For the SEL-287V-2 Relay, the voltage tap connection does not have to be at the midpoint.

2) A PT at the bottom group of the parallel capacitors. This capacitor unit should be of a better quality and higher underrating factor (the rated nominal voltage can be as much as twice the value of normal operating voltage). This ensures a low probability of failure in this group and high sensitivity for any faults in the remaining capacitors. The additional cost of low-voltage capacitors is compensated by the much lower price for low voltage potential transformers, typically less than 1000 V.

### Grounded Double Wye-Connected Bank

Large capacitor banks often exceed the limitations of the maximum number of units in parallel (for externally fused application); or, the total number of capacitor elements in the bank is so large that the unbalance protection is no longer sensitive enough. The bank may now be configured into two wye sections. The characteristics of the grounded double-wye bank are similar to those of a single grounded-wye bank. The two neutrals should have a single grounding point. Because of the size and cost of the bank, a second relay is often installed. This can be a second voltage differential element or neutral voltage/current unbalance element. The following two methods are the most common for this application:

1) Equip each of the two wye connections with a separate unbalance protection relay. The bank is now considered to be two single wye-connected banks, with all the rules applicable to that application. The scheme requires two SEL-287V Relays, one for each wye configuration.

2) For each wye connection, a low-voltage capacitor in the bottom row provides inputs to the differential elements of the SEL-287V Relay. This arrangement requires only one relay per

bank. For critical installations, connect a second relay in parallel with the first relay (two SEL-287V Relays in parallel). This creates redundancy of the protection scheme.

The following examples apply to the SEL-287V, SEL-287V-1, and SEL-287V-2 Relays unless indicated otherwise.

## INTERNALLY FUSED GROUNDED-WYE CAPACITOR BANK EXAMPLE

This section provides example settings and calculations to protect and control the capacitor bank described in Table 5.1.

**Table 5.1: Example Internally Fused Capacitor Bank Data**

| Item | Description |
|---|---|
| Capacitor Bank Configuration | Shunt, Grounded-Wye |
| Series groups per phase, S | 8 |
| Capacitors per group, P | 4 |
| Capacitor Unit | |
| Type | Internally Fused |
| Capacitor Rated Voltage, Vcan | 6700 V |
| Reactive Power Rating, Q | 318 kVar |
| Parallel Connection of Capacitor Elements, q | 12 |
| Series Connection of Capacitor Elements, r | 3 |
| Nominal Bus Voltage, Vbus | 88 kV |
| Bus Potential Transformer Ratio, PTRb | 800 : 1 |
| Tap Potential Transformer Ratio, PTRt | 400 : 1 |
| Capacitor Groups Below the Tap, T | 4 |

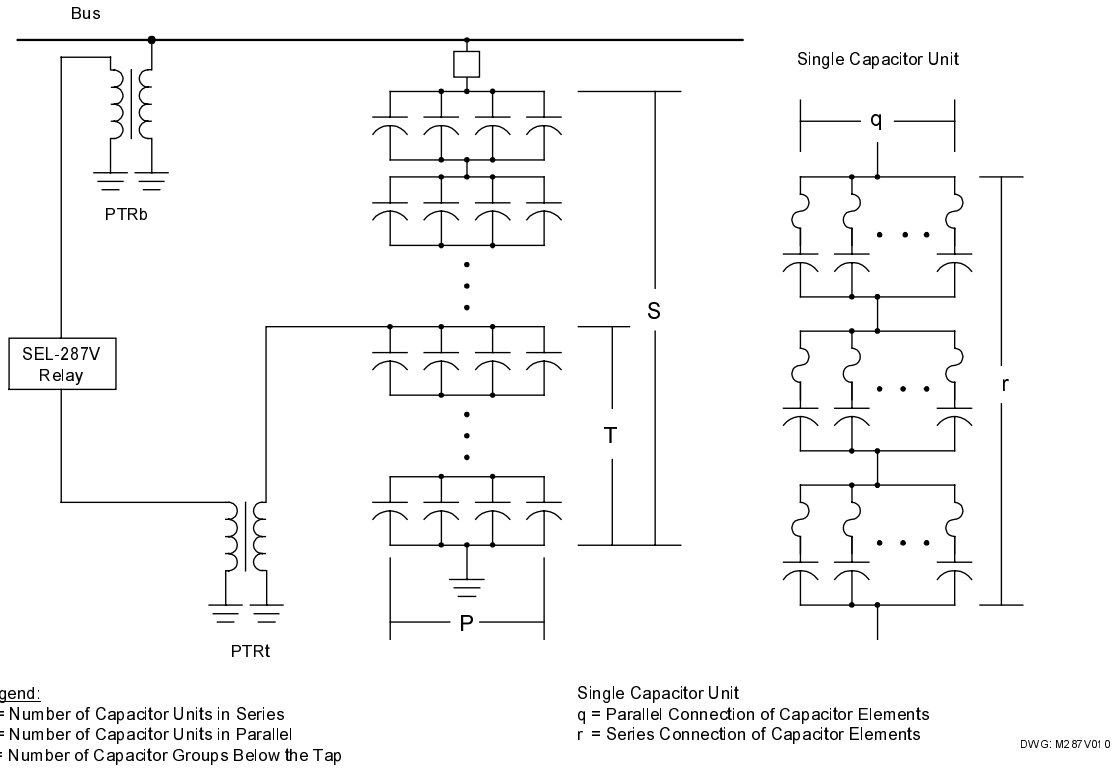



**Figure 5.1: Example Capacitor Bank**

## AC Schematic

Figure 5.1 shows an example capacitor bank. Figure 5.2 shows the SEL-287V Relay Source X inputs connected to the high-voltage bus potential transformers. Tap potential transformers drive the Source Y voltage inputs.

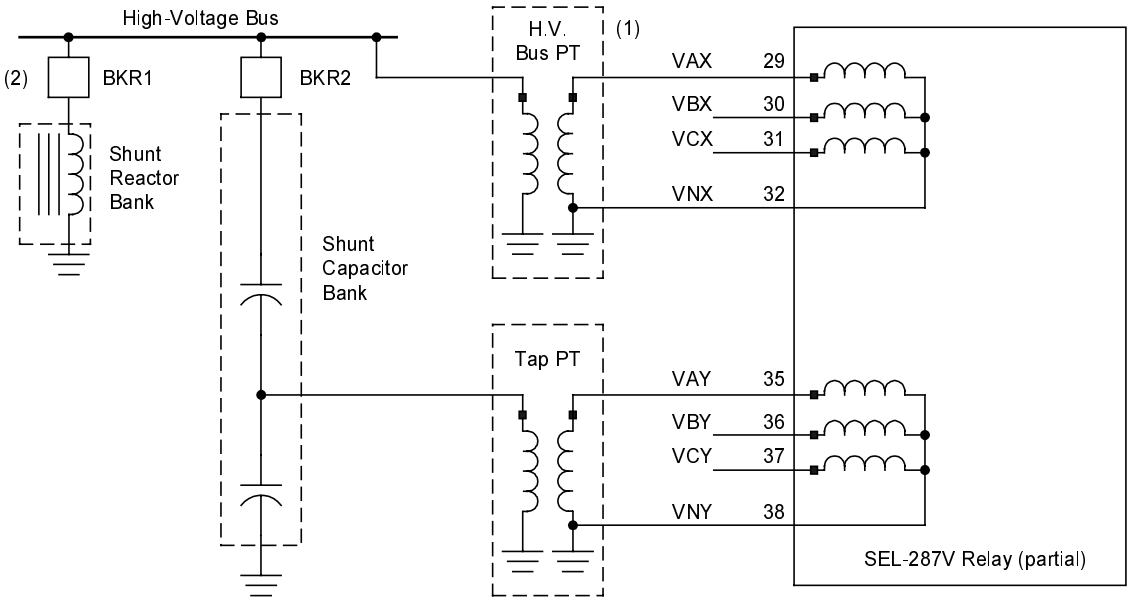



**Figure 5.2: SEL-287V Relay Typical AC Connection Diagram**

The relay protects the shunt capacitor bank by using instantaneous and time-delayed overvoltage elements energized from the bus and tap voltage inputs. The voltage differential elements are set to operate for capacitor bank internal faults.

The voltage control logic outputs insert and remove the capacitor bank at user-settable voltage levels.

## DC Schematic

Figure 5.3 shows typical TRIP and CLOSE circuits. The relay controls capacitor bank insertion and removal with the TRIP and A1 programmable output contacts when the scheme is in automatic mode. If the relay issues a protective trip, the relay A2 contact switches the scheme to manual mode. In manual mode, the relay cannot control the capacitor bank automatically; it cannot reinsert a faulted bank.

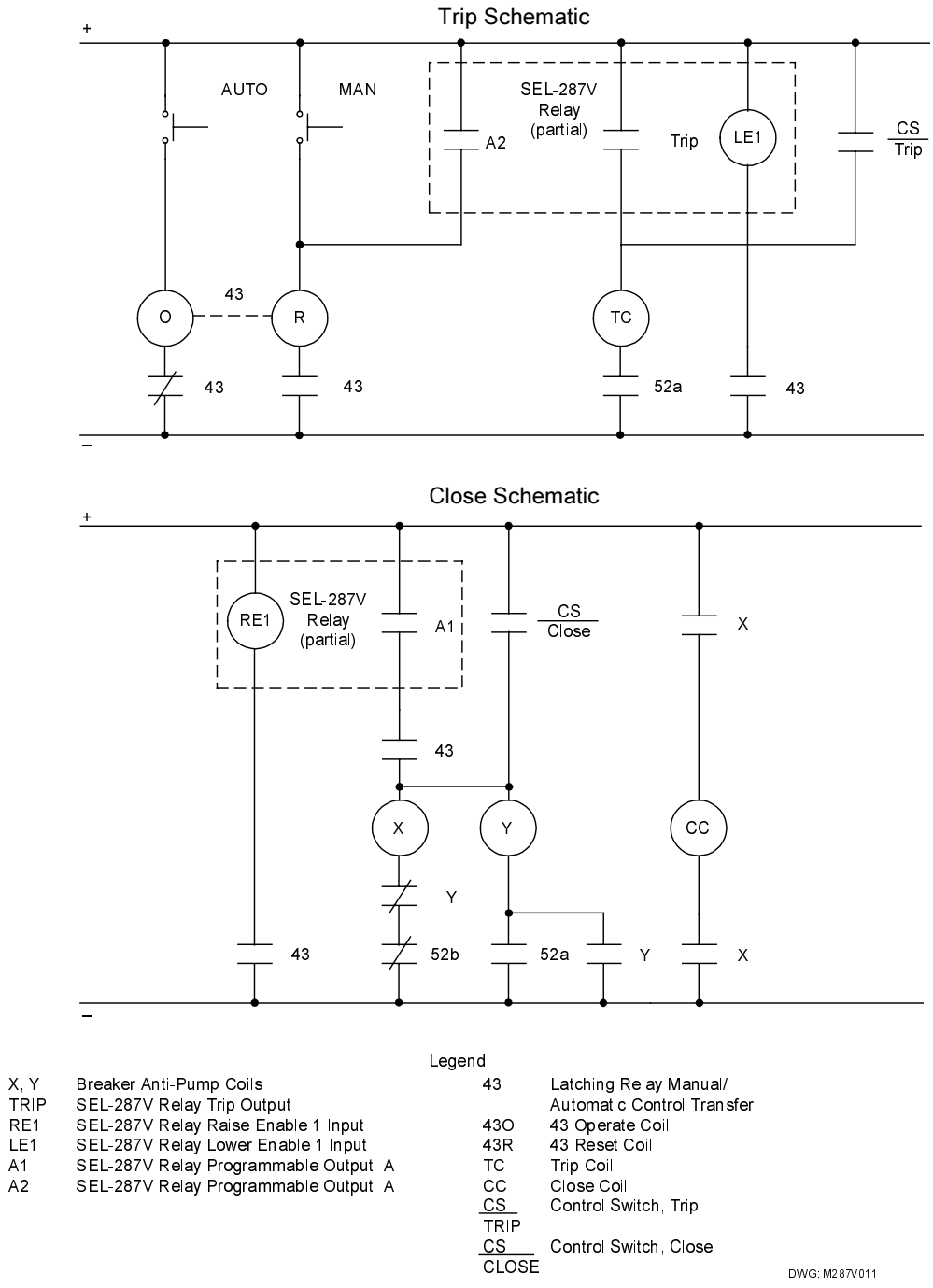



**Figure 5.3: Typical DC Trip and Close Schematics**

Refer to the trip schematic and assume initial conditions with the capacitor bank out of service and the automatic control disabled. Then insert the capacitor bank and enable the automatic control (43). The 43a contacts are closed, asserting the relay LE1 input. When the system voltage rises above the 59P1 setting for THP1 time, Relay Word bit VHD1 asserts. VHD1 is set in the MT logic mask. When VHD1 asserts, the relay closes the TRIP contact, tripping the breaker.

If in the close schematic the automatic control is enabled, the 43a contacts are closed and RE1 is asserted. When the system voltage drops below the 27P1 setting for TLP1 time, Relay Word bit VLD1 asserts. Contact A1 closes, energizing the breaker close coil to return the bank to service.

Capacitor bank protection elements such as the overvoltage and phase differential elements are set in the MA2 programmable logic mask. When any of these elements assert, the TRIP and A2 contacts close. The A2 contact completes the path to assert the 43 reset coil. When 43 resets, it places the TRIP/CLOSE scheme in manual mode. The 43a contacts open, deasserting LE1 and RE1 and isolating A1. With the scheme in manual mode, you can reinsert the bank only with the control switch. Return the scheme to automatic mode with the AUTO pushbutton.

## Example Setting Calculations

The internally fused capacitor bank has many similarities with the externally fused units. The differences include a different criterion for setting the trip and alarm values, and different equations used for fault calculations.

Table 5.2 shows equations applicable for n blown fuses in a row of capacitor elements.

**Table 5.2: General Equations for Internally Fused Grounded-Wye Banks**

| Calculated Quantity | Equation | Number |
|---|---|---|
| Capacitance of healthy unit (pu) | $Cun = \frac{q}{r}$ | Equation 1 |
| Capacitance of unit with n fuses open (pu) | $Cuf(n) = \frac{q-n}{1+\left(1-\frac{n}{q}\right)\bullet(r-1)}$ | Equation 2 |
| Voltage across faulty capacitor unit with n fuses open (pu) | $Vcf(n) = \frac{\frac{P}{S-1}}{\left(\frac{P}{S-1}\right)+(P-1)+\frac{Cuf(n)}{Cun}}\bullet S$ | Equation 3 |
| Voltage across capacitor elements in group with n open fuses (pu) | $Veov(n) = \frac{\frac{q}{r-1}}{(q-n)+\frac{q}{r-1}}\bullet Vcf(n)\bullet r$ | Equation 4 |
| Tap voltage change when n fuses open above tap (pu) | $dVa(n) = \frac{Vcf(n)-1}{S-1}$ | Equation 5 |
| Tap voltage change when n fuses open below tap (pu) | $dVb(n) = (1-Vcf(n))\bullet\frac{S-T}{(S-1)\bullet T}$ | Equation 6 |

### Instantaneous and Definite-Time Overvoltage (59) Elements

Set the instantaneous (59I) and definite-time (59T) overvoltage elements to trip the capacitor bank for system overvoltages that could damage capacitors within the bank. Table 5.3 lists maximum capacitor overvoltage durations per *ANSI/IEEE Std. 18 : 1980, paragraph 8.3.2.1 Momentary Power Frequency Overvoltage*.

**Table 5.3: Maximum Permissible Capacitor Overvoltage Duration**

| Multiplying Factor to be Applied to Rated Voltage RMS | Duration |
|---|---|
| 3.00 | 0.5 cycle |
| 2.70 | 1.0 cycle |
| 2.20 | 6.0 cycle |
| 2.00 | 15.0 cycle |
| 1.70 | 1.0 sec |
| 1.40 | 15.0 sec |
| 1.30 | 1.0 min |
| 1.25 | 30.0 min |

Set the instantaneous overvoltage elements, X59I and Y59I, to pick up at 1.20 per unit of capacitor rated voltage. Set the definite-time, X59T and Y59T, elements to pick up when the capacitor voltage reaches 1.10 per unit of rated voltage.

Use the bus PTs to calculate the capacitor bank rated voltage in bus potential transformer secondary voltage:

$$Vr = \frac{(S \bullet Vcan)}{PTRb} = \frac{(8.0 \bullet 6700)}{800} = 67.0 \text{ V}$$

Set the instantaneous overvoltage element, X59I, to 1.20 per unit on the capacitors:

$$X59I = 1.2 \bullet Vr = 1.2 \bullet 67.0 = 80.4 \text{ V}$$

Set the definite-time overvoltage element, X59PU, to pick up at 1.10 per unit on the capacitors:

$$X59PU = 1.1 \bullet Vr = 1.1 \bullet 67.0 = 73.7 \text{ V}$$

Set time delay X59D to approximately five minutes (18,000 cycles) to prevent nuisance operations resulting from transient overvoltages. This setting is well below the maximum permissible overvoltage duration of 1.20 per unit of capacitor rated voltage.

Consider setting the Y59 elements with the same per-unit overvoltages:

$$Y59I = 1.2 \bullet \frac{(T \bullet Vcan)}{PTRt} = 1.2 \bullet 4 \bullet \frac{6700}{400} = 80.4 \text{ V}$$

$$Y59PU = 1.1 \bullet \frac{\left(T \bullet Vcan\right)}{PTRt} = 1.1 \bullet 4 \bullet \frac{6700}{400} = 73.7\ V$$

### Ratio Adjustment Factors (KA, KB, KC) Elements

The relay calculates the phase magnitude-differential voltage:

$$dV = \left| VX \right| - K \left| VY \right| \text{ per phase.}$$

Assume balanced system conditions (all capacitor fuses intact) to calculate the ratio adjustment factor (K). Under balanced conditions, dV = 0 and you can calculate K from the following equation:

$$K = \left( \frac{PTRt}{PTRb} \right) \bullet \left( \frac{S}{T} \right) = \left( \frac{400}{800} \right) \bullet \left( \frac{8}{4} \right) = 1.000$$

When you install the relay, you can use the KSET and METER commands to make fine adjustments on the ratio adjustment factors.

### High-Set Differential Overvoltage Trip (87H) Elements (SEL-287V Relay)

The 87H elements detect voltage unbalances due to catastrophic failures, such as a whole group arcing over, and trip in the shortest possible time. When a group arcs over low in the bank, the capacitor bank overcurrent protection does not respond fast enough to prevent the fault from increasing in severity (involving more groups) and causing considerable damage. The 87H elements should operate to trip fast enough to reduce the potential damage to the bank from an extended fault.

To set the 87H elements:

A. Determine the per-unit tap voltage change resulting from an entire group arcing over.

B. Calculate the differential element setting in secondary volts.

C. Calculate the element time-delay pickup (87HPD) setting to coordinate with the worst-case fuse clearing time.

For example:

A. Use the following equation to calculate the minimum per-unit change in tap voltage occurring when a group arcs over above the tap:

$$dVt = \frac{F}{\left(S - F\right)} (\text{ pu }) \text{ ; where F is the number of shorted groups}$$

Because the capacitor bank is symmetrical to the tap point (T = 0.5 • S and PTRt = 0.5 • PTRb), faults above and below the tap will result in the same magnitude value of the differential voltage, dV.

For the example capacitor bank with one group shorted:

$$dVt = \frac{1}{(8-1)} = 0.1429 \text{ per-unit change in tap voltage}$$

B. Calculate the differential voltage change and multiply the per-unit change in tap voltage, dVt, by the bus potential transformer secondary voltage at rated capacitor voltage, Vr. Set 87H for approximately 80 percent of this voltage.

$$87H = 0.8 \bullet dVt \bullet Vr = 0.8 \bullet 0.1429 \bullet 67.0 = 7.66 \text{ V}$$

C. Set the 87HPD time delay greater than the worst-case fuse time: 10 cycles in this case.

**Note:** To avoid misoperation of the differential trip elements upon deenergization of the capacitor bank, the pickup time delay should not be set less than two cycles. This is because of the pickup time of the LOP logic in blocking differential element tripping. Typically, this is not a problem because the differential element time delays should be set to coordinate with the worst-case fuse clearing time.

### Differential Overvoltage Trip (87T) Elements (SEL-287V Relay)

The 87T elements detect voltage unbalances resulting from blown capacitor fuses. If an element fails in an internally fused capacitor unit, the fuse will isolate the element. The voltage across the remaining healthy elements in that parallel group increases. The voltage and current distribution on the other capacitor units in the capacitor bank also change. The 87T elements should operate to trip the bank when either:

1. The voltage across the healthy capacitor units reaches 110 percent of the nominal unit value, or
2. The voltage across the capacitor elements in the faulty unit reaches a high level that can involve catastrophic failures such as case rupture.

In a typical application criterion 2 occurs before criterion 1. The voltage value for an overvoltage condition (criterion 2) depends on such factors as: capacitor unit type, age, and external conditions applied to the bank. Newer installations commonly use a value of 1.6–1.8 per unit of nominal capacitor element voltage.

To set the 87T elements:

A. Determine the change in voltages across capacitor elements and units, and in tap voltage when n = 1…q fuses operated within a single group.

B. Select the appropriate number of blown fuses for the trip criterion.

C. Because of the sensitive setting on the 87T element, set the 87T element time-delay pickup (87TPD) long enough to avoid misoperation from system transient conditions.

For example:

A. Use equations in Table 5.2 to calculate the change in voltages across capacitor elements and units, and in tap voltage when n = 1…12 fuses blown within a single group. To calculate the differential element setting, multiply the per-unit change in tap voltage,

dV(n), by the bus potential transformer secondary voltage at rated capacitor voltage, Vr (67 V).

**Table 5.4: Calculation Results for Example Capacitor Bank**

| n | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Veov(n) | 1.0 | 1.066 | 1.141 | 1.227 | 1.327 | 1.445 | 1.587 | 1.759 | 1.973 | 2.246 | 2.606 | 3.105 | 3.84 |
| Vcf(n) | 1.0 | 1.007 | 1.014 | 1.022 | 1.032 | 1.044 | 1.058 | 1.075 | 1.096 | 1.123 | 1.158 | 1.208 | 1.28 |
| dVa(n) [V] | 0 | 0.062 | 0.133 | 0.214 | 0.309 | 0.420 | 0.554 | 0.716 | 0.918 | 1.175 | 1.516 | 1.987 | 2.68 |
| dVb(n) [V] | 0 | 0.062 | 0.133 | 0.214 | 0.309 | 0.420 | 0.554 | 0.716 | 0.918 | 1.175 | 1.516 | 1.987 | 2.68 |

where:

n = number of blown fuses

Veov(n) = voltage across capacitor elements in group with n open fuses (pu)

Vcf(n) = voltage across faulty capacitor unit with n fuses open (pu)

dVa(n) = tap voltage change when n fuses open above tap (pu)

dVb(n) = tap voltage change when n fuses open below tap (pu)

B. Set the voltage differential protection trip value to detect seven open fuses in one row. For this fault the overvoltage of capacitor elements is 176 percent and the overvoltage of the capacitor unit is 108 percent. Because of capacitor bank symmetry, faults above and below the tap point result in the same |dV| value.

87T = 0.716 V

C. Set the 87TPD time delay for one second, or 60 cycles.

### Differential Overvoltage Alarm (87AA, 87BA, 87CA) Elements (SEL-287V Relay)

Because the parallel capacitor elements in the faulty unit can withstand 1.4–1.5 pu for a few months, it would appear satisfactory to alarm the fuse failures at this level of voltage and leave the capacitor bank in service until it is convenient to take it out of service. However, you should inspect the bank without long delay, to avoid possible cascading failures in the faulty unit and unplanned trips. Set the 87A elements to pick up when five fuses operate in one row of elements.

87A = 0.42 V

To avoid nuisance alarms, set the 87AD pickup time delay, 87APD, for one minute, or 3600 cycles.

The relay differential voltage resolution is 0.03 V. To improve security and avoid nuisance operations, do not apply a differential overvoltage setting less than 0.15 V.

## High-Set Differential Overvoltage Trip (87H1P, 87H2P) Elements (SEL-287V-2 Relay)

There are two independent settings for this function: 87H1P and 87H2P. When dV is positive (dV = | VX | –K•|VY|), 87H1P is compared to the dV result. The 87H2P setting is used when dV < 0. Because the capacitor bank in the example is symmetrical about the tap point (T = 0.5 • S and PTRt = 0.5 • PTRb), faults above and below the tap point result in the same magnitude of the differential voltage, dV.

For example:

Use the following example to calculate the minimum per-unit change in tap voltage that occurs when a group arcs over above the tap:

$$dVt = \frac{F}{(S - F)}(\text{pu}) \text{ ; where F is the number of shorted groups}$$

$$dVt = \frac{1}{(8 - 1)} = 0.1429 \text{ per-unit change in tap voltage for F = 1}$$

Calculate the differential voltage change and multiply the per-unit change in tap voltage, dVt, by the bus potential transformer secondary voltage at rated capacitor voltage, Vr. Set 87H1P to approximately 80 percent of this value.

87H1P = 87H2P = 0.8 • dVt • Vr = 0.8 • 0.1429 • 67.0 = 7.66 V

Set the 87HPD time delay greater than the worst-case fuse time, 10 cycles in this case.

**Note :** To avoid misoperation of the differential elements upon deenergization of the capacitor bank, set the 87HPD pickup time delay longer than two cycles. This is because of the pickup time of the LOP logic in blocking the differential trip elements. This is not a problem when the differential element time delay is set to coordinate with the worst-case fuse clearing time.

## Differential Overvoltage Trip (87T1P, 87T2P) Elements (SEL-287V-2 Relay)

Similarly to the high-set differential elements, 87T1P is the valid threshold value if the result of the equation dV = | VX | – K•| VY | is positive, and 87T2P is the valid threshold for negative values of dV.

Set the 87T1P and 87T2P elements in the SEL-287V-2 Relay the same as for the 87T element in the SEL-287V Relay.

Set the voltage differential protection trip value to detect seven open fuses in one row. For this fault the overvoltage of the capacitor elements is 176 percent and the capacitor unit overvoltage is 108 percent. Because of the capacitor bank symmetry, faults above and below the tap point have the same |dV| value:

87T1P = 87T2P = 0.716 V

Set the 87TPD time delay for one second, or 60 cycles.

## Differential Overvoltage Alarm (87A1, 87A2) Elements (SEL-287V-2 Relay)

The SEL-287V-2 Relay does not have separate by-phase alarm threshold settings but has above-tap and below-tap thresholds that apply to all three phases.

Use the same criteria as for the setting of the 87A element in the SEL-287V-2 Relay.

Set the 87A elements to pick up when five fuses operate in one row of elements.

87A1 = 87A2 = 0.42 V

To avoid nuisance alarms, set the 87AD pickup time delay, 87APD, for one minute, or 3600 cycles.

### Loss-of-Potential Dropout Delay (LOPD) Setting

The loss-of-potential dropout delay (LOPD) allows time for the capacitor bank voltages to stabilize before differential overvoltage protection is enabled. The time delay is settable. When selecting the LOPD time delay, consider the following sources of delay:

- Settling time of the capacitor voltage
- Settling time of the tap potential devices

### Voltage Control (59P, 27P) Elements

Use the 27P1 and 27P2 elements to indicate that system voltage is low. Use Relay Word bits VLD1 or VLD2 in any of the programmable output contact logic masks to switch in a capacitor bank, which increases the system voltage.

Set the 59P1 and 59P2 elements to indicate high system voltage. Use Relay Word bits VHD1 or VHD2 in any of the programmable output contact logic masks to switch out a capacitor bank, which reduces the system voltage.

Coordinate 59P1 and 59P2 settings with definite-time and instantaneous overvoltage elements. The 59P1 and 59P2 settings should be lower than the overvoltage element settings. If 59P1 and 59P2 settings are higher than the definite-time overvoltage setting, THP1 and THP2 time delays should be shorter than the definite-time overvoltage element time delay.

Select VLD1 and VLD2 pickup time delays, TLP1 and TLP2, to coordinate with the operating time of the line fault protection equipment on the bus. It is possible that 27P1 or 27P2 could assert during a line or bus fault. The TLP1 and TLP2 delays should allow time for the line protective equipment to operate and clear these faults.

When the nominal secondary voltage of the tap potential transformer differs from the nominal secondary voltage of the bus potential transformer, use a VSS setting of I (Independent) or X (Source X only). With a VSS setting of I or X, the assignment of VX and VY to Voltage Control Scheme 1 and Scheme 2 is fixed. The relay does not change this assignment for changing voltage conditions.

### Voltage Control Instability

The Voltage Control Instability bits, VCI1 and VCI2, indicate when a voltage control raise action causes the system voltage to increase above the voltage control lower (59P) setting.

You may use these indicators to perform one or more functions:

- Operate a programmable output contact
- Trigger event report generation
- Trip the breaker to remove the bank from service and lock out automatic control

Set VCI1 or VCI2 in any of the programmable output contact logic masks. Use the contact to alert the operator to the instability condition. You can also use contact closure to disable the external automatic control scheme.

Set the Voltage Control Instability bits in the MER logic mask for event report triggering. With this setting, when a Voltage Control Instability occurs and no other MER element is asserted, the relay generates an event report.

## Programmable Logic Masks (SEL-287V Relay)

Figure 5.4 shows the programmable logic masks that implement the protection and voltage control functions.

Trip Output
MT Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | Y59A | Y59B | Y59C | |
| | | | | | | | |
| | X59T | | Y59T | | | | |
| | | | | VHD1 | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A1-Raise Voltage Output
MA1 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | VLD1 | | |
| | | | | | | | |
| | | | | | | | |

A2-Reset Automatic Control Output
MA2 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | Y59A | Y59B | Y59C | |
| | | | | | | | |
| | X59T | | Y59T | | | | |
| | | | | | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A5-System Alarm Output
MA5 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | LOPD | VCI1 | VCI2 | | |
| | | | | | | | 87AD |

MER-Event Report Generation
MER Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | Y59A | Y59B | Y59C | |
| | | | | | | | |
| X59P | X59T | Y59T | Y59P | | | | |
| | | | | | | | |
| | 87HD | LOP | | VCI1 | VCI2 | | |
| | | | | | | 87TD | 87AD |

DWG: M287V012

**Figure 5.4: Programmable Logic Mask Settings for the SEL-287V Relay**

### MT Mask Controls the TRIP Output

The MT mask contains the instantaneous overvoltage elements for both Sources X and Y, the definite-time overvoltage elements, X59T and Y59T, the phase differential overvoltage time-delayed trip elements, 87TD and 87HD, and the voltage control lower voltage output, VHD1.

When one of these conditions asserts in the Relay Word, the TRIP output contacts close.

### MA1 Mask Controls the A1 Output, Raises Voltage, Scheme 1

The MA1 mask contains only VLD1. When the VLD1 condition asserts in the Relay Word, it indicates a low system voltage and causes the A1 contact to close.

### MA2 Mask Controls the A2 Output, Resets Automatic Mode

The MA2 mask contains all the elements set in the MT mask except VHD1. When any protective element set in the MA2 programmable logic mask asserts, the A2 contact closes, putting the voltage control scheme in manual mode.

### MA5 Mask Controls the A5 Output, System Alarm Conditions

The MA5 mask contains the time-delayed dropout Loss-of-Potential condition, LOPD, the voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential overvoltage alarm, 87AD. The A5 contact closes when any of these conditions asserts. Monitor this output and use it to alert the operator to unusual system conditions.

### MER Mask Controls Event Report Generation

The MER mask contains all the elements in the MT mask as well as the definite-time overvoltage pickup elements, X59P and Y59P, Loss-of-Potential condition, LOP, voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential overvoltage alarm, 87AD.

The first time an element set in the MER mask asserts, the relay generates an event report. After tripping, it also generates an event report automatically. The MT mask elements have also been asserted in the MER mask as a redundancy. The other elements represent conditions under which event report generation is probably desirable.

## Programmable Logic Masks (SEL-287V-2 Relay)

The Relay Word configuration in the different masks determines different relay outputs. The MT mask determines the trip output, logic masks determine the A1–A5 outputs, and the MER mask determines the entries into the event report. Setting these functions differs between the SEL-287V Relay and the SEL 287V-2 Relay, because row 6 of the Relay Word is different for the two relays (see Table 5.5).

**Table 5.5: Row 6 Relay Word for the SEL-287V and SEL-287V-2 Relays**

| Relay | Relay Word Row 6 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| SEL-287V | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD |
| SEL-287V-2 | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D |

Figure 5.5 shows the programmable logic masks that implement the protection and voltage control functions.

Trip Output
MT Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | Y59A | Y59B | Y59C | |
| | | | | | | | |
| | X59T | | Y59T | | | | |
| | | | | VHD1 | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A1-Raise Voltage Output
MA1 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | VLD1 | | |
| | | | | | | | |
| | | | | | | | |

A2-Reset Automatic Control Output
MA2 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | Y59A | Y59B | Y59C | |
| | | | | | | | |
| | X59T | | Y59T | | | | |
| | | | | | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A5-System Alarm Output
MA5 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | LOPD | VCI1 | VCI2 | | |
| | | | | 87A1D | | | 87A2D |

MER-Event Report Generation
MER Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | Y59A | Y59B | Y59C | |
| | | | | | | | |
| X59P | X59T | Y59T | Y59P | | | | |
| | | | | | | | |
| | 87HD | LOP | | VCI1 | VCI2 | | |
| | | | | 87A1D | | 87TD | 87A2D |

DWG: M287V024

**Figure 5.5: Programmable Logic Mask Settings for the SEL-287V-2 Relay**

## MT Mask Controls the TRIP Output

The MT mask contains the instantaneous overvoltage elements for both Sources X and Y, the definite-time overvoltage elements, X59T and Y59T, the phase differential overvoltage time-delayed trip elements, 87TD and 87HD, and the voltage control lower voltage output, VHD1.

When one of these conditions asserts in the Relay Word, the TRIP output contacts close.

## MA1 Mask Controls the A1 Output, Raises Voltage

The MA1 mask contains only VLD1. When the VLD1 condition asserts in the Relay Word, it indicates a low system voltage and causes the A1 contact to close.

## MA2 Mask Controls the A2 Output, Resets Automatic Mode

The MA2 mask contains all of the elements set in the MT mask except VHD1. When any protective element set in the MA2 programmable logic mask asserts, the A2 contact closes, putting the voltage control scheme in manual mode.

### MA5 Mask Controls the A5 Output, System Alarm Conditions

The MA5 mask contains the time-delayed dropout Loss-of-Potential condition, LOPD, the voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential overvoltage alarms, 87A1D and 87A2D. The A5 contact closes when any of these conditions asserts. Monitor this output and use it to alert the operator to unusual system conditions.

### MER Mask Controls Event Report Generation

The MER mask contains all of the elements in the MT mask as well as the definite-time overvoltage pickup elements, X59P and Y59P, Loss-of-Potential condition, LOP, voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential overvoltage alarms, 87A1D and 87A2D.

### Another Possible Solution for SEL-287V-2 Relay

For the SEL-287V-2 Relay, which has independent settings for faults above and below the tap, the tap potential transformer can be connected to the last row of the capacitor units (T =1). The ratio of the transformer must change according to the changed voltage. For the example in Figure 5.1 all parameters are the same, except for the following:

T = 1 and TPRt = 100/1

The settings for the elements X59I, X27L, X59PU, X59D, VSS, 27P1, 27P2, 59P1, 59P2, THP1, THP2, TLP1, TLP2, THD1, THD2, and the Programmable Logic Mask remain unchanged.

### Ratio Adjustment Factors (KA, KB, KC) Elements

The relay calculates the phase magnitude-differential voltage:

$$dV = \left| VX \right| - K \left| VY \right| \text{ per phase.}$$

Assume balanced system conditions (all capacitor fuses good) in calculating the ratio adjustment factor (K). Under balanced conditions dV = 0, and you can calculate K according to the following:

$$K = \left( \frac{PTRt}{PTRb} \right) \bullet \left( \frac{S}{T} \right) = \left( \frac{100}{800} \right) \bullet \left( \frac{8}{1} \right) = 1.00$$

Use the KSET and METER commands to make fine adjustments on the ratio adjustment factors when you install the relay.

### Instantaneous and Definite-Time Overvoltage (Y59) Elements

Consider setting the Y59 elements with the same per-unit overvoltages you used for the X59 elements:

$$Y\ 59\ I = 1.2 \bullet \left( \frac{T \bullet Vcan}{PTRt} \right) = 1.2 \bullet 1 \bullet \frac{6700}{100} = 80.4\ V$$

$$Y\ 59\ PU = 1.1 \bullet \left( \frac{T \bullet Vcan}{PTRt} \right) = 1.1 \bullet 1 \bullet \frac{6700}{100} = 73.7\ V$$

Y59D = 18000 cycles

## Differential Overvoltage Trip Elements (87)

Use the equations in Table 5.6 to calculate the change in voltages across capacitor elements and units and in tap voltage when n = 1…12 fuses operate within a single group. To calculate the differential element setting, multiply the per-unit change in tap voltage, dV(n), by the bus potential transformer secondary voltage at rated capacitor voltage, Vr (67 V).

**Table 5.6: Calculation Results for the Example Capacitor Bank**

| n | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Veov(n) | 1.0 | 1.066 | 1.141 | 1.227 | 1.327 | 1.445 | 1.587 | 1.759 | 1.973 | 2.246 | 2.606 | 3.105 | 3.84 |
| Vcf(n) | 1.0 | 1.007 | 1.014 | 1.022 | 1.032 | 1.044 | 1.058 | 1.075 | 1.096 | 1.123 | 1.158 | 1.208 | 1.28 |
| dVa(n) [V] | 0 | 0.062 | 0.133 | 0.214 | 0.309 | 0.420 | 0.554 | 0.716 | 0.918 | 1.175 | 1.516 | 1.987 | 2.68 |
| dVb(n) [V] | 0 | 0.434 | 0.929 | 1.498 | 2.161 | 2.942 | 3.876 | 5.012 | 6.425 | 8.228 | 10.61 | 13.91 | 18.76 |

where:

n = number of blown fuses

Veov(n) = voltage across capacitor elements in group with n open fuses (pu)

Vcf(n) = voltage across faulty capacitor unit with n fuses open (pu)

dVa(n) = tap voltage change when n fuses open above tap (pu)

dVb(n) = tap voltage change when n fuses open below tap (pu)

A change of the tap position in the capacitor bank has no effect on the values of Veov(n), Vcf(n), and dVa(n).

A blown fuse in the capacitor unit above the tap will make the dV value positive. A blown fuse in the section below the tap will result in dV < 0. The 87T1P and 87A1P elements are set to detect blown fuses above the tap, while elements 87T2P and 87A2P detect blown fuses below the tap point. Set the alarm level for five blown fuses and a trip for seven blown fuses as follows:

87A1P = 0.42 V

87A2P = 2.942 V

87APD = 3600 cyc

87T1P = 0.716 V

87T2P = 5.012 V

87TPD = 60 cyc

The 87H elements detect voltage unbalances resulting from a whole group arcing over. This type of fault above the tap increases the tap voltage and results in a negative value for the differential voltage. The 87H2P element is set to detect this failure. A flashover in the last row of capacitor units shorts out the tap PT, making the Source Y voltage equal zero:

87H1P = 0.8 • Vr = 0.8 • 67 = 53.6 V

87H2P = 7.66 V

87HPD = 10 cyc

## EXTERNALLY FUSED GROUNDED-WYE CAPACITOR BANK EXAMPLE

The enhanced version SEL-287V-2 Relay differs from the standard SEL-287V Relay in that it provides separate threshold settings for voltage differential functions. These settings depend on the sign of the dV value. The SEL-287V-2 Relay also does not have separate per-phase alarm threshold settings, allowing for a tap voltage connection to a much lower voltage point on the capacitor bank than does the more conventional center point connection. Potential transformers used in this application can have much lower ratings, offering a substantial cost saving.

The following elements are common to both relays: instantaneous and definite-time overvoltage (59), loss-of-potential logic, and voltage control (59P, 27P). Voltage control is identical in both versions. In balanced system conditions, the relay calculates the ratio adjustment factors (KA, KB, KC) according to the PT ratios.

All applications that use SEL-287V or SEL-287V-2 Relays provide trip and close control of the capacitor bank breaker, similarly to the method that Figure 5.3 illustrates. Separate control and protection functions settings ensure the integrity of both control and protection systems.

Consider application of the SEL-287V-2 to the example that Figure 5.1 (disregard the single capacitor unit sketch) and Figure 5.2 illustrate.

The data for this bank are shown in Table 5.7. Equations used to calculate this bank are shown in Table 5.8.

**Table 5.7: Example Externally Fused Capacitor Bank Data**

| Item | Description |
|---|---|
| Capacitor Bank Configuration | Shunt, Grounded-Wye |
| Series groups per phase, S | 17 |
| Capacitors per group, P | 16 |
| Capacitor Unit | |
| Type | Externally Fused |
| Capacitor Rated Voltage, Vcan | 7960 V |

| Item | Description |
|---|---|
| Nominal Bus Voltage, Vbus | 230 kV |
| Bus Potential Transformer Ratio, PTRb | 2000 : 1 |
| Tap Potential Transformer Ratio, PTRt | 1000 : 1 |
| Capacitor Groups Below the Tap, T | 8 |
| Voltage Control Lower, 107% | 246 kV |
| Voltage Control Raise, 97.8% | 225 kV |

**Table 5.8: General Equations for Externally Fused Grounded-Wye Banks**

| Calculated Quantity | Equation | Number |
|---|---|---|
| Tap voltage change (pu) for 10% group overvoltage above tap | $dV10 = \frac{0.1}{S-1}$ | Equation 1 |
| Tap voltage change (pu) for 10% group overvoltage below tap | $dVT10 = \frac{0.1 \bullet \left(\frac{S}{T} - 1\right)}{S-1}$ | Equation 2 |
| Fuse operations (n) necessary to cause a 10% group overvoltage | $n = \frac{S \bullet P}{11 \bullet (S-1)}$ | Equation 3 |
| Tap voltage change (pu) when n fuses open in one group above tap | $dV(n) = \frac{n}{S \bullet (P-n) + n}$ | Equation 4 |
| Tap voltage change (pu) when n fuses open in one group below tap | $dVT(n) = \frac{n \bullet \left(\frac{S}{T} - 1\right)}{S \bullet (P-n) + n}$ | Equation 5 |
| Voltage (pu) across capacitors in group with n open fuses | $Vc(n) = \frac{S \bullet P}{S \bullet (P-n) + n}$ | Equation 6 |

Use the sign of the differential voltage elements to determine the location of a blown fuse. In our example, a blown fuse above the tap point isolates the faulty capacitor unit. This results in decreased Source Y voltage, i.e., in the KA•|VAY| term of the differential equation (dV = |VAX| – KA• |VAY|). Because the VAX element connects to the reference voltage, and remains unaffected by fuses blowing in the capacitor bank, the differential equation, dV = |VAX| – K|VAY|, yields a positive sign. Conversely, a negative value of dV indicates a blown fuse below the tap point.

In the case of a capacitor unit flashover, in which a complete series group shorts out, the result is the opposite–a fault above the tap point increases the Source Y voltage and dV is negative. For a flashover below the tap point, the differential voltage is positive.

**Table 5.9: Summary of dV Sign According to Fault Type and Position**

| Fault Type | Fault Position | dV Sign |
|---|---|---|
| Blown fuse | Above tap point | Positive |
| Blown fuse | Below tap point | Negative |
| Flashover | Above tap point | Negative |
| Flashover | Below tap point | Positive |

Consider the above when calculating the threshold values for the differential voltage alarm, trip, and high-set trip elements, as this manual describes in the setting calculation for the SEL-287V Relay.

## High-Set Differential Overvoltage Trip (87H1P, 87H2P) Elements (SEL-287V-2 Relay)

This function has two separate settings, one for a positive differential voltage and one for a negative value. Setting 87H1P is effective when the differential voltage, dV, is positive, and 87H2P is effective when dV is negative. Use these elements for high-speed tripping in the case of catastrophic failures such as a flashover on a whole group.

When a flashover occurs in a capacitor group above the tap, the voltage measured at the tap PT (dVt) changes as follows:

$$dVt = \frac{1}{(S-1)} = \frac{1}{(17-1)} = 0.0625 \text{ per unit}$$

To ensure operation for this fault, set the 87H2P element at 80 percent of this value:

$$87H2P = 0.8 \bullet 0.0625 \bullet 67.66 = 3.38 \text{ V}$$

Should the same type of fault occur below the tap point, calculate dVt as follows:

$$dVt = \frac{(T-S)}{T \bullet (S-1)} = 0.0703 \text{ per unit}$$

And the setting for 87H1P, with 20 percent adjustment, is as follows:

$$87H1P = 0.8 \bullet 0.0703 \bullet 67.66 = 3.81 \text{ V}$$

The 87HPD timer delay is common to both elements. For proper grading, set 87HPD longer than the operating time of the slowest blowing fuse.

## Differential Overvoltage Trip (87T1P, 87T2P) Elements (SEL-287V-2 Relay)

Set the 87T setting according to the maximum overvoltage stress that the capacitor units can withstand continuously, typically about 110 percent of the rated voltage. Similarly to the high-set differential elements, 87T1P is the valid threshold setting when dV is positive, and 87T2P is the active setting when dV is negative.

The setting for the 87T1P element is equal to the tap voltage change that results from the 110 percent overvoltage in one of the groups above the tap. Use Equation 1 from Table 5.8 to obtain the following:

$$dV(10\%) = \frac{0.1}{(S-1)} = \frac{0.1}{(17-1)} = 0.00625 \text{ per unit}$$

When set to 80 percent the setting yields the following:

87T1P = 0.8 • 0.00625 • 67.66 = 0.34 V

Use Equation 2 from Table 5.8 when the fault is below the tap for a 110 percent overvoltage condition:

$$dVt10 = 0.1 \bullet \frac{\left(\frac{S}{T-1}\right)}{(s-1)} = 0.1 \bullet \frac{\left(\frac{17}{8-1}\right)}{(17-1)} = 0.007 \text{ per unit}$$

87T2P = 0.8 • 0.007 • 67.66 = 0.38 V

Set the 87TPD time delay for one second, or 60 cycles.

## Differential Overvoltage Alarm (87A1, 87A2) Elements (SEL-287V Relay)

Set the 87A element to pick up when one capacitor fuse in a series group blows. Set n equal to 1 and use Equations 3, 4, and 5 from Table 5.8 to calculate the per-unit change in the tap voltage for a single fuse operation in a single group above and below the tap point.

For the example capacitor bank with n equal to 1:

dV(n) = 0.00391 pu, above the tap

dVT(n) = 0.00439 pu, below the tap

To ensure that the 87A element picks up for a single fuse operation, set the element at 0.80 times the lowest differential voltage resulting from a single fuse operation. Use the following equations to calculate the differential alarm settings:

87A1 = 0.8 • dV(n) • Vr = 0.8 • 0.00391 • 67.66 = 0.21 V

87A2 = 0.8 • dVT(n) • Vr = 0.8 • 0.00439 • 67.66 = 0.24 V

The relay differential voltage resolution is 0.03 V. To improve security and avoid nuisance operations, do not apply a differential overvoltage setting below 0.15V.

Table 5.10 and Table 5.11 correlate the number of blown fuses in a row with the resulting voltage changes for faults above and below the tap point.

**Table 5.10: Fault Above Tap Point**

| n | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Vc(n) | 1.063 | 1.133 | 1.214 | 1.308 |
| dV (per unit) | 0.0039 | 0.0083 | 0.013 | 0.019 |
| dV (V) | 0.26 | 0.56 | 0.91 | 1.30 |

**Table 5.11: Fault Below Tap Point**

| n | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Vc(n) | 1.063 | 1.133 | 1.214 | 1.308 |
| dV (per unit) | 0.0044 | 0.0094 | 0.015 | 0.022 |
| dV (V) | 0.30 | 0.63 | 1.02 | 1.46 |

n = number of blown fuses in one row

Vc(n) = voltage across capacitors in group with n faulty fuses

dV = tap voltage change

## Programmable Logic Masks

We have three types of masks:

- MT (tripping mask) declares the trip output functions
- Masks MA1–MA5 (alarm masks) configure the remaining outputs
- Mask MER (event report mask) event report function is based on the Relay Word configuration. Because the SEL-287V and SEL 287V-2 Relays have different Relay Words in row 6–see Table 5.12, the relay settings will differ for this mask.

**Table 5.12: Row 6 of Relay Word for the SEL-287V and SEL-287V-2 Relays**

| Relay | Relay Word Row 6 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| SEL-287V | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD |
| SEL-287V-2 | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D |

Figure 5.6 shows the programmable logic masks, which implement the protection and voltage control functions.

Trip Output
MT Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | Y59A | Y59B | Y59C | |
| | | | | | | | |
| | X59T | | Y59T | | | | |
| | | | | VHD1 | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A1-Raise Voltage Output
MA1 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | VLD1 | | |
| | | | | | | | |
| | | | | | | | |

A2-Reset Automatic Control Output
MA2 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | Y59A | Y59B | Y59C | |
| | | | | | | | |
| | X59T | | Y59T | | | | |
| | | | | | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A5-System Alarm Output
MA5 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | LOPD | VCI1 | VCI2 | | |
| | | | | 87A1D | | | 87A2D |

MER-Event Report Generation
MER Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | Y59A | Y59B | Y59C | |
| | | | | | | | |
| X59P | X59T | Y59T | Y59P | | | | |
| | | | | | | | |
| | 87HD | LOP | | VCI1 | VCI2 | | |
| | | | | 87A1D | | 87TD | 87A2D |

DWG: M287V024

**Figure 5.6: Programmable Logic Mask Settings–SEL-287V-2**

## MT Mask Controls the TRIP Output

The MT mask contains the instantaneous overvoltage elements for both Sources X and Y, the definite-time overvoltage elements, X59T and Y59T, the phase differential overvoltage time-delayed trip elements, 87TD and 87HD, and the voltage control lower voltage output, VHD1.

When one of these Relay Words assert, the TRIP output contacts close.

## MA1 Mask Controls the A1 Output, Raises Voltage

The MA1 mask contains only VLD1. Assertion of the VLD1 condition in the Relay Word indicates a low system voltage, which causes the A1 contact to close.

## MA2 Mask Controls the A2 Output, Resets Automatic Mode

The MA2 mask contains all of the elements set in the MT mask except VHD1. When any protective element set in the MA2 programmable logic mask asserts, the A2 contact closes, putting the voltage control scheme into manual mode.

### MA5 Mask Controls the A5 Output, System Alarm Conditions

The MA5 mask contains the time-delayed dropout loss-of-potential condition, LOPD, the voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential overvoltage alarms, 87A1D and 87A2D. The A5 contact closes when any of these conditions assert. Monitor this output for any unusual system conditions.

### MER Mask Controls Event Report Generation

The MER mask contains all of the elements in the MT mask, as well as the definite-time overvoltage pickup elements, X59P and Y59P, loss-of-potential condition, LOP, voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential overvoltage alarms, 87A1D and 87A2D.

## FUSELESS, SINGLE-GROUNDED WYE-CONNECTED CAPACITOR BANK EXAMPLE

This section provides example settings and calculations to protect and control the capacitor bank described in Table 5.13.

**Table 5.13: Example Capacitor Bank**

| Item | Description |
|---|---|
| Capacitor Bank Configuration | Shunt, Grounded-Wye |
| Series groups per phase, L | 6 |
| Series capacitors per string, S | 24 |
| Capacitor Unit | |
| Type | Fuseless |
| Series capacitor elements, r | 4 |
| Parallel capacitor elements, q | 3 |
| Reactive power rating, Q | 420 kVar |
| Capacitor rated voltage, Vcan | 7280 V |
| Unit capacitance, Cu | 25.24 μF |
| Low Voltage Capacitors | |
| Number of units | 4 |
| Reactive power rating, Q | 167 kVAr |
| Capacitor rated voltage, Vcan | 825 V |
| Unit capacitance, C | 781 μF |
| Nominal Bus Voltage, Vbus | 275 kV |

| Item | Description |
|---|---|
| Nominal System Frequency, Nfreq | 50 Hz |
| Bus Potential Transformer Ratio, PTRb | 2500 |
| Tap Potential Transformer Ratio, PTRt | 3.2 |

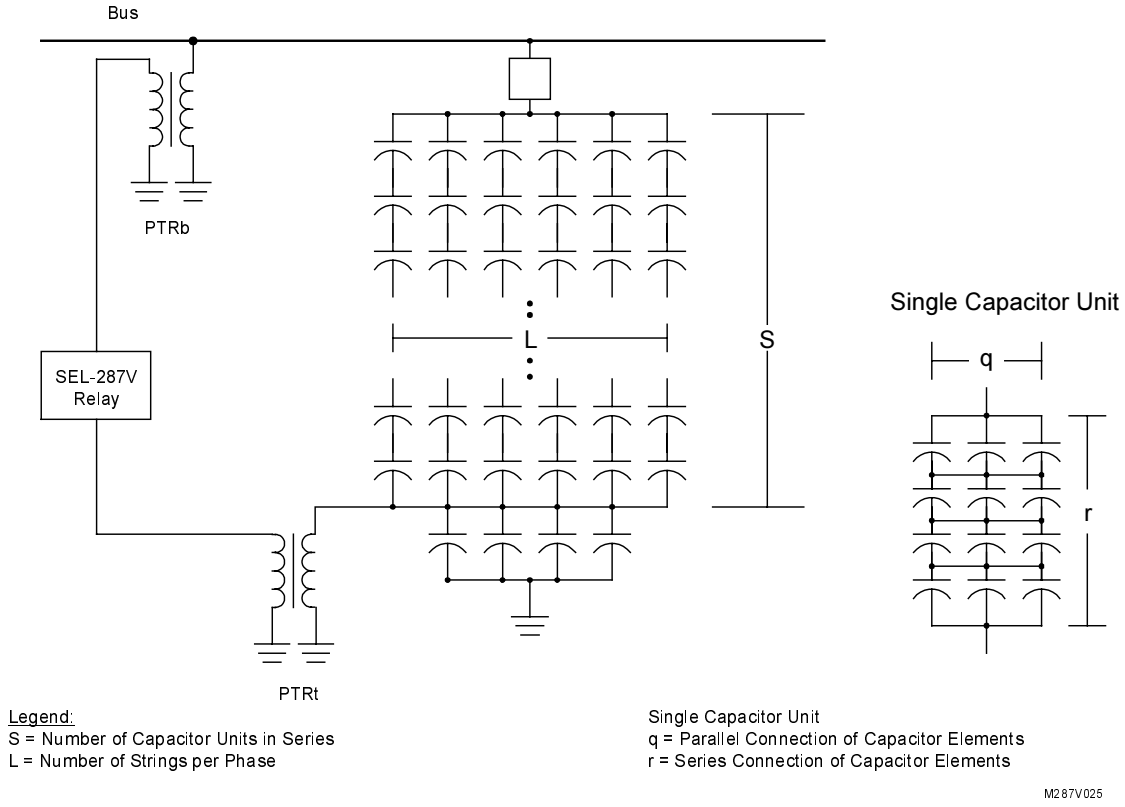



**Figure 5.7: Example Capacitor Bank**

## AC Schematic

Figure 5.8 shows an example capacitor bank. Figure 5.8 shows the SEL-287V Relay Source X inputs connected to high-voltage bus potential transformers. Low-voltage potential transformers drive the Source Y voltage inputs.

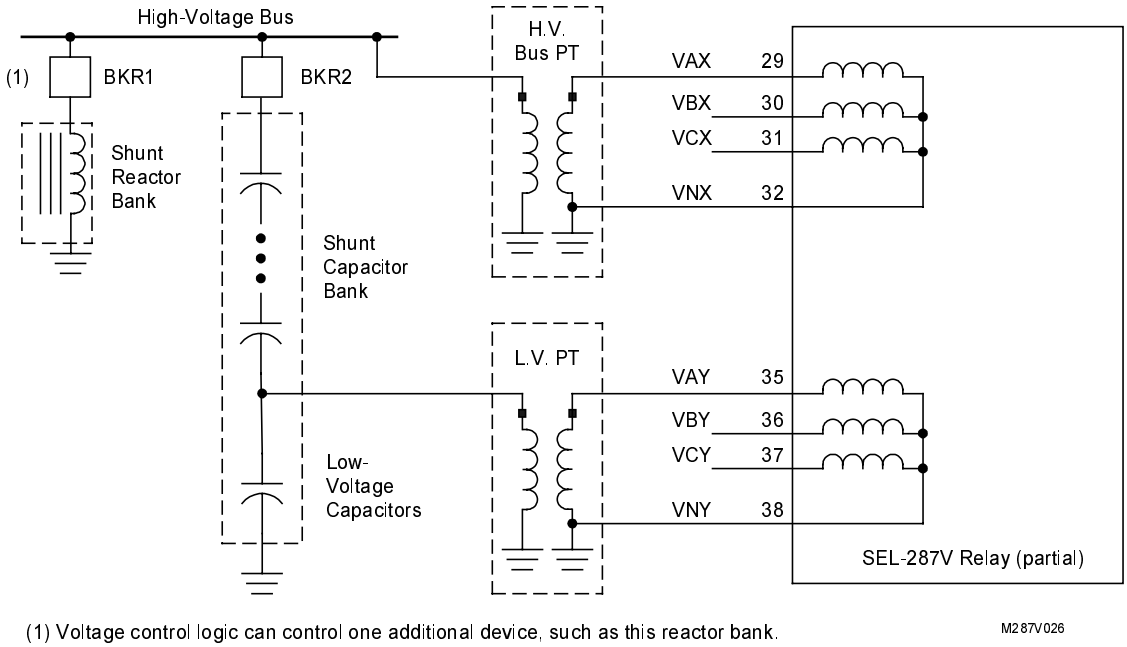



**Figure 5.8: SEL-287V Relay AC Connection Diagram**

The relay uses instantaneous and time-delayed overvoltage elements taken from the bus and tap voltage inputs to protect the shunt capacitor bank for system overvoltage conditions. Use the voltage differential elements to protect the capacitor bank for internal faults.

The voltage control logic outputs insert and remove the capacitor bank at user-settable voltage levels.

## DC Schematic

Figure 5.9 shows typical TRIP and CLOSE circuits. The relay controls capacitor bank insertion and removal with the TRIP and A1 programmable output contacts when the scheme is in automatic mode. If the relay issues a protective trip, the relay A2 contact switches the scheme to manual mode. In manual mode the relay cannot control the capacitor bank automatically; it cannot reinsert a faulted bank.

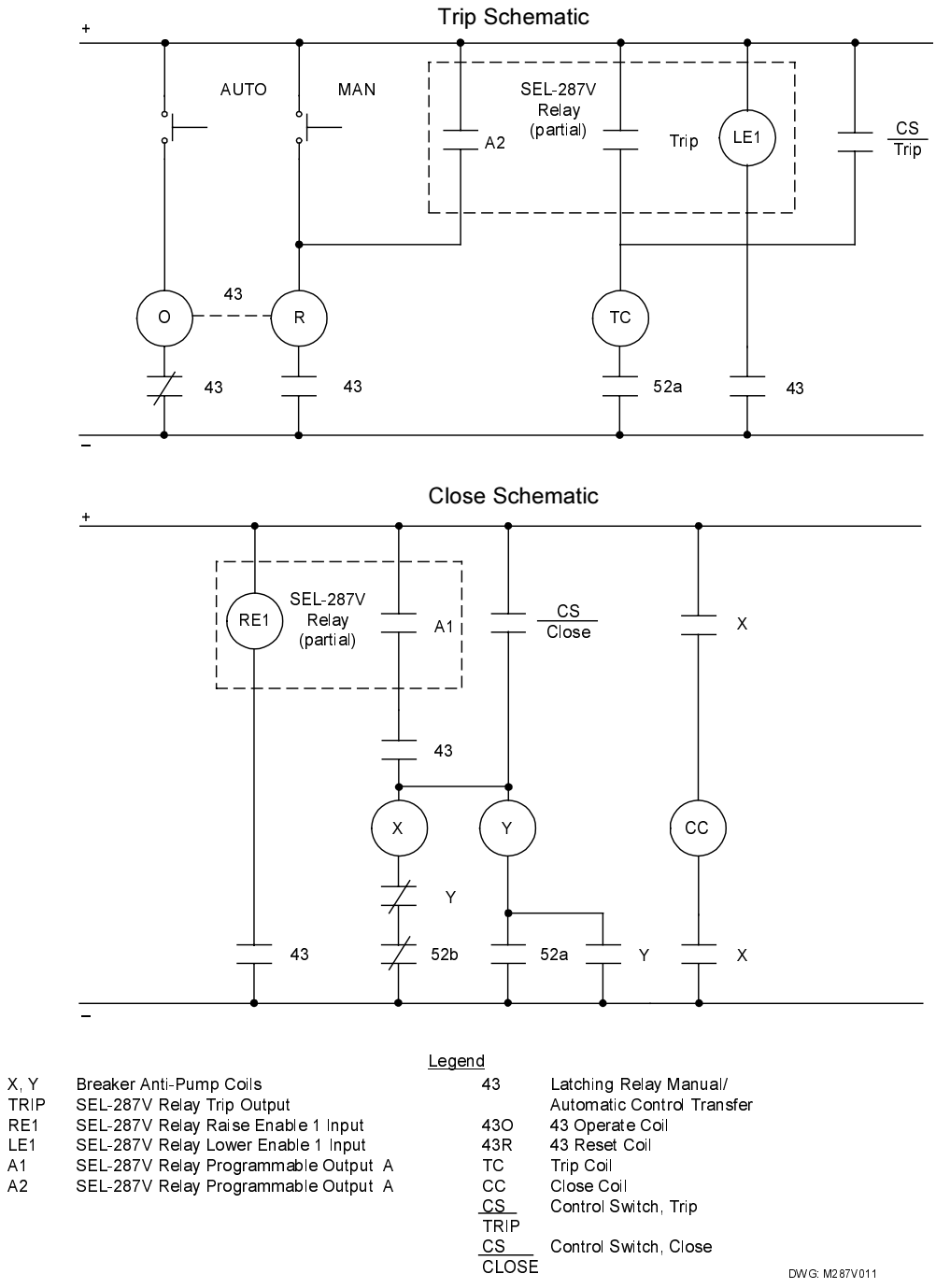



**Figure 5.9: Typical DC Trip and Close Schematics**

Refer to the trip schematic and assume initial conditions with the capacitor bank out of service and the automatic control disabled. Then insert the capacitor bank and enable the automatic control (43). The 43a contacts are closed, asserting the relay LE1 input. When the system voltage rises above the 59P1 setting for THP1 time, Relay Word bit VHD1 asserts. VHD1 is set in the MT logic mask. When VHD1 asserts, the relay closes the TRIP contact, tripping the breaker.

If in the close schematic the automatic control is enabled, the 43a contacts are closed and RE1 is asserted. When the system voltage drops below the 27P1 setting for TLP1 time, Relay Word bit VLD1 asserts. Contact A1 closes, energizing the breaker close coil to return the bank to service.

Capacitor bank protection elements such as the overvoltage and phase differential elements are set in the MA2 programmable logic mask. When any of these elements assert, the TRIP and A2 contacts close. The A2 contact completes the path to assert the 43 reset coil. When 43 resets, it places the TRIP/CLOSE scheme in manual mode. The 43a contacts open, deasserting LE1 and RE1 and isolating A1. With the scheme in manual mode, you can reinsert the bank only with the control switch. Return the scheme to automatic mode with the AUTO pushbutton.

## Example Setting Calculations

For the nominal bus voltage (275 kV) each capacitor unit in the strings is exposed to $275/\sqrt{3} \bullet 24 = 6.62$ kV voltage (disregard the low-voltage capacitors for this calculation, because the value is usually so low that it has no effect on the calculated values). The overrating factor (nominal voltage of the capacitor unit to voltage applied on the unit with nominal bus voltage) is equal to $7280/6620 = 1.1$.

### Instantaneous and Definite-Time Overvoltage (59) Elements

Set the instantaneous (59I) and definite-time (59T) overvoltage elements to trip the capacitor bank out of service for system overvoltage that could damage capacitors within the bank.

Calculate the capacitor bank rated secondary voltage from the bus PT, using the following equation:

$$Vr = \frac{(S \bullet Vcan)}{PTRb} = \frac{(24 \bullet 7280)}{2500} = 69.9 \text{ V}$$

Set the instantaneous overvoltage element, X59I, to 1.20 per unit on the capacitors:

$$X\,59I = 1.2 \bullet Vr = 1.2 \bullet 69.9 = 83.8 \text{ V}$$

Set the definite-time overvoltage element, X59PU, to pick up at 1.10 per unit on the capacitors:

$$X59PU = 1.1 \bullet Vr = 1.1 \bullet 69.9 = 76.9 \text{ V}$$

Time delay the X59D element by approximately five minutes (18,000 cycles) to prevent nuisance operations resulting from transient overvoltages. This setting is well below the maximum permissible overvoltage duration of 1.20 per unit of capacitor rated voltage.

Use the Y59 elements to protect the low-voltage capacitors from overvoltages.

Calculate the primary tap voltage under bus rated voltage:

$$Vt = Vph \bullet Dn = 158771 \bullet 0.002 = 320 \text{ V}$$

where:

Dn = voltage divider factor for balance system,

$$Dn = \frac{Cb}{(Cb + Cl)} = \frac{6.31}{(6.31 + 3124)} = 0.002$$

Cb = capacitance of the one phase, $Cb = Cu \bullet \frac{L}{S} = 25.24 \bullet \frac{6}{24} = 6.31\,\mu F$

Vph = phase nominal voltage, $Vph = \frac{275000}{1.73} = 158771\,V$

Cl = low-voltage capacitor

The secondary tap voltage becomes the following:

$$VY = \frac{Vt}{PTR\,1} = \frac{320}{3.2} = 100\,V$$

Because the rated voltage for low-voltage capacitors is 825 V (825/320) = 2.58 times "working" voltage, there is no need to apply the Y59 elements.

### Ratio Adjustment Factors (KA, KB, KC) Elements

The relay calculates the phase magnitude-differential voltage:

$$dV = \left| VX \right| - K \left| VY \right| \text{ per phase}$$

Assume balanced system conditions and no fault on the capacitor bank in calculating the ratio adjustment factor (K). Under balanced conditions, dV = 0 and you can calculate K according to the following:

$$K = \frac{PTR\,1}{(PTRb \bullet Dn)} = \frac{3.2}{(2500 \bullet 0.002)} = 0.635$$

When you install the relay, use the KSET and METER commands to make fine adjustments on the ratio adjustment factors.

### Loss-of-Potential Dropout Delay (LOPD) Setting

The loss-of-potential dropout delay (LOPD) allows time for the capacitor bank voltages to stabilize before differential overvoltage protection is enabled. The time delay is settable. When selecting the LOPD time delay, consider the following sources of delay:

- Settling time of the capacitor voltage
- Settling time of the tap potential devices

### Voltage Control (59P, 27P) Elements

Use the 27P1 and 27P2 elements to indicate that system voltage is low. Use Relay Word bits VLD1 or VLD2 in any of the programmable output contact logic masks to switch in a capacitor bank, which increases the system voltage. The example capacitor bank 27P1 setting is 64.95 V.

Set the 59P1 and 59P2 elements to indicate that the system voltage is high. Use Relay Word bits VHD1 or VHD2 in any of the programmable output contact logic masks to switch out a capacitor bank, which reduces the system voltage. The example capacitor bank 59P1 setting is 71.01 V.

Coordinate your 59P1 and 59P2 settings with definite-time and instantaneous overvoltage elements. The 59P1 and 59P2 settings should be lower than overvoltage element settings. If 59P1 and 59P2 settings are higher than the definite-time overvoltage setting, THP1 and THP2 time delays should be shorter than the definite-time overvoltage element time delay.

Select VLD1 and VLD2 pickup time delays TLP1 and TLP2 to coordinate with the operating time of the line fault protection equipment on the bus. It is possible that 27P1 or 27P2 could assert during a line or bus fault. The TLP1 and TLP2 delays should allow time for the line protective equipment to operate and clear these faults.

When the nominal secondary voltage of the tap potential transformer differs from the nominal secondary voltage of the bus potential transformer, use a VSS setting of I (Independent) or X (Source X only). With a VSS setting of I or X, the assignment of VX and VY to Voltage Control Scheme 1 and Scheme 2 is fixed. The relay does not change this assignment for changing voltage conditions.

### Voltage Control Instability

These elements are independent of the type of capacitor bank. Setting these elements is the same for the SEL-287V and SEL-287V-2 Relays. Refer to the previous example for more information. Calculate the settings for the 59P and 27P elements as follows:

X27A = X27B = X27C = 32 V

Y27A = Y27B = Y27C = 27 V

VSS = X

27P1 = 60 V

59P1 = 76 V

### Calculations for Voltage Differential Protection

Figure 5.7 shows a fuseless capacitor bank with six strings per phase, each string consisting of 24 capacitor units connected in series. The single capacitor unit has four parallel groups (three capacitor elements in parallel) connected in series (see Figure 5.7). The string consists of 24 • 4 = 96 capacitor parallel groups connected in series. Failure of one capacitor element will short out an entire parallel group and increase the voltage on all remaining capacitors in the string by the same value.

Assume that all of the shorted capacitors are in the same string, and use the following formula to calculate the voltage differential for a fault in the capacitor bank:

$$dV = \left| VX \right| \bullet \frac{\left( Dn - Df \right)}{Dn} \quad \text{(Volt)}$$

Dn = voltage divider factor for balance system,

$$Dn = \frac{Cb}{\left( Cb + C1 \right)} = \frac{6.31}{\left( 6.31 + 3124 \right)} = 0.002$$

Df = voltage divider factor with the fault in the capacitor bank, $Df = \frac{Cf}{(Cf + Cl)}$

Cf = capacitance of the faulty phase of the capacitor bank,
$Cf = \frac{(Cu \bullet r)}{(r \bullet S - n)} + \frac{(Cu \bullet (L - 1))}{S}$

Cb = capacitance of the one phase, $Cb = 25.24 \bullet \frac{6}{24} = 6.31\,\mu F$

Cl = low-voltage capacitor

Cu, S, L= as per Table 5.12

n = number of faulty (shorted) parallel capacitor group in one string

Differential voltage, dV, is proportional to the bus secondary voltage, VX, and the number of faulty parallel capacitor groups, n. Increase the VX value to where the minimum setting of the voltage differential protection elements is less than the smallest recommended setting (0.15V), usually with large capacitor banks. Do this by using a bus potential transformer with a smaller ratio or by interposing an additional transformer. Calculate a new value for the correction factor, K, in this case.

Calculate the increase in the voltage rise on the remaining healthy capacitors in the string with n-shorted parallel group as follows:

$$Vc(n) = r \bullet \frac{S}{(r \bullet S - n)} = \frac{96}{(96 - n)} \quad (pu)$$

You can omit the low-voltage capacitors for this calculation.

Table 5.14 shows the results of the calculations with different values for n.

**Table 5.14: Vc(n) and dV for Varying Number of Faults in One String**

| n | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 12 | 15 | 20 | 30 | 32 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Vc(n) | 1.01 | 1.02 | 1.03 | 1.04 | 1.06 | 1.07 | 1.08 | 1.09 | 1.10 | 1.12 | 1.14 | 1.19 | 1.26 | 1.46 | 1.5 |
| dV(1) | 0.11 | 0.23 | 0.34 | 0.46 | 0.58 | 0.70 | 0.83 | 0.96 | 1.09 | 1.23 | 1.51 | 1.96 | 2.78 | 4.8 | 5.28 |
| dV(2) | 0.12 | 0.25 | 0.38 | 0.51 | 0.64 | 0.78 | 0.91 | 1.06 | 1.20 | 1.35 | 1.66 | 2.15 | 3.06 | 5.28 | 5.81 |

n = number of faulty parallel capacitor groups in one string

dV(1) = phase magnitude-differential voltage calculated at nominal bus voltage, 275 kV

dV(2) = phase magnitude-differential voltage calculated at rated capacitor voltage (bus voltage = 24 • 7280 • 1.73 = 302 kV)

### High-Set Differential Overvoltage Trip (87H) Elements (SEL-287V Relay)

The 87H elements detect voltage unbalances due to catastrophic failures, such as a whole group arcing over, and trip in the shortest possible time. When a group arcs over low in the bank, the capacitor bank overcurrent protection does not respond fast enough to prevent the fault from increasing in severity (involving more groups) and causing considerable damage. The 87H elements should operate to trip fast enough to reduce the potential damage to the bank from an extended fault.

In the example the capacitor bank consists of three frames (stacking assemblies), each of which supports eight capacitor units. Set the 87H element to detect the flashover of eight capacitor units. A flashover increases the voltage on the healthy capacitors in the string to 150 percent of the prefault value. The maximum permissible capacitor duration for 150 percent overvoltage is about eight seconds (see Table 5.3). For the fault involving 32 groups and at rated capacitor voltage, the differential value is 5.81 V. Set 87H to 80 percent of this voltage:

$$87H = 0.8 \bullet 5.81 = 4.65 \text{ V}$$

Set the 87HPD time delay to allow for the LOPD element to pick up for a manual opening of the circuit breaker. This delay is typically five cycles.

### Differential Overvoltage Trip (87T) Elements (SEL-287V Relay)

The 87T elements detect voltage unbalances resulting from short circuits in the capacitor elements. The voltage on the remaining capacitors in the string now uniformly increases to a much greater value. The 87T elements should trip the bank before an overvoltage stress occurs on the remaining capacitors. Use the maximum overvoltage withstand rating of the capacitors (typically 110 percent) as the limit when setting the element. In the example we set the 87T threshold to detect the shorting out of nine parallel capacitor groups. Such a short increases the voltage on the healthy capacitors to the maximum permissible value (see Table 5.12) at capacitor rated voltage.

$$87T = 1.20 \text{ V}$$

Set the 87TPD time delay long enough to accommodate the transient phenomena during switch-in, typically 10 cycles.

### Differential Overvoltage Alarm (87AA, 87BA, 87CA) Elements (SEL-287V Relay)

Select the alarm level to respond to a noncritical failure in the capacitor bank. This alarm can serve as an alert for scheduled maintenance, especially in cases where an unplanned trip and lockout of the capacitor bank can adversely affect the system. Set the 87A elements to pick up when one capacitor unit (four capacitors in a series group) is faulty. This represents about 50 percent of the trip criteria (failure of nine capacitor series groups)

$$87A = 87B = 87C = 0.51 \text{ V}$$

To avoid nuisance alarms but ensure that actual alarm conditions persist, set the 87APD pickup time delay for 1000 cycles.

The relay differential voltage resolution is 0.03 V. To improve security and avoid nuisance operations, do not apply a differential overvoltage setting less than 0.15 V.

## Programmable Logic Masks (SEL-287V Relay)

Figure 5.10 shows the programmable logic masks that implement the described protection and voltage control functions.

Trip Output
MT Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | | | | |
| | | | | | | | |
| | X59T | | | | | | |
| | | | | VHD1 | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A1-Raise Voltage Output
MA1 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | VLD1 | | |
| | | | | | | | |
| | | | | | | | |

A2-Reset Automatic Control Output
MA2 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | | | | |
| | | | | | | | |
| | X59T | | | | | | |
| | | | | | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A5-System Alarm Output
MA5 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | LOPD | VCI1 | VCI2 | | |
| | | | | | | | 87AD |

MER-Event Report Generation
MER Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | | | | |
| | | | | | | | |
| X59P | X59T | | | | | | |
| | | | | | | | |
| | 87HD | LOP | | VCI1 | VCI2 | | |
| | | | | | | 87TD | 87AD |

DWG: M287V027

**Figure 5.10: Programmable Logic Mask Settings–SEL-287V Relay**

### MT Mask Controls the TRIP Output

The MT mask contains the instantaneous overvoltage elements for the Source X, the definite-time overvoltage element, X59T, the phase differential overvoltage time-delayed trip elements, 87TD and 87HD, and the undervoltage control voltage output, VHD1.

When one of these conditions asserts in the Relay Word, the TRIP output contacts close.

### MA1 Mask Controls the A1 Output, Raises Voltage, Scheme 1

The MA1 mask contains only VLD1. Relay Word Bit VLD1 asserts for a low system voltage and causes the A1 contact to close.

### MA2 Mask Controls the A2 Output, Resets Automatic Mode

The MA2 mask contains all the elements set in the MT mask except VHD1. When any protective element set in the MA2 programmable logic mask asserts, the A2 contact closes, putting the voltage control scheme in manual mode.

### MA5 Mask Controls the A5 Output, System Alarm Conditions

The MA5 mask contains the time-delayed dropout Loss-of-Potential condition, LOPD, the voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential overvoltage alarm, 87AD. The A5 contact closes when any of these conditions assert. Monitor this output and use it to alert the operator to unusual system conditions.

### MER Mask Controls Event Report Generation

The MER mask contains all the elements in the MT mask as well as the definite-time overvoltage pickup elements, X59P, Loss-of-Potential condition, LOP, voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential overvoltage alarm, 87AD.

The first time an element set in the MER mask asserts, the relay generates an event report. After tripping, it also generates an event report automatically. The MT mask elements have also been asserted in the MER mask as a redundancy. The other elements represent conditions under which event report generation is probably desirable.

### High-Set Differential Overvoltage Trip (87H1P, 87H2P) Elements (SEL-287V-2 Relay)

There are two independent settings for this function: 87H1P and 87H2P. The relay compares the 87H1P value with differential voltage, dV, if the formula | VX | –K•|VY| produces a positive result. The relay uses the 87H2P setting when dV < 0.

Faults in the capacitor bank result in increasing the Source Y voltage and making the dV value negative. Only short circuiting the low capacitor will decrease the Y voltage to 0 V, but this is an unlikely case.

Set the 87H2P threshold by using the same calculation that you used for the SEL-287V Relay.

87H2P = 4.65 V

Set the 87H1P threshold to trip the capacitor bank for the abnormal situation in the low voltage capacitors, when Source Y voltage drops to less than 70 percent of nominal value and the VX voltage remains unchanged.

87H1P = 0.3 • K • |VY|n = 0.3 • 0.635 • 100 = 19.05 V

|VY|n = secondary voltage from the low voltage capacitors at bus nominal voltage (275 kV)

Set the 87HPD time delay (common for both elements 87H1P and 87H2P) to five cycles.

### Differential Overvoltage Trip (87T1P, 87T2P) Elements (SEL-287V-2 Relay)

The 87T1P element activates when the sign of the equation dV = |VX| – K • |VY| is positive. Because faults in the fuseless capacitor bank example result in dV having a negative value, the 87T1P element is not used. Set the 87T1P threshold value for the maximum possible setting:

87T1P = 150 V

The 87T2P element activates when the sign of the equation dV = |VX| – K • |VY| is negative. The considerations for the setting of 87T2P threshold are the same as for the 87T element in the SEL-287V Relay.

87T2P = 1.20 V

Set the 87TPD time delay (common for both elements 87T1P and 87T2P) long enough to accommodate transient phenomena during switch-in, typically 10 cycles.

### Differential Overvoltage Alarm (87A1, 87A2) Elements (SEL-287V-2 Relay)

The SEL-287V-2 Relay does not have separate per-phase alarm threshold settings but has above-tap and below-tap thresholds that apply to all three phases.

The 87A1 element responds to a positive value of the differential voltage, dV, and is used as an alarm to signal an abnormal situation in the capacitor bank. Set the 87A1 threshold value equal to the 87T2P setting.

87A1 = 1.20 V

The 87A2 element is set to detect failure of one capacitor unit in the string (see Table 5.12).

87A2 = 0.51 V

To avoid nuisance alarms but ensure that actual alarm conditions persist, set the 87APD pickup time delay for 1000 cycles

The relay differential voltage resolution is 0.03 V. To improve security and avoid nuisance operations, do not apply a differential overvoltage setting less than 0.15 V.

### Programmable Logic Masks (SEL-287V-2 Relay)

Figure 5.11 shows the programmable logic masks that implement the protection and voltage control functions.

Trip Output
MT Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | | | | |
| | | | | | | | |
| | X59T | | | | | | |
| | | | | VHD1 | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A1-Raise Voltage Output
MA1 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | VLD1 | | |
| | | | | | | | |
| | | | | | | | |

A2-Reset Automatic Control Output
MA2 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | | | | |
| | | | | | | | |
| | X59T | | | | | | |
| | | | | | | | |
| | 87HD | | | | | | |
| | | | | | | 87TD | |

A5-System Alarm Output
MA5 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | LOPD | VCI1 | VCI2 | | |
| | | | | 87A1D | | | 87A2D |

MER-Event Report Generation
MER Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X59A | X59B | X59C | | | | | |
| | | | | | | | |
| X59P | X59T | | | | | | |
| | | | | | | | |
| | 87HD | LOP | | VCI1 | VCI2 | | |
| | | | | 87A1D | | 87TD | 87A2D |

DWG: M287V028

**Figure 5.11: Programmable Logic Mask Settings–SEL-287V-2 Relay**

## MT Mask Controls the TRIP Output

The MT mask contains the instantaneous overvoltage elements for the Source X, the definite-time overvoltage element, X59T, the phase differential overvoltage time-delayed trip elements, 87TD and 87HD, and the voltage control lower voltage output, VHD1.

When one of these Relay Word bits asserts, the TRIP output contacts close.

## MA1 Mask Controls the A1 Output, Raises Voltage, Scheme 1

The MA1 mask contains only VLD1. When the VLD1 Relay Word bit asserts, it indicates a low system voltage and causes the A1 contact to close.

## MA2 Mask Controls the A2 Output, Resets Automatic Mode

The MA2 mask contains all of the elements set in the MT mask except VHD1. When any protective element set in the MA2 programmable logic mask asserts, the A2 contact closes, putting the voltage control scheme in manual mode.

## MA5 Mask Controls the A5 Output, System Alarm Conditions

The MA5 mask contains the time-delayed dropout Loss-of-Potential condition, LOPD, the voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential

overvoltage alarms, 87A1D and 87A2D. The A5 contact closes when any of these conditions assert. Monitor this output and use it to alert the operator to unusual system conditions.

### MER Mask Controls Event Report Generation

The MER mask contains all of the elements in the MT mask, as well as the definite-time overvoltage pickup elements, X59P, Loss-of-Potential condition, LOP, voltage control instability indicators, VCI1 and VCI2, and the time-delayed phase differential overvoltage alarms, 87A1D and 87A2D.

### For More Information

For more information on capacitor bank protection methods and standards, refer to the *IEEE C37.99 : 1980 Guide for Protection of Shunt Capacitor Banks* and the *ANSI/IEEE Std. 18 : 1980 Standard for Shunt Power Capacitors*.

## THREE-PHASE UNDERVOLTAGE LOAD SHEDDING

When a large load center is fed from remote generation sources through parallel lines, it is possible that under heavy load conditions, loss of a major load-carrying transmission line may cause the voltage to collapse. Three-phase undervoltage loadshedding may be necessary to prevent a total voltage collapse from occurring due to high load conditions and lack of reactive support.

When one of the parallel lines is removed due to a fault or other occurrence, the load is transferred to other parts of the system. This increases the reactive losses on the system due to increased current flow on the remaining lines and results in decreased receiving end voltage. If the load is very high and local reactive support is insufficient, the voltage continues to decrease due to the increased current draw from the receiving end load (i.e., as the voltage decreases, the current increases to hold the real power the same). If this condition continues, it may cause system overload and result in a major outage.

One solution is to trip off blocks of load when the voltage starts to collapse. Because this is a three-phase condition, three-phase undervoltage elements are used to detect the presence of a possible voltage collapse and trip load off after a set time delay.

Because this is a 60 Hz phenomenon (the generation sources do not see the low-voltage condition and keep the system frequency stable), an underfrequency load-shedding scheme may not operate. Therefore, using the undervoltage condition to trip off load is an ideal application.

Once the system has recovered, the blocks of load can be restored. To ensure system voltage stabilization, this should be done after a long time delay.

### AC Schematic

Figure 5.12 shows an example substation where load may be dropped for an undervoltage condition. The Source Y voltage input is connected to the high-voltage bus potential transformers.

The relay is set to detect a three-phase undervoltage condition and trip the circuit breakers specified for load shedding after a specified time delay. The voltage control logic can also be used to restore power after system voltage returns to normal.

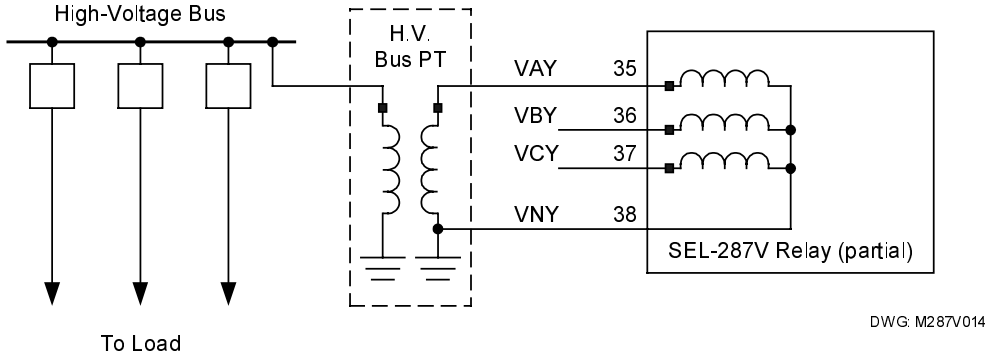



**Figure 5.12: Three-Phase Undervoltage Load Shedding—Typical AC Schematic**

## DC Schematic

Figure 5.13 shows a dc schematic using the SEL-287V Relay in an undervoltage load shedding scheme. Assuming normal system voltage conditions, the 3Y59 element is picked up and the A3 contact is closed. When a system undervoltage condition occurs, the 3Y27 element picks up and starts the A4 timer (A4PD). After the A4PD time delay, it trips the associated circuit breakers and sets the LATCH (LTCH) bit by energizing the ET2 input. The A1 output is masked by the LTCH bit and gives local annunciation and/or SCADA indication. A1 also enables load restoration logic by energizing the LE2 input.

Once system voltage returns to normal, the voltage control logic starts timing to allow restoration of the tripped load. The A2 output contact is masked with the VHD2 bit. Once the A2 contact closes, it energizes the ET1 input and resets the LATCH bit. This resets the voltage control logic and drops the SCADA alarm.

SCADA alarm reset signals operations personnel to start closing the tripped circuit breakers.

If load restoration logic is not used, the LATCH bit can be reset via SCADA input to ET1 or from the breaker 52A contact.

For this scheme design, if relay potential is lost, the load-shedding scheme should be disabled before relay potential is restored.

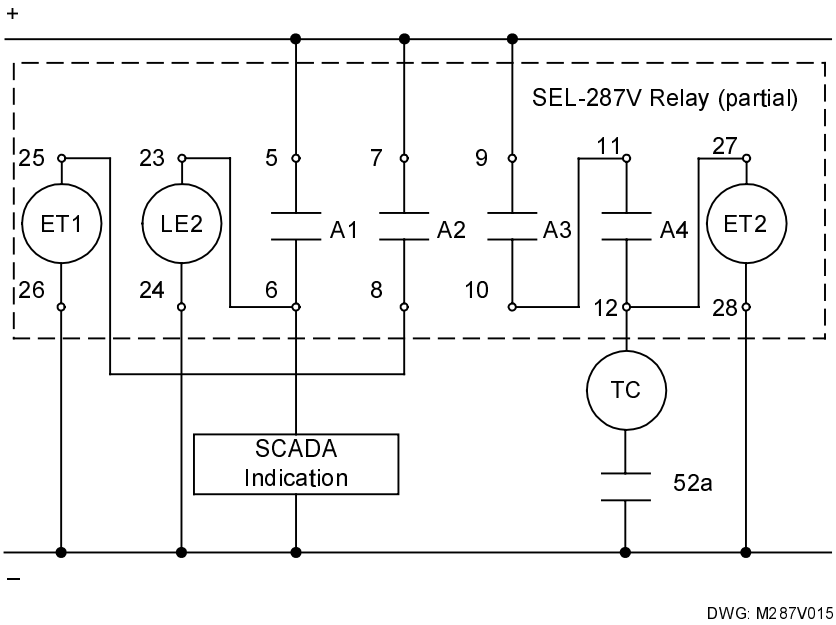



**Figure 5.13: Three-Phase Undervoltage Load Shedding—Typical DC Schematic**

Figure 5.14 shows the programmable mask logic for this scheme.

A1-Latch Logic
MA1 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | LTCH | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

A2-Load Restoration
MA2 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | VHD2 | |
| | | | | | | | |
| | | | | | | | |

A3-Three-Phase Voltage Threshold
MA3 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | 3Y59 | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

A4-Three-Phase Undervoltage Threshold
MA4 Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | | | | | 3Y27 |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

MER-Event Report Generation
MER Logic Mask

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |
| | | | LTCH | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

DWG: M287V013

**Figure 5.14: Programmable Logic Mask Settings for Scheme of Figure 5.12**

## Setting Criteria

The threshold for the three-phase undervoltage (3Y27) element and associated timer (A4PD) setting are dictated solely by your system voltage stability criteria. However, there are some guidelines to setting other elements for this application.

The latch feature must be set to LTCHE=Y. The three-phase undervoltage condition (3Y27 element) is set by the Y27L setting. The A4PD timer provides the undervoltage tripping delay. The Y59I determines the three-phase voltage threshold (3Y59). Set Y59I to pick up for any undervoltage conditions for which you want to trip.

The element 59P2 is used for load restoration logic (Voltage Control Scheme 2) and should be set at an adequate voltage level for this purpose. The Voltage Selection Scheme should be selected for the Independent mode (VSS=I). This enables the Scheme 2 logic for the Source Y potentials only. THP2 should be set for the restoration delay time after the 59P2 picks up. Loss-of-potential logic is also set by LOPE2=Y. Voltage control logic checks the 3Y27 element before starting the THP2 timer. This gives added security to ensure that system voltage is above the undervoltage trip level before restoring load.

If you do not use load restoration logic, ET1 can be energized from an external SCADA contact or the circuit breaker 52A contact. This resets the LATCH bit and opens the A1 contact. This means that A1 closes and the local or SCADA alarm remains in until reset by closing the breaker or SCADA.

The A3 output contact is set by the 3Y59 bit and provides security to prevent tripping on loss-of-potential or close in three-phase faults. The time delay for the undervoltage load-shedding scheme (A4PD) should prevent any false trips due to a race condition between 3Y27 pickup and 3Y59 dropout.

## Programmable Logic Masks

Figure 5.14 shows the programmable logic masks that implement the protection and control functions described above.

### MA1 Mask Controls the A1 Output, Latch Logic

The MA1 mask contains only LTCH. When the ET2 input is asserted, the LTCH bit in the Relay Word asserts and the A1 contact closes. This sends an alarm to SCADA or gives a local alarm and energizes the LE2 input to enable the Load Restoration scheme.

### MA2 Mask Controls the A2 Output, Load Restoration

The MA2 mask contains only VHD2. When the system voltage returns to normal after a undervoltage loadshedding trip, the Scheme 2 voltage control logic starts timing. After the time delay set by THD2, the VHD2 bit asserts and closes the A2 contact. This resets the LTCH bit and SCADA alarm and allows load restoration to begin.

### MA3 Mask Controls the A3 Output, Three-Phase Voltage Threshold

The MA3 Mask contains only 3Y59. When the three-phase system voltage is above the Y59I setting the A3 contact closes.

### MA4 Mask Controls the A4 Output, Three-Phase Undervoltage Threshold

The MA4 Mask contains only 3Y27. When the three-phase system voltage is below the Y27L setting, the 3Y27 bit asserts and starts the A4 pickup delay timer. After A4PD pickup delay time, the A4 contact closes.

### MER Mask Controls Event Report Generation

The MER mask contains only LTCH. The LTCH bit sets any time the undervoltage load-shedding scheme operates (A3 and A4 contacts close to trip). This causes event report generation any time an undervoltage trip occurs.

# SETTINGS SHEET
# FOR THE SEL-287V-0, 1 RELAY

Date _____

**Substation**_____ **Bank** _____

**Breaker** _____ **Device No.**_____

**Function** _____

**Make** _____ **Model/Style No.**_____

**Part #**_____ **Software Version** _____

**Serial #**_____ **Power Supply**_____**Volts ac/dc** **Logic Input**_____**Vdc**

**Secondary Inputs: 0–150 V $_{l-n}$, 60 Hz**

| Binary-Hexadecimal Conversion Chart | | | | |
|---|---|---|---|---|
| **Binary** | **Hexadecimal** | | **Binary** | **Hexadecimal** |
| 0000 | 0 | | 1000 | 8 |
| 0001 | 1 | | 1001 | 9 |
| 0010 | 2 | | 1010 | A |
| 0011 | 3 | | 1011 | B |
| 0100 | 4 | | 1100 | C |
| 0101 | 5 | | 1101 | D |
| 0110 | 6 | | 1110 | E |
| 0111 | 7 | | 1111 | F |

| ACCESS Command Passwords (6 characters excluding SPACE, COMMA, SEMICOLON, and SLASH) | |
|---|---|
| LEVEL 0: "=" | ACCESS **<ENTER>** PASSWORD |
| LEVEL 1: "=>" | 2ACCESS **<ENTER>** PASSWORD |
| LEVEL 2: "=>>" | ENTER SETTINGS PER TABLE |
| **Note:** | For new relays begin with LEVEL 1 password = OTTER and LEVEL 2 password = TAIL. When in LEVEL 2 use password 1 and 2 commands to modify passwords. |

## Logic Mask Settings (LOGIC Command)

| **MASK: MT (Trip)** | | | | | | | | | **Hexadecimal Setting** |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD | |

# SETTINGS SHEET
# FOR THE SEL-287V-0, 1 RELAY

Date _____

| MASK: MA1 (A1 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD | |

| MASK: MA2 (A2 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD | |

| MASK: MA3 (A3 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD | |

# SETTINGS SHEET
# FOR THE SEL-287V-0, 1 RELAY

Date _____

| MASK: MA4 (A4 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD | |

| MASK: MA5 (A5 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD | |

| MASK: MER (Event Report Trigger) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87AT | 87AA | 87BT | 87BA | 87CT | 87CA | 87TD | 87AD | |

## Relay Settings (SET Command)

| Settings Increment Chart | |
|---|---|
| Cycles | 1 cycle steps, unless otherwise noted |
| Volts | in .03 steps |

### Relay Settings

| Description | Range | Abbrev. | | Setting |
|---|---|---|---|---|
| Relay ID | As many as 39 characters | **ID** | = | |
| Phase Undervoltage Threshold for Source X | 0.00–150.00 V | **X27L** | = | |
| Phase Overvoltage Threshold for Source X | 0.00–150.00 V | **X59I** | = | |
| Phase Undervoltage Threshold for Source Y | 0.00–150.00 V | **Y27L** | = | |
| Phase Overvoltage Threshold for Source Y | 0.00–150.00 V | **Y59I** | = | |
| Dropout Delay for Source Y Three-Phase Overvoltage Condition | 0–64000 cycles | **3Y59D** | = | |
| Pickup Threshold of Definite-Time Overvoltage Element for Source X | 0.00–150.00 V | **X59PU** | = | |
| Time Delay of Definite-Time Overvoltage Element for Source X | 0–64000 cycles | **X59D** | = | |
| Pickup Threshold of Definite-Time Overvoltage Element for Source Y | 0.00–150.00 V | **Y59PU** | = | |
| Time Delay of Definite-Time Overvoltage Element for Source Y | 0–64000 cycles | **Y59D** | = | |
| Voltage Selection Scheme | I, B, X | **VSS** | = | |
| Voltage-Control Overvoltage Setting for Scheme 1 | 0.00–150.00 V | **59P1** | = | |
| Overvoltage Control Time Delay Pickup | 0–64000 cycles | **THP1** | = | |
| Overvoltage Control Time Delay Dropout | 0–64000 cycles | **THD1** | = | |
| Voltage-Control Undervoltage Setting | 0.00–150.00 V | **27P1** | = | |
| Undervoltage Control Time Delay Pickup | 0–64000 cycles | **TLP1** | = | |
| Undervoltage Control Time Delay Dropout | 0–64000 cycles | **TLD1** | = | |
| Voltage-Control Overvoltage Setting for Scheme 2 | 0.00–150.00 V | **59P2** | = | |
| Overvoltage Control Time Delay Pickup | 0–64000 cycles | **THP2** | = | |
| Overvoltage Control Time Delay Dropout | 0–64000 cycles | **THD2** | = | |
| Voltage-Control Undervoltage Setting | 0.00–150.00 V | **27P2** | = | |
| Undervoltage Control Time Delay Pickup | 0–64000 cycles | **TLP2** | = | |
| Undervoltage Control Time Delay Dropout | 0–64000 cycles | **TLD2** | = | |
| 87A Ratio Adjustment Factor | 0.000–1.999 | **KA** | = | |
| 87B Ratio Adjustment Factor | 0.000–1.999 | **KB** | = | |
| 87C Ratio Adjustment Factor | 0.000–1.999 | **KC** | = | |
| 87A Alarm Threshold | 0.00–150.00 V | **87AA** | = | |
| 87B Alarm Threshold | 0.00–150.00 V | **87BA** | = | |
| 87C Alarm Threshold | 0.00–150.00 V | **87CA** | = | |
| 87A, 87B, and 87C Trip Threshold | 0.00–150.00 V | **87T** | = | |
| 87A, 87B, and 87C High-Set Trip Threshold | 0.00–150.00 V | **87H** | = | |
| Pickup Delay for 87A Differential Overvoltage | 0–64000 cycles | **87APD** | = | |

# SETTINGS SHEET
# FOR THE SEL-287V-0, 1 RELAY

Date _____

## Relay Settings (continued)

| Description | Range | Abbrev. | | Setting |
|---|---|---|---|---|
| Pickup Delay for 87T Differential Overvoltage | 0–64000 cycles | **87TPD** | = | |
| Pickup Delay for 87H Differential Overvoltage | 0–64000 cycles | **87HPD** | = | |
| Dropout Delay for 87A, 87T, and 87H Differential Overvoltage Conditions and A4 and A5 Output Contacts | 0–64000 cycles | **87DO** | = | |
| Pickup Delay for A1 Output Contact | 0–64000 cycles | **A1PD** | = | |
| Pickup Delay for A2 Output Contact | 0–64000 cycles | **A2PD** | = | |
| Pickup Delay for A3 Output Contact | 0–64000 cycles | **A3PD** | = | |
| Pickup Delay for A4 Output Contact | 0–64000 cycles | **A4PD** | = | |
| Pickup Delay for A5 Output Contact | 0–64000 cycles | **A5PD** | = | |
| Min. Trip Duration Timer | 0–255 cycles | **TDUR** | = | |
| Latch Bit (LTCH) Enable | Y, N | **LTCHE** | = | |
| Scheme 1 Voltage Control Logic LOP Enable | Y, N | **LOPE1** | = | |
| Scheme 2 Voltage Control Logic LOP Enable | Y, N | **LOPE2** | = | |
| Source X or Y LOP Dropout Delay | 0–64000 cycles | **LOPD** | = | |
| Port 1 Communications Timeout | 0–30 minutes | **TIME1** | = | |
| Port 2 Communications Timeout | 0–30 minutes | **TIME2** | = | |
| Destination for Automatic Messages | Port 1, 2, or 3 (both) | **AUTO** | = | |
| Rings Before Port 1 Modem answers | –30 to 30, excluding 0 | **RINGS** | = | |

# SETTINGS SHEET
# FOR THE SEL-287V-2 RELAY

Date _____

**Substation**_____ **Bank** _____

**Breaker** _____ **Device No.**_____

**Function** _____

**Make** _____ **Model/Style No.**_____

**Part #**_____ **Software Version** _____

**Serial #**_____ **Power Supply**_____**Volts ac/dc** **Logic Input**_____**Vdc**

**Secondary Inputs: 0–150 V $_{l-n}$, 60 Hz**

| Binary-Hexadecimal Conversion Chart | | | | |
|---|---|---|---|---|
| **Binary** | **Hexadecimal** | | **Binary** | **Hexadecimal** |
| 0000 | 0 | | 1000 | 8 |
| 0001 | 1 | | 1001 | 9 |
| 0010 | 2 | | 1010 | A |
| 0011 | 3 | | 1011 | B |
| 0100 | 4 | | 1100 | C |
| 0101 | 5 | | 1101 | D |
| 0110 | 6 | | 1110 | E |
| 0111 | 7 | | 1111 | F |

| ACCESS Command Passwords (6 characters excluding SPACE, COMMA, SEMICOLON, and SLASH) | |
|---|---|
| LEVEL 0: "=" | ACCESS **<ENTER>** PASSWORD |
| LEVEL 1: "=>" | 2ACCESS **<ENTER>** PASSWORD |
| LEVEL 2: "=>>" | ENTER SETTINGS PER TABLE |
| **Note:** | For new relays begin with LEVEL 1 password = OTTER and LEVEL 2 password = TAIL. When in LEVEL 2 use password 1 and 2 commands to modify passwords. |

## Logic Mask Settings (LOGIC Command)

| **MASK: MT (Trip)** | | | | | | | | | **Hexadecimal Setting** |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D | |

# SETTINGS SHEET
# FOR THE SEL-287V-2 RELAY

Date _____

| MASK: MA1 (A1 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D | |

| MASK: MA2 (A2 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D | |

| MASK: MA3 (A3 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D | |

# SETTINGS SHEET
# FOR THE SEL-287V-2 RELAY

Date _____

| MASK: MA4 (A4 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D | |

| MASK: MA5 (A5 Contact) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D | |

| MASK: MER (Event Report Trigger) | | | | | | | | | Hexadecimal Setting |
|---|---|---|---|---|---|---|---|---|---|
| ROW #1: Relay Word Binary Representation | X59A | X59B | X59C | 3Y59 | Y59A | Y59B | Y59C | 3Y59D | |
| ROW #2: Relay Word Binary Representation | X27A | X27B | X27C | LTCH | Y27A | Y27B | Y27C | 3Y27 | |
| ROW #3: Relay Word Binary Representation | X59P | X59T | Y59P | Y59T | 59P1 | 27P1 | 59P2 | 27P2 | |
| ROW #4: Relay Word Binary Representation | VH1 | VL1 | VH2 | VL2 | VHD1 | VLD1 | VHD2 | VLD2 | |
| ROW #5: Relay Word Binary Representation | 87H | 87HD | LOP | LOPD | VCI1 | VCI2 | 87T | 87A | |
| ROW #6: Relay Word Binary Representation | 87A1 | 87AA | 87A2 | 87BA | 87A1D | 87CA | 87TD | 87A2D | |

## Relay Settings (SET Command)

| Settings Increment Chart | |
|---|---|
| Cycles | 1 cycle steps, unless otherwise noted |
| Volts | in .03 steps |

### Relay Settings

| Description | Range | Abbrev. | | Setting |
|---|---|---|---|---|
| Relay ID | As many as 39 characters | **ID** | = | |
| Phase Undervoltage Threshold for Source X | 0.00–150.00 V | **X27L** | = | |
| Phase Overvoltage Threshold for Source X | 0.00–150.00 V | **X59I** | = | |
| Phase Undervoltage Threshold for Source Y | 0.00–150.00 V | **Y27L** | = | |
| Phase Overvoltage Threshold for Source Y | 0.00–150.00 V | **Y59I** | = | |
| Dropout Delay for Source Y Three-Phase Overvoltage Condition | 0–64000 cycles | **3Y59D** | = | |
| Pickup Threshold of Definite-Time Overvoltage Element for Source X | 0.00–150.00 V | **X59PU** | = | |
| Time Delay of Definite-Time Overvoltage Element for Source X | 0–64000 cycles | **X59D** | = | |
| Pickup Threshold of Definite-Time Overvoltage Element for Source Y | 0.00–150.00 V | **Y59PU** | = | |
| Time Delay of Definite-Time Overvoltage Element for Source Y | 0–64000 cycles | **Y59D** | = | |
| Voltage Selection Scheme | I, B, X | **VSS** | = | |
| Voltage-Control Overvoltage Setting for Scheme 1 | 0.00–150.00 V | **59P1** | = | |
| Overvoltage Control Time Delay Pickup | 0–64000 cycles | **THP1** | = | |
| Overvoltage Control Time Delay Dropout | 0–64000 cycles | **THD1** | = | |
| Voltage-Control Undervoltage Setting | 0.00–150.00 V | **27P1** | = | |
| Undervoltage Control Time Delay Pickup | 0–64000 cycles | **TLP1** | = | |
| Undervoltage Control Time Delay Dropout | 0–64000 cycles | **TLD1** | = | |
| Voltage-Control Overvoltage Setting for Scheme 2 | 0.00–150.00 V | **59P2** | = | |
| Overvoltage Control Time Delay Pickup | 0–64000 cycles | **THP2** | = | |
| Overvoltage Control Time Delay Dropout | 0–64000 cycles | **THD2** | = | |
| Voltage-Control Undervoltage Setting | 0.00–150.00 V | **27P2** | = | |
| Undervoltage Control Time Delay Pickup | 0–64000 cycles | **TLP2** | = | |
| Undervoltage Control Time Delay Dropout | 0–64000 cycles | **TLD2** | = | |
| 87A Ratio Adjustment Factor | 0.000–1.999 | **KA** | = | |
| 87B Ratio Adjustment Factor | 0.000–1.999 | **KB** | = | |
| 87C Ratio Adjustment Factor | 0.000–1.999 | **KC** | = | |
| 87 Alarm Threshold Above Tap | 0.00–150.00 V | **87A1P** | = | |
| 87 Alarm Threshold Below Tap | 0.00–150.00 V | **87A2P** | = | |
| 87 Trip Threshold Above Tap | 0.00–150.00 V | **87T1P** | = | |
| 87 Trip Threshold Below Tap | 0.00–150.00 V | **87T2P** | = | |
| 87 High-Set Trip Threshold ($\Delta V>0$) | 0.00–150.00 V | **87H1P** | = | |
| 87 High-Set Trip Threshold ($\Delta V\leq 0$) | 0.00–150.00 V | **87H2P** | = | |

# SETTINGS SHEET
# FOR THE SEL-287V-2 RELAY

Date _____

## Relay Settings (continued)

| Description | Range | Abbrev. | | Setting |
|---|---|---|---|---|
| Pickup Delay for 87 Alarm Condition | 0–64000 cycles | **87APD** | = | |
| Pickup Delay for 87 Trip Condition | 0–64000 cycles | **87TPD** | = | |
| Pickup Delay for 87 High-Set Condition | 0–64000 cycles | **87HPD** | = | |
| Dropout Delay for 87 Alarm, Trip, High-Set Conditions, A4 and A5 Output Contacts | 0–64000 cycles | **87DO** | = | |
| Pickup Delay for A1 Output Contact | 0–64000 cycles | **A1PD** | = | |
| Pickup Delay for A2 Output Contact | 0–64000 cycles | **A2PD** | = | |
| Pickup Delay for A3 Output Contact | 0–64000 cycles | **A3PD** | = | |
| Pickup Delay for A4 Output Contact | 0–64000 cycles | **A4PD** | = | |
| Pickup Delay for A5 Output Contact | 0–64000 cycles | **A5PD** | = | |
| Min. Trip Duration Timer | 0–255 cycles | **TDUR** | = | |
| Latch Bit (LTCH) Enable | Y, N | **LTCHE** | = | |
| Scheme 1 Voltage Control Logic LOP Enable | Y, N | **LOPE1** | = | |
| Scheme 2 Voltage Control Logic LOP Enable | Y, N | **LOPE2** | = | |
| Source X or Y LOP Dropout Delay | 0–64000 cycles | **LOPD** | = | |
| Port 1 Communications Timeout | 0–30 minutes | **TIME1** | = | |
| Port 2 Communications Timeout | 0–30 minutes | **TIME2** | = | |
| Destination for Automatic Messages | Port 1, 2, or 3 (both) | **AUTO** | = | |
| Rings Before Port 1 Modem answers | –30 to 30, excluding 0 | **RINGS** | = | |

# TABLE OF CONTENTS



# TABLES



# FIGURES

# SECTION 6: INSTALLATION

## INSTALLATION

### Mounting

The relay is designed for mounting by its front vertical flanges in a 19" vertical relay rack. It may also be mounted semi-flush in a switchboard panel. Use four #10 screws for mounting. This section includes front- and rear-panel drawings.

### Frame Ground Connection

Terminal 46 on the rear panel must be connected to frame ground for safety and performance. These terminals connect directly to the chassis ground of the instrument.

### Power Connections

Terminals 44 and 45 on the rear panel must be connected to a source of control voltage. Control power passes through these terminals to the fuse(s) and a toggle switch, if installed. The power continues through a surge filter and connects to the switching power supply. The control power circuitry is isolated from the frame ground.

### Secondary Circuits

The relay presents a very low burden to the secondary potential circuits. It requires four-wire wye potentials.

### Control Circuits

The control inputs are dry. For example, to assert the ET1 input, you must apply control voltage to the ET1 input terminals. Each input is individually isolated, and a terminal pair is brought out for each input. There are no internal connections between control inputs.

Control outputs are dry relay contacts rated for tripping duty. A metal-oxide varistor (MOV) protects each contact.

### Communications Circuits

Connections to the two EIA-232 serial communications ports are made via the two nine-pin connectors labeled Port 1 and Port 2R on the rear panel and Port 2F on the front panel. Pins 5 and 9 connect directly to frame (chassis) ground. See Table 6.1 for pin assignment.

**WARNING**

Do not rely upon pins 5 and 9 for safety grounding, since their current-carrying capacity is less than control-power short circuit current and protection levels.

The communications circuits are protected by low-energy, low-voltage MOVs and passive RC filters. You can minimize communications-circuit difficulties by keeping the length of the

EIA-RS-232-C cables as short as possible. Lengths of 12 feet or less are recommended, and the cable length should never exceed 100 feet. Use shielded communications cable for lengths greater than 10 feet. Modems are required for communications over long distances.

Route the communications cables well away from the secondary and control circuits. Do not bundle the communications wiring with secondary or control circuit wiring. If these wires are bundled, switching spikes and surges can cause noise in the communications wiring. This noise may exceed the communications logic thresholds and introduce errors. The IRIG-B clock cable should also be routed away from the control wiring and secondary circuits.

## Jumper Selection

Jumpers JMP103, JMP104, and J6 are on the front edge of the main board. They are easily accessed by removing the top cover or front panel. Jumpers JMP3 and soldered wire jumpers JMP4 through JMP11 are toward the back of the main board and are accessed by removing the top cover. Use a pair of small needle-nose pliers to add or remove jumpers.

### EIA-232 Jumpers

J6 provides EIA-232 baud rate selection. Available baud rates are 300, 600, 1200, 2400, 4800, and 9600. To select a baud rate for a particular port, place the jumper so it connects a pin labeled with the desired port to a pin labeled with the desired baud rate.


Do not select two baud rates for the same port. This can damage the baud rate generator.

### Password Protection Jumper

Put JMP103 in place to disable password protection. This feature is useful if passwords are not required or when passwords are forgotten.

### PULSE n Command Enable Jumper

With jumper JMP104 in place, the PULSE n command is enabled. If you remove jumper JMP104, PULSE n command execution results in the message: "Command Aborted."

### A4 Output Contact Jumper

With jumper JMP3 in the A4 position, the A4 output contact operates per the MA4 setting mask. With jumper JMP3 in the ALARM position, the A4 output contact operates with the ALARM output contact.

### Output Contact Soldered Wire Jumpers

All the output contacts can be configured as "a" or "b" contacts with soldered wire jumpers JMP4 through JMP11 (each jumper has positions A and B). The output contact/soldered wire jumper correspondence is as follows:

| Output Contact | Jumper |
|---|---|
| TRIP (terminals 1, 2) | JMP11 |
| TRIP (terminals 3, 4) | JMP10 |
| CLOSE | JMP9 |
| A1 | JMP8 |
| A2 | JMP7 |
| A3 | JMP6 |
| A4 | JMP5 |
| ALARM | JMP4 |

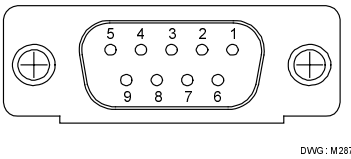
### Communication Port External Power Jumpers

DC power is available from Port 1 and Port 2R to power external devices. Jumpers must be selected to route dc power to the rear-panel connectors. The internal jumpers are near Port 1 and are labeled as follows: JMP12 = +5 V; JMP13 = +12 V; JMP14 = –12 V. Use caution to ensure the dc current requirement of the external equipment does not exceed the relay power supply specifications. Only route dc power to the rear ports if required for your application.

## EIA-232 and IRIG-B Installation

The following information contains specific details regarding communications port pinouts.

Figure 6.1 shows the pin number convention for the nine-pin (EIA-232) port connectors. The following cable listings show several types of EIA-232 cables. These and other cables are available from SEL. Cable configuration sheets are also available at no charge for a large number of devices. Contact the factory for more information.




(female chassis connector, as viewed from outside panel

**Figure 6.1: Nine-Pin Connector Pin Number Convention**

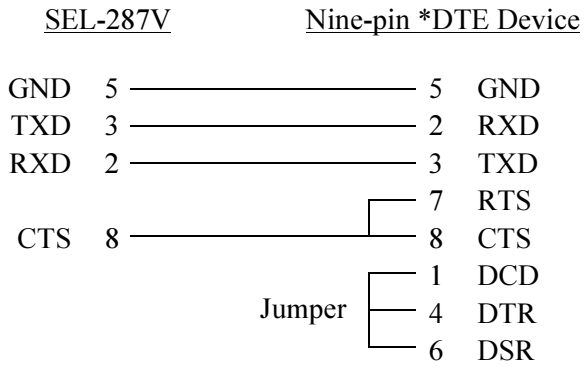
**Table 6.1: SEL-287V Relay Serial Port Connector Pin Assignments**

| Pin | PORT 1, PORT 2R | PORT 2F | Description |
|---|---|---|---|
| 1 | +5 Vdc | N/C | |
| 2 | RXD | RXD | Receive data input. |
| 3 | TXD | TXD | Transmit data output. |
| 4 | +12 Vdc | N/C | |
| 5 | GND | GND | |
| 6 | –12 Vdc | N/C | |

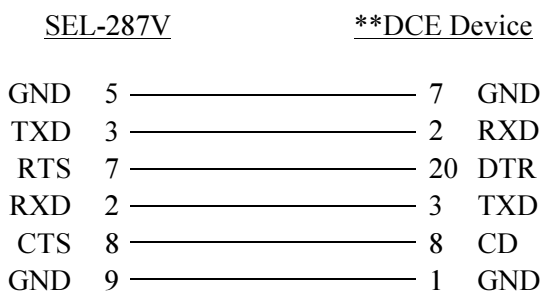
| Pin | PORT 1, PORT 2R | PORT 2F | Description |
|---|---|---|---|
| 7 | RTS | RTS | The relay asserts this line under normal conditions. When its received-data buffer is full, the line is deasserted. It asserts again when the buffer has sufficient room to receive more data. Connected devices should monitor RTS (usually with their CTS input) and stop transmission whenever the line deasserts. If transmission continues, data may be lost. |
| 8 | CTS | CTS | The relay monitors CTS, and transmits characters only if CTS is asserted. |
| 9 | GND | GND | Ground for ground wires and shields. |

## EIA-232 Cables

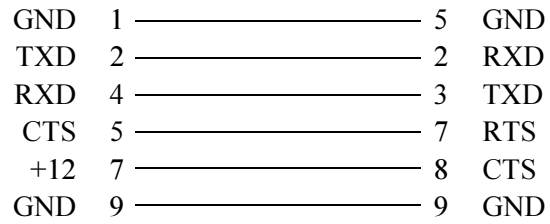
Cable 234A



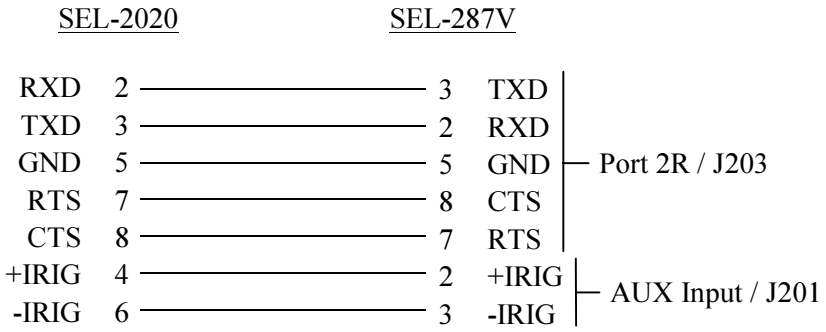

Cable 222



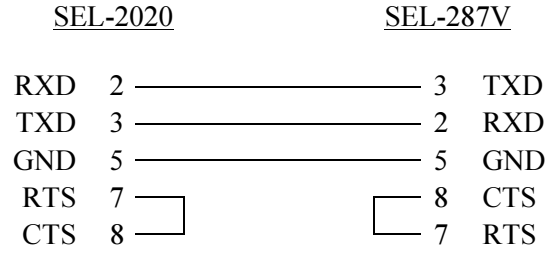
Cable 231




Cable 239
Data and IRIG-B




Cable 272A
Data Only




* DTE = Data Terminal Equipment (Computer, Terminal, Printer, etc.)
** DCE = Data Communications Equipment (Modem, etc.)

## IRIG-B Input Description

The port labeled J201/AUX INPUT receives demodulated IRIG-B input. Pin definitions appear in Table 6.2.

**Table 6.2: IRIG-B Pin Definitions**

| Pin | Name | Description |
|---|---|---|
| 1 | +5 | * |
| 2 | IRIGIN HI | Positive IRIG-B input |
| 3 | IRIGIN LOW | Negative IRIG-B input |
| 4 | +12 | * |
| 6 | –12 | * |
| 5, 9 | GND | Ground for ground wires and shields |

* Consult the factory before using these power supply outputs

The actual IRIG-B input circuit is a 56-ohm resistor in series with an optocoupler input diode. The input diode has a forward drop of about 1.5 volts. Driver circuits should put approximately 10 mA through the diode when "on."

The IRIG-B serial data format consists of a one-second frame containing 100 pulses and divided into fields. The relay decodes the second, minute, hour, and day fields and sets the internal relay clock accordingly.

When IRIG-B data acquisition is activated either manually (with the IRIG command) or automatically, two consecutive frames are taken. The older frame is updated by one second and the two frames are compared. If they do not agree, the relay considers the data erroneous and discards it.

The relay reads the time code automatically about once every five minutes. The relay stops IRIG-B data acquisition 10 minutes before midnight on New Year's Eve so the relay clock may implement the year change without interference from the IRIG-B clock. Ten minutes later, the relay restarts IRIG-B data acquisition.

## INSTALLATION CHECKOUT

You may follow the suggestions below or combine them with your normal practice. Never implement recommendations prohibited by the rules of your normal practice. The checkout procedure recommends various settings for ease of testing. These settings may not be applicable to an in-service installation.

The following equipment is required for initial checkout:

- Portable terminal or computer with interconnecting cable (connect to Port 2F)
- Control power to the relay power connections
- Source of three-phase voltages and at least one current source
- Ohmmeter or contact opening/closing device
- Plug-in mating connectors/wiring harness (for plug-in connector model only)

1. Apply control power and make sure the terminal displays the startup message. If not, set AUTO = 2 with the SET command in Access Level 2. Check the settings with the ACCESS and SHOWSET commands. Use the TIME command to set the clock.

2. Apply three-phase voltages to Sources X and Y. Execute the METER command and make sure the readings are accurate. If they are not, be sure the correct PT ratio was entered. Remember that displayed values are in primary line-to-line volts.

3. Use the TRIGGER command to generate an event record. Type **EVENT 1 <ENTER>** and examine the event record. Refer to the top row of data as the "y" components and the next row as the "x" components. Using the SEL Direction and Polarity Check Form at the end of this section, plot the six voltage phasors to ensure that they are 120° apart, of reasonable magnitudes, and rotating in the positive-sequence direction. The zero-sequence voltage y and x components (times a factor of three) are the totals of the three y components and the three x components. These sums should be near zero if balanced three-phase potentials are present.

4. Use the TARGET command to check all inputs (IN1–IN6). Type **TAR 7 <ENTER>** and the front-panel target LEDs display input states. Corresponding targets and inputs appear below:

| EN | 87A | 87B | 87C | X59T | Y59T | X59I | Y59I | Front-Panel Targets |
|---|---|---|---|---|---|---|---|---|
| | | ET2 | ET1 | LE2 | RE2 | LE1 | RE1 | Inputs |

   An LED illuminates when a corresponding input is energized with nominal control voltage. Apply nominal control voltage to each input and make sure the corresponding LED illuminates. When the test is complete, type **TAR R <ENTER>** to reset and clear the front-panel target LEDs.

5. Proceed to Access Level 2 with the 2ACCESS command and second password. Be sure the ALARM relay contacts close and open when the relay executes the 2ACCESS command. The ALARM pulse will not be detectable if the ALARM contacts are closed due to an alarm condition.

6. Test the tripping function. Apply voltages to Source X and Source Y. Voltages should represent a condition for which the relay should trip. The TRIP contacts remain closed until the trip condition vanishes and the trip duration trip timer expires.

7. Assert either External Trigger input (ET1 or ET2). This should trigger an event record. It does not affect the protective relaying functions in any way.

8. Use the STATUS command to inspect the self-test status. You may wish to save the reading as part of an as-left record.

When local checkout is complete, check communications with the instrument via a remote interface (if used). Make sure the automatic port is properly assigned and that desired timeout intervals are selected for each port. Also, be sure to record password settings.

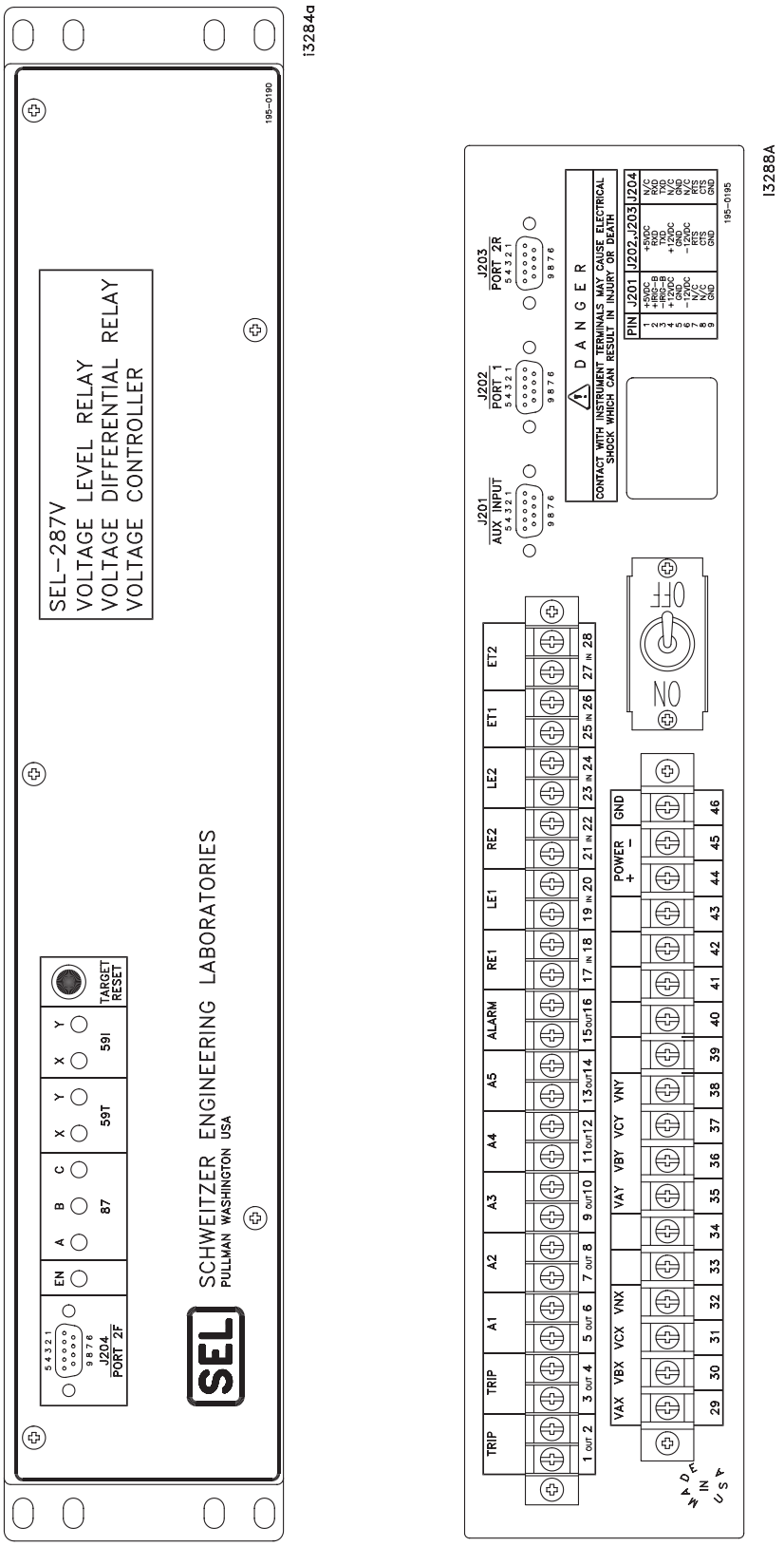



**Figure 6.2: SEL-287V Conventional Terminal Block Model Relay Horizontal Front- and Rear-Panel Drawings**

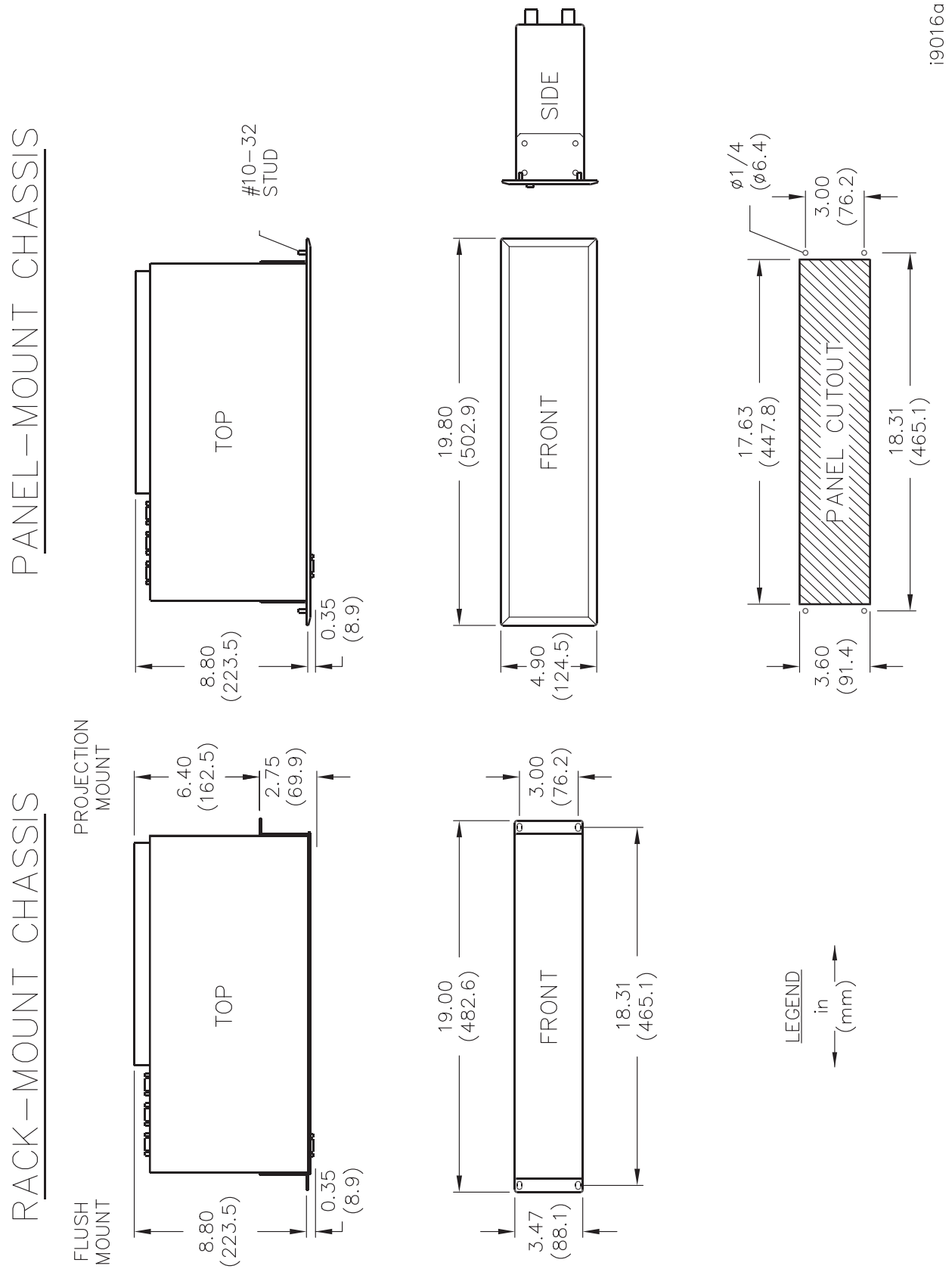



**Figure 6.3: Relay Dimensions, Panel Cutout, and Drill Plan**

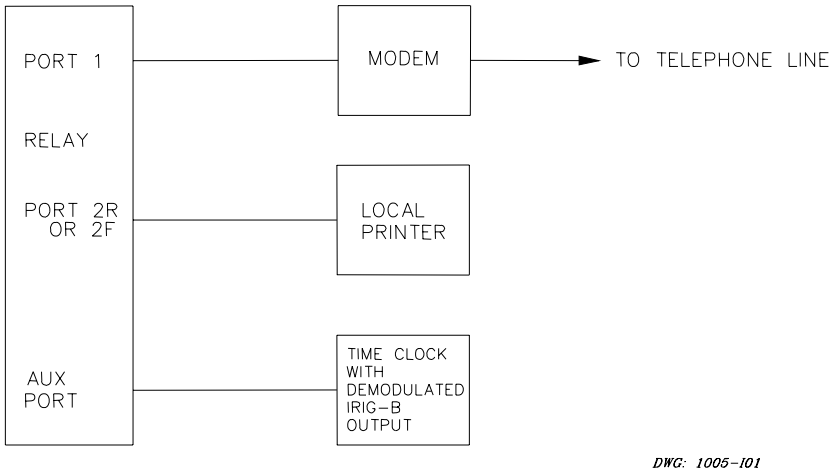



**Figure 6.4: Communications and Clock Connections – One Unit at One Location**

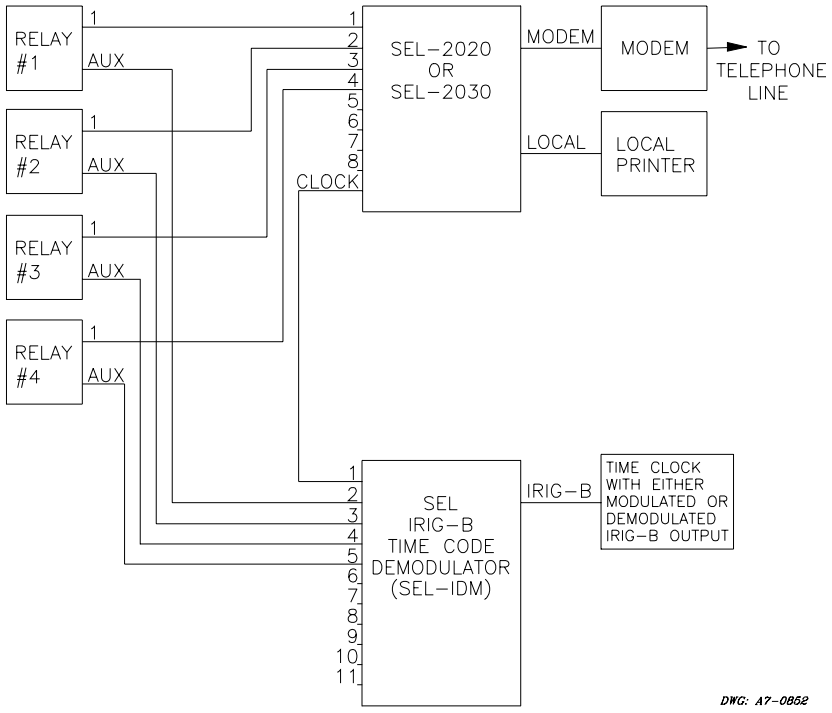



**Figure 6.5: Remote Communications, Local Display, and Clock Connections – Multiple Relay Units at One Location**

# SEL DIRECTION AND POLARITY CHECK FORM

STATION: _____ DATE: ___/___/___ TESTED BY: _____

SWITCH NO.: _____ EQUIPMENT: _____

INSTALLATION: _____ ROUTINE: _____ OTHER: _____

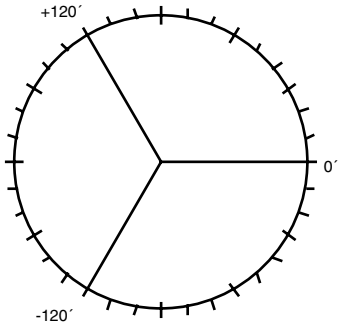
**LOAD CONDITIONS**

STATION READINGS: _____ MW (OUT)(IN) _____ MVAR (OUT)(IN) _____ VOLTS _____ AMPS

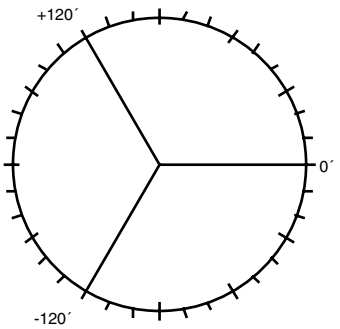
SEL READINGS: _____ MW (+)(-) _____ MVAR (+)(-)

| AS SEEN ON SCREEN | Ia | Ib | Ic | Va | Vb | Vc | |
|---|---|---|---|---|---|---|---|
| COMPANY NOTATION | I( ) | I( ) | I( ) | V( ) | V( ) | V( ) | |
| 1st LINE CHOSEN (Y COMPONENT) | | | | | | | |
| 2nd LINE CHOSEN (X COMPONENT) | | | | | | | |
| CALCULATED MAGNITUDE $\sqrt{X^2 + Y^2}$ | | | | | | | ROW 1 |
| ANGLE IN DEGREES ARCTAN Y/X | | | | | | | |
| VALUE OF Va DEGREES TO OBTAIN Va DEGREES = 0 | | | | | | | |
| @ Va DEGREES = 0, ANGLE USED TO DRAW PHASOR DIAGRAM | | | | | | | ROW 2 |

USE THE VALUES IN ROWS 1 AND 2 ABOVE TO DRAW PHASOR DIAGRAMS BELOW




CURRENTS




VOLTAGES

*DWG: A7-0446*

# SEL DIRECTION AND POLARITY CHECK FORM

STATION: _____ DATE: ___/___/___ TESTED BY: _____

SWITCH NO.: _____ EQUIPMENT: _____

INSTALLATION: _____ ROUTINE: _____ OTHER: _____

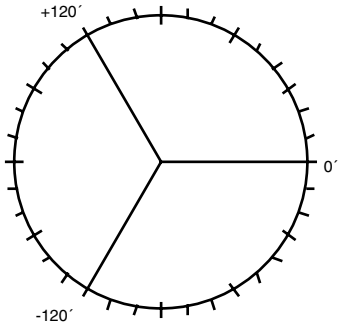
**LOAD CONDITIONS**

STATION READINGS: _____ MW (OUT)(IN) _____ MVAR (OUT)(IN) _____ VOLTS _____ AMPS

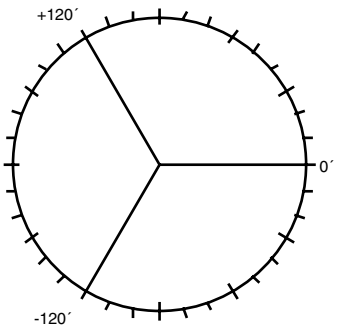
SEL READINGS: _____ MW (+)(-) _____ MVAR (+)(-)

| AS SEEN ON SCREEN | Ia | Ib | Ic | Va | Vb | Vc | |
|---|---|---|---|---|---|---|---|
| COMPANY NOTATION | I( ) | I( ) | I( ) | V( ) | V( ) | V( ) | |
| 1st LINE CHOSEN (Y COMPONENT) | | | | | | | |
| 2nd LINE CHOSEN (X COMPONENT) | | | | | | | |
| CALCULATED MAGNITUDE $\sqrt{X^2 + Y^2}$ | | | | | | | ROW 1 |
| ANGLE IN DEGREES ARCTAN Y/X | | | | | | | |
| VALUE OF Va DEGREES TO OBTAIN Va DEGREES = 0 | | | | | | | |
| @ Va DEGREES = 0, ANGLE USED TO DRAW PHASOR DIAGRAM | | | | | | | ROW 2 |

USE THE VALUES IN ROWS 1 AND 2 ABOVE TO DRAW PHASOR DIAGRAMS BELOW




CURRENTS




VOLTAGES

*DWG: A7-0446*

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# TABLES



# FIGURES

# SECTION 7: MAINTENANCE AND TESTING

## INITIAL CHECKOUT

You should become familiar with the relay and ensure that all functions are operational in the initial checkout procedure.

### Equipment Required

Use the following equipment to perform an initial checkout of the relay:

1. Computer terminal with EIA-232 serial interface
2. Interconnecting cable between terminal and relay
3. Source of control power
4. Two voltage sources

Because the relay elements depend on voltage magnitude only, phase angle is not important. This is an advantage when testing the relay because only two voltage sources are required. One source may drive up to five inputs while the other source drives the input under test.

### Checkout Procedure

In the procedure below, you use several relay commands. While ***Section 3: Communications*** provides a full explanation of all commands, with the following information you should be able to complete the checkout without referring to the detailed descriptions.

**Note:** In this manual, commands to type appear in bold/upper case: **OTTER**. Keys to press appear in bold/upper case/brackets: **<ENTER>**

Relay output appears in the following format and font:

```
Example Settings                  Date: 6/1/92   Time: 01:01:01
```

1. Inspect the instrument for physical damage such as dents or rattles.

2. Connect a computer terminal to PORT 2 on the front or rear panel of the relay. The terminal should be configured to 2400 baud, eight data bits, two stop bits (-E2 model) or one stop bit (-E1 model), and no parity. ***Section 3: Communications*** provides additional details on port configurations. Baud rate selection is described under ***Jumper Selection*** in ***Section 6: Installation***.

3. Connect a frame ground to terminal marked GND on the rear panel. Connect control power to terminals marked + and –.

4. Turn the power on. The enable target (EN) should illuminate. If not, be sure power is present and check the fuse or fuses. The following message should appear on the terminal:

```
Example Settings             Date: 6/1/92Time: 01:01:01

SEL-187V

=
```

The ALARM relay should pull in. Since the LOP bit of the MA5 mask is set, output relay A5 (set to follow LOP) should stay closed until you apply voltage to the Source X voltage inputs. If the relay pulls in but no message is displayed, check the terminal configuration. If neither occurs, turn the power off and refer to the TROUBLESHOOTING guide.

The = prompt indicates that communications with the relay are at Access Level 0, the first of three levels. The only command accepted at this level is ACCESS, which opens communications on Access Level 1, as described below.

5. Type **ACCESS** and press **<ENTER>**. At the prompt, enter the password **OTTER** and press **<ENTER>**. The => prompt should appear, indicating that you have established communications at Access Level 1.

6. The relay is shipped with demonstration settings; type **SHOWSET** and press **<ENTER>** to view these settings. Refer to the SHOWSET command in ***Section 3: Communications*** for a screen capture of what your terminal should display.

   The SET command section provides a complete description of the settings.

   The LOGIC command section includes a detailed explanation of the logic settings. Each column in the logic settings display shows masks for the six rows of the Relay Word as shown in ***Section 2: Specifications***.

   Logic settings appear in hexadecimal format. A table and example of hexadecimal-to-binary conversion appears with the SHOWSET command description.

7. Turn the power off and connect a single source of voltages to the relay at terminals VAX, VBX, VCX, and VNX (Source X) and terminals VAY, VBY, VCY, and VNY (Source Y). Figure 7.1 illustrates Test Connection #1. Apply 67 volts per phase (line-to-neutral).

8. Turn the relay power back on, execute the ACCESS command, and enter the password OTTER again. With potentials applied to the relay, the A5 contacts should now open.

9. Now use the METER command to measure the voltages. With applied voltages of 67 volts per phase on both sources, phase voltage magnitudes should read 67 volts per phase, while differential voltages should read approximately 0 volts secondary.

10. Turn the voltage sources off. Disconnect VAX, VBX, and VCX from the 67 volt source and connect them to the second voltage source. Figure 7.2 illustrates Test Connection #2. Turn both sources on and adjust Source 2 until it delivers 67 volts.

11. This step operates the differential overvoltage elements. Adjust Source 2 until it delivers 68 volts. A moment after the voltage applied to VAX reaches 68 volts, the 87A, 87B, and 87C target lamps illuminate and the A2 contact, A4 contact, A5 contact, and TRIP contacts close. Afterward, the relay displays a short form event report.

12. This step operates the instantaneous overvoltage elements. Decrease the voltage output from Source 2 (VAX, VBX, and VCX) until it delivers 40 volts. This causes X27L to assert, disabling the differential overvoltage function. Press the TARGET RESET button to clear the front-panel targets. Increase the Source 1 voltage (VAY, VBY, and VCY). The Y59I

target lamp illuminates when the Source 1 voltage reaches 80 volts. Y59I is the Source Y instantaneous overvoltage element.

13. Reduce the voltages to zero, ending the element test. Type **HISTORY <ENTER>**. The history command output shows a brief summary for each of the previous events.

14. To view a full event report for one of the events, type **EVENT n <ENTER>**, where n is the event number you wish to see. Press **<CTRL>S** if you would like to pause during the display. Press **<CTRL>Q** to begin scrolling again; **<CTRL>X** to cancel the report.

15. Type **STATUS <ENTER>** to view the self-test status of the relay.

This checkout procedure demonstrates only a few of the features of the relay. Study ***Section 2: Specifications*** and ***Section 3: Communications*** for complete information about the capabilities of this instrument. For more test procedures, see the ***Full Functional Test*** below.

## FULL FUNCTIONAL TEST

This procedure thoroughly tests the SEL-287V Relay protective and control functions.

Because the relay elements depend on voltage magnitude only, phase angle is not important. This is an advantage during relay testing because only two voltage sources are required. One source may drive up to five inputs while the other source drives the input under test.

### Test Methods

There are two ways to test relay element operation: via target lamp illumination or contact closure.

#### Tests Using Target Lamps

You can test the relay with target lamp illumination. Using the TARGET command, set the front-panel targets to display the element under test. For example, single-phase differential overvoltage elements are shown in Relay Word row 6. When you use the command TARGET 6, front-panel LEDs display Relay Word row 6. When an element asserts, the corresponding LED illuminates. Thus, with Target 6 displayed, if the B-phase differential overvoltage alarm condition (87BA) asserts, the fourth LED from the left illuminates. Using the LEDs as indicators, you can measure element operating characteristics.

When the TARGET command sets target LED output to a level other than Level 0 (Relay Targets), front-panel target markings are not relevant to illuminated LEDs. Therefore, it is very important that you use the TARGET R command to return LEDs to TAR 0 when you finish testing. This helps prevent misinterpretation of relay targets by other personnel.

Be aware that if the relay sends an automatic message to a timed serial port, the relay returns the target display to TAR 0 and displays event targets. When testing with target LEDs, set the serial port time-out settings to zero.

Target LEDs are useful for testing because you need not change logic settings between tests.

### Tests Using Output Contacts

To test via output contact closure, set one programmable output contact to close when the condition under test asserts. Using the LOGIC n command, set a 1 in the mask for the condition under test. Set the other elements to 0. When the condition asserts, the output contact closes; when the condition deasserts, the output contact opens. Using contact operation as an indicator, you can measure element operating characteristics.

## Test Procedures

### Equipment Required

The following equipment is necessary to perform a full functional test:

1. Computer terminal with EIA-232 serial interface
2. Interconnecting cable between terminal and relay
3. Source of control power
4. Two voltage sources

Connect the relay to the computer terminal and establish communications with the relay as described in the Initial Checkout Procedure.

Perform the test procedures below as required by your application.

The element test procedures assume a nominal input voltage of 67 volts per phase.

**Note:** Before beginning the element tests, set all MT logic mask elements to zero. This simplifies the procedure.

### Setting Test

To ensure that the relay accepts settings, perform the following steps:

1. Gain Level 2 Access (see ACCESS and 2ACCESS commands).
2. Type **SET <ENTER>**.
3. Change one setting. For example, change Scheme 1 voltage control overvoltage setting 59P1 from 70 to 72 volts.
4. Type **END <ENTER>** to complete the setting procedure. Type **Y** to the prompt: "OK (Y or N) ?" Unless an alarm condition exists, ALARM contacts should close for several seconds while the relay computes internal settings.
5. Use SHOWSET to inspect the settings. Make sure your change was accepted.
6. Use SET and SHOWSET again to restore and check the original settings.
7. Type **LOG MT <ENTER>**.
8. Change one bit.

9. Complete the logic setting procedure.

10. Type **LOG MT <ENTER>** again and make sure the bit change is present. Restore the setting and use SHOWSET to check the original setting.

## METER Test

This test checks the relay magnitude accuracy.

1. As shown in Figure 7.1, connect voltage input terminals VAX, VBX, VCX, VAY, VBY, and VCY together. Apply 67 Vac from those terminals to neutral points VNX and VNY.

2. Use the METER command to inspect measured voltages. The relay generates magnitude measurements in secondary volts, so all six voltages should read 67 volts. Phase differential voltages should be approximately 0 volts.

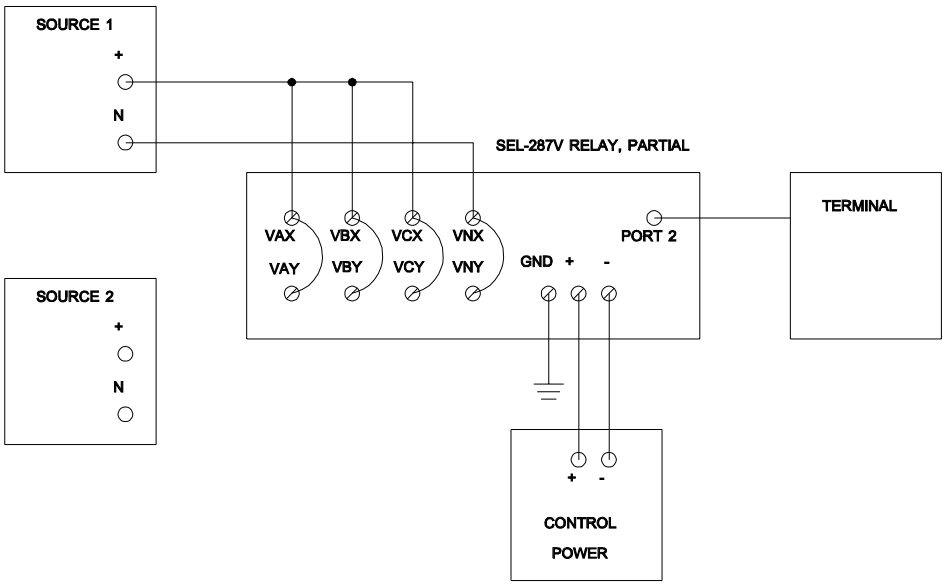


**Figure 7.1: Test Connection #1**

## Instantaneous Overvoltage (59I) Elements

This test checks the operation and accuracy of instantaneous overvoltage elements, X59I and Y59I.

1. Use the SHOWSET command to check the X59I and Y59I settings.

2. Set the relay targets to display Relay Word row 1 by typing **TARGET 1 <ENTER>**.

3. As shown in Figure 7.3, connect Source 1 between VAX and VNX. Connect Source 2 between the other five inputs and two neutrals.

4. Turn the voltage sources on. Adjust Sources 1 and 2 to 67 Vac.

5. Increase Source 1 until the first (X59A) LED illuminates. Make a note of the voltage applied to VAX.

6. Turn the voltage sources off.

7. Test Source X B- and C-phase overvoltage elements by connecting Source 1 to the phase under test and Source 2 to the other five phases. Make sure the appropriate LED(s) illuminate for each test performed.

8. As shown in Figure 7.2, connect the positive output of Source 2 to VAX, VBX, and VCX. Connect the Source 2 neutral to VNX. Connect Source 1 to VAY, VBY, and VCY. Connect Source 1 neutral to VNY.

9. Turn the voltage sources on. Adjust Sources 1 and 2 to 67 Vac.

10. Increase Source 1 until the fourth through eighth LEDs (3Y59, Y59A, Y59B, Y59C, and 3Y59D) illuminate. Make note of the voltage applied to Source Y.

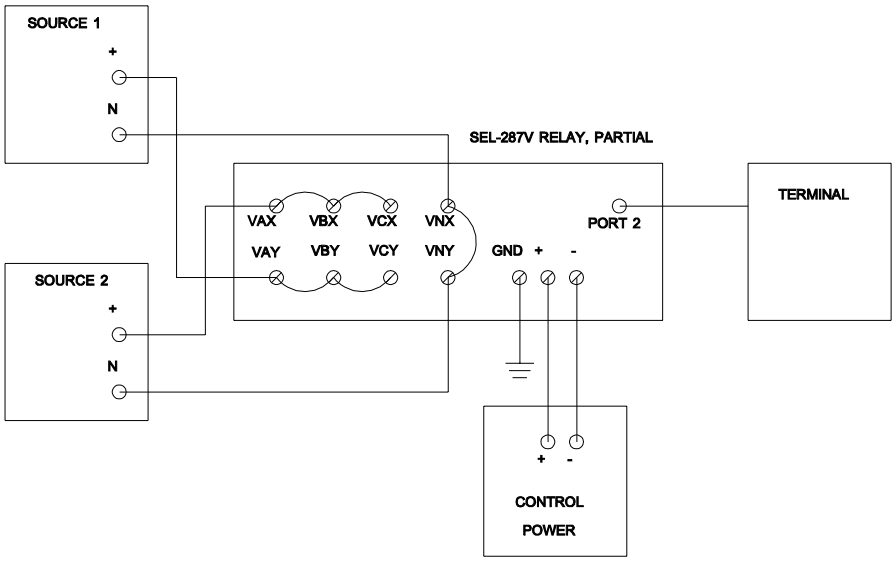


**Figure 7.2: Test Connection #2**

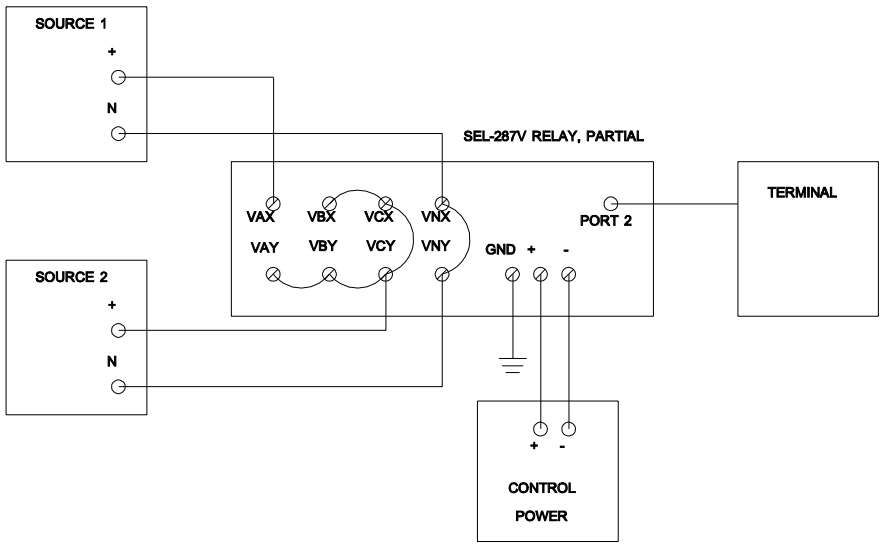


**Figure 7.3: Test Connection #3**

### Definite-Time Overvoltage (59T) Elements

This test checks the operation, timing, and accuracy of the definite-time overvoltage elements, X59T and Y59T.

1. Use the SHOWSET command to check the X59PU, X59D, Y59PU, and Y59D settings.
2. Type **TARGET 3 <ENTER>** to set targets to Relay Word row 3.
3. Using the LOGIC MER command, set all elements to 0 except X59P and Y59P in the MER mask. Set X59T and Y59T equal to 1 in the MT mask.
4. As shown in Figure 7.3, connect Source 1 between VAX and VNX. Connect Source 2 between the other five inputs and two neutrals.
5. Turn the voltage sources on. Adjust Sources 1 and 2 to 67 Vac.
6. Increase Source 1 until the first (X59P) LED illuminates. A moment after LED 1 illuminates, LED 2 illuminates, indicating definite-time delay expiration and X59T assertion. Make note of the voltage applied to VAX.
7. In the test setting group, the MER setting causes event report generation upon pickup. The MT setting causes event report generation upon time out of definite-time overvoltage elements. This test generates two event reports; both are time tagged to the nearest quarter-cycle. Calculate the element time delay using the report times on element pickup and trip.

You can test definite-time overvoltage element response to overvoltages on each phase by connecting Source 1 to the phase under test and Source 2 to the other five phases. Make sure the appropriate LEDs illuminate for each test performed. Set X59T and Y59T equal to 0 in the MT mask when you finish the test. An alternative method for performing this test is given in ***Timed Element Tests*** below.

### Instantaneous Undervoltage (27L) Elements

This test checks the operation and accuracy of the instantaneous undervoltage elements, X27L and Y27L.

1. Use the SHOWSET command to check the X27L and Y27L settings.
2. Set the relay targets to display Relay Word row 2 by typing **TARGET 2 <ENTER>**.
3. As shown in Figure 7.3, connect Source 1 between VAX and VNX. Connect Source 2 between the other five inputs and two neutrals.
4. Turn the voltage sources on. Adjust Sources 1 and 2 to 67 Vac.
5. Decrease Source 1 until the first (X27A) LED illuminates. Make a note of the voltage applied to VAX.
6. Turn the voltage sources off.
7. Test Source X B- and C-phase undervoltage elements by connecting Source 1 to the phase under test and Source 2 to the other five phases. Make sure the appropriate LED(s) illuminate for each test performed.

8. As shown in Figure 7.2, connect the positive output of Source 2 to VAX, VBX, and VCX. Connect the Source 2 neutral to VNX. Connect Source 1 to VAY, VBY, and VCY. Connect the Source 1 neutral to VNY.

9. Turn the voltage sources on. Adjust Sources 1 and 2 to 67 Vac.

10. Decrease Source 1 until the fifth through eighth LEDs (Y27A, Y27B, Y27C, and 3Y27) illuminate. Make note of the voltage applied to Source Y.

### Phase Differential Overvoltage (87) Elements (SEL-287V, SEL-287V-1 Relay)

This test checks the operation and accuracy of the phase differential overvoltage elements, 87A, 87T, and 87H.

1. Use SHOWSET to check the phase differential alarm and trip settings.

2. Set the relay targets to display Relay Word row 5 by typing **TARGET 5 <ENTER>**.

3. As shown in Figure 7.3, connect Source 1 between VAX and VNX. Connect Source 2 between the other five inputs and two neutrals.

4. Turn Sources 1 and 2 on. Adjust the voltage sources to 67 Vac.

5. Execute the KSET command to cancel any minor differences between phase voltage magnitudes. Start this test with the differential voltage of the phase under test at approximately 0 volts. Execute the METER command to verify the differential voltage.

6. Increase Source 1 until the eighth LED (87A) illuminates. The eighth LED indicates the A-phase differential overvoltage element alarm (87AA) pickup. Make note of the voltage applied to VAX.

7. Continue to increase Source 1 until the seventh (87T) LED illuminates. The seventh LED indicates the A-phase differential overoltage element trip (87AT) pickup. Make note of the voltage applied to VAX.

8. Continue to increase Source 1 until the first (87H) LED illuminates. The first LED indicates the A-phase differential overvoltage element trip (87AH) pickup. Make note of the voltage applied to VAX.

9. Turn the voltage sources off.

10. Check the time-delayed phase differential elements by setting both 87A in the MER mask and 87AD in the MT mask. Apply 87AA pickup voltage difference between the Source X and Y voltage inputs. Calculate the time difference between the two event reports. Repeat this test using 87T or 87H in the MER mask and 87TD or 87HD in the MT mask. An alternative method for performing these tests is given in ***Timed Element Tests*** below.

You can test each of the phase differential overvoltage element by connecting Source 1 to the phase under test and Source 2 to the other five phases. Make sure the appropriate LED(s) illuminate for each test performed.

### Phase Differential Overvoltage (87) Elements (SEL-287V-2 Relay)

This test checks the operation and accuracy of the phase differential overvoltage elements, 87A, 87T, and 87H. It is slightly modified from the standard SEL-287V Relay tests to reflect the 87 element differences in the SEL-287V-2 Relay version.

1. Use SHOWSET to check the phase differential alarm and trip settings.
2. Set the relay targets to display Relay Word row 5 by typing **TARGET 5 <ENTER>**.
3. As shown in Figure 7.3, connect Source 1 between VAX and VNX. Connect Source 2 between the other five inputs and two neutrals.
4. Turn Sources 1 and 2 on. Adjust the voltage sources to 67 Vac.
5. Execute the KSET command to cancel any minor differences between phase voltage magnitudes. Start this test with the differential voltage of the phase under test at approximately 0 volts. Execute the METER command to verify the differential voltage.
6. Increase Source 1 until the eighth LED (87A) illuminates. The eighth LED indicates a differential overvoltage element alarm (87A) pickup. Make note of the voltage applied to VAX. This verifies the element for the 87A1P (dV > 0) threshold value.
7. Continue to increase Source 1 until the seventh (87T) LED illuminates. The seventh LED indicates a differential overvoltage element trip (87T) pickup. Make note of the voltage applied to VAX. This verifies the element for the 87T1P (dV > 0) threshold value.
8. Continue to increase Source 1 until the first (87H) LED illuminates. The first LED indicates a differential overvoltage element high-set trip (87H) pickup. Make note of the voltage applied to VAX. This verifies the element for the 87H1P (dV > 0) threshold value.
9. Return Source 1 to the same value as Source 2. Verify dV is approximately zero via the METER command. Repeat the tests of steps 6–8 by lowering the Source 1 voltage. This produces a negative dV and verifies the elements for thresholds 87A2P, 87T2P, and 87H2P.
10. Turn the voltage sources off.
11. Check the time-delayed phase differential elements by setting both 87A in the MER mask and 87A1D in the MT mask. Raise Source 1 voltage to apply the 87A1P pickup voltage difference between the Source X and Y voltage inputs. Calculate the time difference between the two event reports. Repeat this test using 87T or 87H in the MER mask and 87TD or 87HD in the MT mask. An alternative method for performing these tests is given in ***Timed Element Tests*** below.

You can test each of the phase differential overvoltage elements by connecting Source 1 to the phase under test and Source 2 to the other five phases. Make sure the appropriate LED(s) illuminate for each test performed.

### Voltage Control Logic

This test checks the operation and accuracy of the voltage control logic.

1. Use SHOWSET to check the VSS, 59P1, 59P2, 27P1, and 27P2 settings.
2. Set the relay targets to display Relay Word row 4 by typing **TARGET 4 <ENTER>**.

3. Refer to Figure 7.1, but only connect the X voltage inputs. Turn the voltage source on. Adjust Source 1 to 67 Vac.

4. Test the Raise Voltage function. Assert the RE1 contact by applying dc control voltage to terminals 39 and 40. Decrease Source 1 until the second LED (VL1) illuminates. A moment after VL1 asserts, the sixth LED (VLD1) illuminates. Make a note of the voltage applied to Source X. It should equal the 27P1 setting.

5. Test the Lower Voltage function. Assert the LE1 contact by applying dc control voltage to terminals 41 and 42. Increase Source 1 until the first LED (VH1) illuminates. A moment after VH1 asserts, the fifth LED (VHD1) illuminates. Make a note of the voltage applied to Source X. It should equal the 59P1 setting.

6. Turn the voltage source off.

Test the different scheme selection settings as follows. With the settings VSS = I (independent), Scheme 1 operates from Source X voltages. Scheme 2 operates from Source Y voltages. When VSS = I, test 59P1, 27P1, VH1, VHD1, VL1, and VLD1 by using Source X voltages and 59P2, 27P2, VH2, VHD2, VL2, and VLD2 by using Source Y voltages.

When setting VSS = B (better), under normal conditions Source X corresponds to Scheme 1 and Source Y corresponds to Scheme 2. When one source experiences a loss-of-potential condition (X27D or Y27D), both schemes are operated from the source not experiencing a 27D undervoltage condition.

When VSS = B and both sources experience a 27D undervoltage condition, Scheme 1 is driven from Source X, while Scheme 2 is driven from Source Y. If LOPE1 is enabled under these circumstances, Scheme 1 is disabled. Likewise, when LOPE2 is enabled, Scheme 2 is disabled.

When VSS = B, test the voltage control elements with Source X voltage above the X27L settings and Source Y voltage above the Y27L setting. Test 59P1, 27P1, VH1, VHD1, VL1, and VLD1 by using Source X voltages and 59P2, 27P2, VH2, VHD2, VL2, and VLD2 by using Source Y voltages.

When setting VSS = X, Scheme 1 and Scheme 2 are controlled by Source X voltage. Test all voltage control elements by using Source X voltages.

### Voltage Control Instability Logic

This test checks the operation and accuracy of voltage control instability logic.

1. Use SHOWSET to check the VSS, TLD1, TLD2, 59P1, and 59P2 settings.

2. Use the Access Level 2 SET command to set VSS = I, if it is not already.

3. For the VCI bit under test to assert, the test voltage must increase from below the 27P setting to above the 59P setting before TLD expires.

4. Set the relay targets to display Relay Word row 4 by typing **TARGET 4 <ENTER>**.

5. Complete the connections shown in Figure 7.2 and turn the voltage source on. Adjust Source 1 and 2 to 67 Vac.

6. Assert both the RE1 and LE1 inputs by applying dc control voltage to them.

7. Operate the Raise Voltage function. Decrease Source 2 until the second LED (VL1) illuminates. A moment after VL1 asserts, the sixth LED (VLD1) illuminates. Make a note of the voltage applied to Source X. It should equal the 27P1 setting.

8. Set the relay targets to display Relay Word row 5 by typing **TARGET 5 <ENTER>**.

9. Quickly increase the Source 2 voltage to a level above the 59P1 setting. The fifth LED from the left (VCI1) should illuminate for a moment, between VH1 element assertion and TLD1 timer.

10. Repeat using Source 1 and asserting the RE2 and the LE2 inputs by applying dc control voltage to them.

### Timed Element Tests (SEL-287V, SEL-287V-1 Relay)

Testing the relay timers requires an external timer that can be stopped and started for settable conditions. For instance, it is necessary in one test to start the external timer when voltage is applied and stop the external timer when a contact closes.

Table 7.1 lists all timers included in the SEL-287V Relay.

To test a relay timer, refer to Table 7.1 and perform the following steps:

1. Set the timer you are testing to the desired value using the Access Level 2 SET command.

2. Set the mask bit in one of the programmable output contact logic masks by using the Access Level 2 LOGIC command. This bit should be the only one set in that logic mask.

3. Connect the terminals of the mask bit programmed output contact to the external timer stop timer input.

4. Connect Voltage Source X to the relay Source X inputs. Connect VAX, VBX, and VCX to the Voltage Source X positive terminal and VNX to the Voltage Source X neutral terminal. For tests 4 through 7, see Note 1.

5. Connect Voltage Source Y to the relay Source Y inputs. Connect VAY, VBY, and VCY to the Voltage Source Y positive terminal and VNY to the Voltage Source Y neutral terminal. For tests 4 through 7, see Note 1.

6. Turn on the voltage sources and apply pretest Voltage X and pretest Voltage Y to the relay. Table entries containing dashes indicate that the input is not necessary to perform that test.

7. Set the start and stop timer conditions listed in Table 7.1 for the timer.

8. Apply the test voltages listed.

9. Note the test results.

**Table 7.1: Timed Element Tests (SEL-287V, SEL-287V-1 Relay)**

| Test # | Timer Under Test | Mask Bit | Pretest Voltage X | Pretest Voltage Y | Test Voltage X | Test Voltage Y | Start Timer | Stop Timer |
|---|---|---|---|---|---|---|---|---|
| 1 | X59D | X59T | VX=0 | ----- | VX>X59PU | ----- | VX On | Contact Close |
| 2 | Y59D | Y59T | ----- | VY=0 | ----- | VY>Y59PU | VY On | Contact Close |
| 3 | 3Y59 | 3Y59D | ----- | VY>Y59I | ----- | VY=0 | VY Off | Contact Open |
| 4 | 87HP | 87HD | VX>X27L | VY=VX>Y27L | VX=VX | VY=0,0-∅ | VY Off | Contact Close |
| 5 | 87TP | 87TD | VX>X27L | VY=VX>Y27L | VX=VX | VY=0,1-∅ | VY Off | Contact Close |
| 6 | 87AP | 87AD | VX>X27L | VY=VX>Y27L | VX=VX | VY=0,1-∅ | VY Off | Contact Close |
| 7 | 87DO | 87AD | VX>X27L, Y27L | VY=0,1-∅ | VX=VX | VY=VX | VY On | Contact Open |
| 8 | LOPD | LOPD | VX=0 | VY>Y27L | VX>X27L | VY>Y27L | VX On | Contact Open |
| 9 | THP1 | VHD1 | VX=0 | ----- | VX>59P1 | ----- | VX On | Contact Close |
| 10 | THD1 | VHD1 | VX>59P1 | ----- | VX=0 | ----- | VX Off | Contact Open |
| 11 | THP2 | VHD2 | ----- | VY=0 | ----- | VY>59P2 | VY On | Contact Close |
| 12 | THD2 | VHD2 | ----- | VY>59P2 | ----- | VY=0 | VY Off | Contact Open |
| 13 | TLP1 | VLD1 | VX>27P1 | ----- | VX=0 | ----- | VX Off | Contact Close |
| 14 | TLD1 | VLD1 | VX=0 | ----- | VX>27P1 | ----- | VX On | Contact Open |
| 15 | TLP2 | VLD2 | ----- | VY>27P2 | ----- | VY=0 | VY Off | Contact Close |
| 16 | TLD2 | VLD2 | ----- | VY=0 | ----- | VY>27P2 | VY On | Contact Open |
| 17 | A1PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 18 | A2PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 19 | A3PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 20 | A4PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 21 | A4D0 | 3Y59 | ----- | VY>Y59I | ----- | VY=0 | VY Off | Contact Open |
| 22 | A5PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 23 | A5DO | 3Y59 | ----- | VY>Y59I | ----- | VY=0 | VY Off | Contact Open |

**Note 1**: In tests 4 through 7, Voltage Source Y is listed as one phase. To perform these tests, connect Voltage Source Y to one phase of relay Source Y input. Connect Voltage Source X to relay Source X inputs and the remaining two relay Source Y inputs. This connection is similar to the one shown in Figure 7.3.

**Note 2**: In tests 9 through 16, the proper voltage control enable inputs must be asserted to allow the element under test to operate. The table below shows which input to assert before performing each test. Also set VSS = I.

| Input | Tests |
|---|---|
| LE1 | 9 and 10 |
| LE2 | 11 and 12 |
| RE1 | 13 and 14 |
| RE2 | 15 and 16 |

Additionally, the LOPE1 and LOPE2 settings can affect tests 9, 11, 14, and 16. In tests 9 and 14, set LOPE1 = N or use a pretest VX above the X27L setting. In tests 11 and 16, set LOPE2 = N or use a pretest VY above the Y27L setting. If you fail to do so, the time delay measured in tests 9, 11, 14, and 16 includes the LOPD setting time.

**Note 3**: In tests 20 and 21, monitor A4 output contact for time-delay pickup and dropout. In tests 22 and 23, monitor A5 output contact for time-delay pickup and dropout. Mask setting for both tests is for MA4 and MA5 logic masks.

Dashed lines indicate that a source is not used in the test.

## Timed Element Tests (SEL-287V-2 Relay)

Testing the relay timers requires an external timer that can be stopped and started for settable conditions. For instance, it is necessary in one test to start the external timer when voltage is applied and stop the external timer when a contact closes. The test setup is similar to that in Figure 7.3.

Table 7.2 lists all timers included in the SEL-287V-2 Relay.

To test the 87 element timers, refer to tests 4–7 in Table 7.2 and perform the following steps:

1. Set the timer you are testing to the desired value using the Access Level 2 SET command.
2. Set the mask bit in one of the programmable output contact logic masks using the Access Level 2 LOGIC command. This bit should be the only one set in that logic mask.
3. Connect the terminals of the mask bit programmed output contact to the external timer stop timer input.
4. Connect Voltage Source X to the relay Source X inputs. Connect VAX, VBX, VCX, VBY, and VCY to the Voltage Source X positive terminal, and connect VNX and VNY to the Voltage Source X neutral terminal.
5. Connect Voltage Source Y to the remaining relay Source Y input, VAY. Connect VAY to the Voltage Source Y positive terminal and VNY to the Voltage Source Y neutral terminal.
6. Turn the voltage sources on and apply pretest Voltage X and pretest Voltage Y to the relay, as indicated in tests 4–7.
7. Set the start and stop timer conditions listed in Table 7.2 for the timer.
8. Apply the test voltages listed.
9. Note the test results.

**Table 7.2: Timed Element Tests (SEL-287V-2 Relay)**

| Test # | Timer Under Test | Mask Bit | Pretest Voltage X | Pretest Voltage Y | Test Voltage X | Test Voltage Y | Start Timer | Stop Timer |
|---|---|---|---|---|---|---|---|---|
| 1 | X59D | X59T | VX=0 | ----- | VX>X59PU | ----- | VX On | Contact Close |
| 2 | Y59D | Y59T | ----- | VY=0 | ----- | VY>Y59PU | VY On | Contact Close |
| 3 | 3Y59D | 3Y59D | ----- | VY>Y59I | ----- | VY=0 | VY Off | Contact Open |
| 4 | 87HPD | 87HD | VX>X27L | VY=VX>Y27L | VX=VX | VY=0,0-∅ | VY Off | Contact Close |
| 5 | 87TPD | 87TD | VX>X27L | VY=VX>Y27L | VX=VX | VY=0,1-∅ | VY Off | Contact Close |
| 6 | 87APD | 87A1D | VX>X27L | VY=VX>Y27L | VX=VX | VY=0,1-∅ | VY Off | Contact Close |
| 7 | 87DO | 87A1D | VX>X27L,Y27L | VY=0,1-∅ | VX=VX | VY=VX | VY On | Contact Open |
| 8 | LOPD | LOPD | VX=0 | VY>Y27L | VX>X27L | VY>Y27L | VX On | Contact Open |

| Test # | Timer Under Test | Mask Bit | Pretest Voltage X | Pretest Voltage Y | Test Voltage X | Test Voltage Y | Start Timer | Stop Timer |
|---|---|---|---|---|---|---|---|---|
| 9 | THP1 | VHD1 | VX=0 | ----- | VX>59P1 | ----- | VX On | Contact Close |
| 10 | THD1 | VHD1 | VX>59P1 | ----- | VX=0 | ----- | VX Off | Contact Open |
| 11 | THP2 | VHD2 | ----- | VY=0 | ----- | VY>59P2 | VY On | Contact Close |
| 12 | THD2 | VHD2 | ----- | VY>59P2 | ----- | VY=0 | VY Off | Contact Open |
| 13 | TLP1 | VLD1 | VX>27P1 | ----- | VX=0 | ----- | VX Off | Contact Close |
| 14 | TLD1 | VLD1 | VX=0 | ----- | VX>27P1 | ----- | VX On | Contact Open |
| 15 | TLP2 | VLD2 | ----- | VY>27P2 | ----- | VY=0 | VY Off | Contact Close |
| 16 | TLD2 | VLD2 | ----- | VY=0 | ----- | VY>27P2 | VY On | Contact Open |
| 17 | A1PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 18 | A2PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 19 | A3PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 20 | A4PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 21 | A4D0 | 3Y59 | ----- | VY>Y59I | ----- | VY=0 | VY Off | Contact Open |
| 22 | A5PD | 3Y59 | ----- | VY=0 | ----- | VY>Y59I | VY On | Contact Close |
| 23 | A5DO | 3Y59 | ----- | VY>Y59I | ----- | VY=0 | VY Off | Contact Open |

## Input Circuit Test

This test checks contact input operation.

1. Set LTCHE = N by using the Access Level 2 SET command.
2. Set target LEDs to display the contact inputs by typing **TAR 7 <ENTER>**.
3. Apply control voltage to each input and observe that the corresponding target LED turns on. Energizing the ET1 or ET2 input should trigger an event report.
4. Set LTCHE = Y by using the Access Level 2 SET command.
5. Set the target LEDs to display the LTCH bit by typing **TAR 2 <ENTER>**.
6. Apply control voltage to ET2 and observe LTCH LED illumination. Apply control voltage to ET1 and observe that the LTCH LED stays on. The LTCH LED should turn off when you remove control voltage from ET2. Energizing the ET1 or ET2 input with LTCHE=Y should not trigger an event report.

## Output Circuit Test

This test checks contact output operation.

1. Set target LEDs to display contact output states by typing **TAR 8 <ENTER>**.
2. Execute the PULSE n command for each output contact. During the one-second contact closure pulse, observe the appropriate target LED illumination for each output and check continuity between the terminals of the contact under test. Several PULSE n command executions may be required for each contact.

### Serial Port Test

The checkout procedure assumes that you connect a terminal to PORT 2. Set the baud rate of PORT 1 to the same value as that of PORT 2 and switch your terminal from PORT 2 to PORT 1. Make sure you can communicate through this port. If your relay is equipped with front- and rear-panel serial ports, ensure that both operate properly.

### IRIG-B Time Code Input Test

1. Connect a source of demodulated IRIG-B time code to the Auxiliary Port with a series resistor to monitor the current. Adjust the source to obtain an "ON" current of about 10 mA.
2. Execute the IRIG command and make sure the relay clock displays the correct date and time.

**Note:** A recording of the IRIG-B signal passed through a simple demodulator provides a convenient, inexpensive test of the IRIG-B port. Please contact the factory for further details.

### Power Supply Voltage Test

1. Execute the STATUS command and inspect voltage readings for the +5 and ±15 volt supplies.
2. At the Auxiliary Port, use a voltmeter to read +5 and ±12 volt outputs. The 12-volt outputs are derived from the 15-volt supplies using three-terminal regulators.

| SEL-287V |
|---|
| Pin 1: +5 Vdc |
| Pin 4: +12 Vdc |
| Pin 6: –12 Vdc |

3. Compare +5 volt readings from the status report and voltmeter. Voltage difference should not exceed 50 mV; both readings should be within 0.15 volts of 5 volts.
4. The 12-volt supplies should be within 0.5 volts of their nominal values.

## CALIBRATION

Each SEL Relay is factory calibrated. If you suspect that the relay is out of calibration, please contact the factory.

# TROUBLESHOOTING GUIDE

## Inspection Procedure

Complete the following inspection procedure before disturbing the system. After you finish the inspection, proceed to ***Troubleshooting Table***.

1. Measure and record control power voltage at terminals marked + and –.
2. Check to see that the power is on, but do not turn system off if it is on.
3. Measure and record the voltage at all control inputs.
4. Measure and record the state of all output relays.
5. Inspect the cabling to the serial communications ports and be sure a communications device is connected to at least one communications port.

## Troubleshooting Table

### All Front-Panel LEDs Dark

1. Power is off.
2. Blown fuse.
3. Input power not present.
4. Self test failure.
5. Target command improperly set.

**Note:** For 1, 2, 3, and 4, the ALARM relay contacts should be closed.

### System Does Not Respond to Commands

1. Communications device not connected to system.
2. Relay or communications device at incorrect baud rate or other communication parameter incompatibility, including cabling error.
3. Internal ribbon cable connector loose or disconnected.
4. System is processing event record. Wait several seconds.
5. System is attempting to transmit information, but cannot due to handshake line conflict. Check communications cabling.
6. System is in the XOFF state, halting communications. Type **<CTRL>Q** to put system in XON state.

### Tripping Output Relay Remains Closed Following Fault

1. Auxiliary contact inputs improperly wired.
2. Output relay contacts burned closed.
3. Interface board failure.

### No Prompting Message Issued to Terminal Upon Power-Up

1. Terminal not connected to system.
2. Terminal improperly connected to system.
3. Wrong baud rate.
4. Other port designated AUTO in the relay settings.
5. Port time-out interval set to value other than zero.
6. Main board or interface board failure.

### System Does Not Respond to Faults

1. Relay improperly set. Review your settings with SET and LOGIC.
2. Improper test settings.
3. PT input cable wiring error.
4. Analog input cable between transformer-termination and main board loose or defective.
5. Check self-test status with STATUS command.
6. Check input voltages and currents with METER command and TRIGGER and EVENT sequence.

### Terminal Displays Meaningless Characters

1. Baud rate set incorrectly.
2. Check terminal configuration. See ***Section 3: Communications***.

### Self-Test Failure: +5 Volts

1. Power supply +5 volt output out of tolerance. See STATUS command.
2. A/D converter failure.

### Self-Test Failure: +15 Volts

1. Power supply +15 volt output out of tolerance. See STATUS command.
2. A/D converter failure.

### Self-Test Failure: –15 Volts

1. Power supply –15 volt output out of tolerance. See STATUS command.
2. A/D converter failure.

### Self-Test Failure: Offset

1. Offset drift. Adjust offsets.
2. A/D converter drift.
3. Loose ribbon cable between transformers and main board.

### Self-Test Failure: ROM Checksum

1. EPROM failure. Replace EPROMs.

### Self-Test Failure: RAM

1. Failure of static RAM IC. Replace RAM.

### Self-Test Failure: A/D Converter

1. A/D converter failure.
2. RAM error not detected by RAM test.

### Alarm Contacts Closed

1. Power is off.
2. Blown fuse.
3. Power supply failure.
4. Improper EPROMs or EPROM failure.
5. Main board or interface board failure.

## FIRMWARE UPGRADE INSTRUCTIONS

SEL may occasionally offer firmware upgrades to improve the performance of your relay. These instructions explain how to install new firmware.

The modifications require that you power-down the relay, remove its front panel, pull out the drawout unit, exchange several integrated circuit chips, and reassemble the relay. If you do not wish to perform the modifications yourself, we can assist you. Simply return the relay and integrated circuit chips to us. We will install the new chips and return the unit to you within a few days.

**CAUTION**

The relay contains devices sensitive to electrostatic discharge (ESD). When working on the relay with front or top cover removed, work surfaces and personnel must be properly grounded or equipment damage may result. If your facility is not equipped to work with these components, we recommend that you return the relay to SEL for firmware installation.

1. If the relay is in service, disable its control functions. Turn control power to the relay off.
2. Remove the relay front panel by unscrewing the five front-panel screws. With the front panel removed, you can see the aluminum drawout chassis. The main board is attached to the top of the drawout chassis. The power supply and transformer assembly are attached to the bottom of the relay chassis.
3. Disconnect the power supply and transformer secondary cables from the underside of the drawout assembly.
4. Remove the drawout assembly by pulling the spacers on the bottom of the drawout chassis. You should be able to remove the assembly with your fingers. Because steps 5 and 6 involve handling devices and assemblies sensitive to electrostatic discharge (ESD), perform these steps at an ESD-safe work station. This will help prevent possible damage by electrostatic discharge.
5. Note the orientation of the ICs to be replaced. Use a small screwdriver to pry the indicated ICs free from their sockets. Be careful not to bend the IC pins or damage adjacent components.
6. Carefully place the new ICs in the appropriate sockets. Check the orientation of the ICs. Be sure that each IC is in its corresponding socket. Look for IC pins that bent under or did not enter a socket hole.
7. Slide the drawout assembly into the relay chassis. Using your fingers, push the assembly in until the front of the assembly is flush with the front of the relay chassis. Reconnect the power supply and transformer secondary cables to the receivers on the underside of the drawout assembly. Replace the relay front panel.
8. With breaker control disabled, turn relay power on and enter your settings. Execute the STATUS, METER, and TRIGGER commands to ensure that all functions are operational. Set and record your Access Level 1 and 2 passwords and the date and time. The relay is now ready to resume protective functions.

## FACTORY ASSISTANCE

We appreciate your interest in SEL products and services. If you have questions or comments, please contact us at:

Schweitzer Engineering Laboratories, Inc.
2350 NE Hopkins Court
Pullman, WA USA 99163-5603
Tel: (509) 332-1890
Fax: (509) 332-7990
Internet: www.selinc.com

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# TABLES



# FIGURES

# APPENDIX A: FIRMWARE VERSIONS

Firmware part numbers and revision numbers are identical for both SEL-287V and SEL-187V relays. This manual covers SEL relays that contain firmware bearing the following part numbers and revision numbers:

| Firmware Part/Revision No. | Description of Firmware |
|---|---|
| Firmware for Revision 4, 287V/187V Main Board Configurations | |
| | This firmware differs from previous versions as follows:<br>– New setting range for the RINGS setting (-30 to 30, excluding 0).<br>– Added functionality that permits the user to prevent the relay from writing the new year to EEPROM at midnight every New Year's Eve, which disables the relay for approximately 12 cycles. |
| SEL-287V-R501-D990319 | 50 Hz, ABC rotation, standard filter. |
| SEL-187V-R406-D990319 | 60 Hz, ABC rotation, standard filter. |
| SEL-187V-1-R401-D990319 | 60 Hz, ABC rotation, fast filter. |
| SEL-287V-2-R401-D990319 | 60 Hz, ABC rotation, standard filter, signed voltage differential. |
| SEL-287V-R500-D950425 | 50 Hz, standard element operation. |
| SEL-187V-R405-D940820 | No distinct difference from previous revision. |
| SEL-187V-1-R400-D940820 | Faster element operation, slightly lower pickup accuracy. |
| SEL-287V-2-R400-D970814 | Modified voltage differential logic and settings (above/below tap). |
| Past Versions | |
| SEL-187V-R404 | No distinct difference from previous version. |
| SEL-187V-R403 | Timers were added for the A1, A2, and A3 contacts. |
| SEL-187V-R402 | No distinct difference from previous version. |
| SEL-187V-R401 | No distinct difference from previous version. |
| SEL-187V-R400 | No distinct difference from previous version. |

To find the firmware revision number in your relay, obtain an event report (which identifies the firmware) by using the EVENT command. This is an FID number with the Part/Revision number in bold:

FID=**SEL-187V-R404-**V6P1-D940320-E2

or

FID=**SEL-187V-1-R404-**V6P2-D940820-E2

or

FID=**SEL-287V-R500-**V5P1-D950425-E2

For a detailed explanation of the FID refer to ***Section 4: Event Reporting***. For more information about revisions, contact SEL.

# APPENDIX B: INTERNAL DIAGRAM

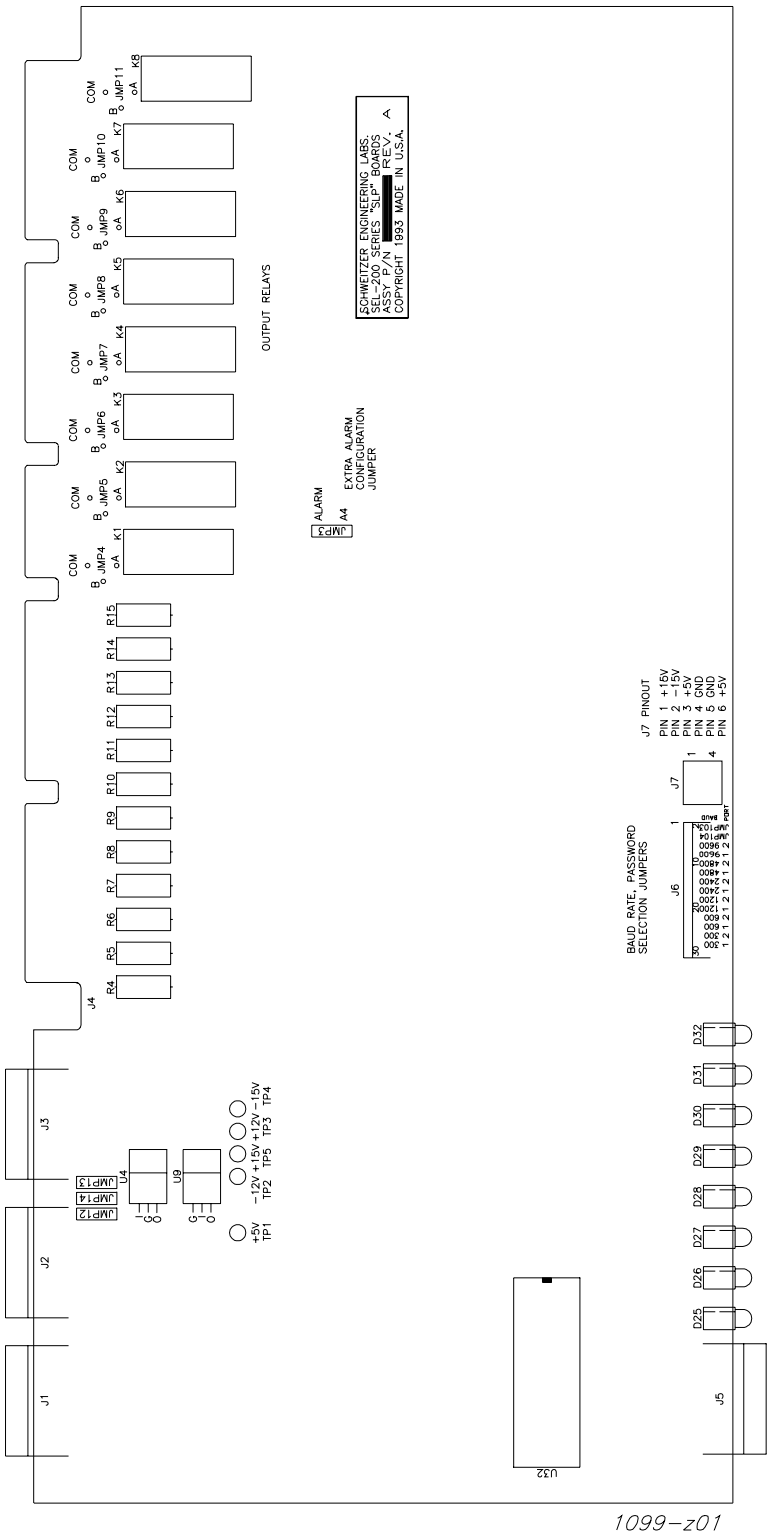



**Figure B.1: SEL-200 Series Main Board Troubleshooting Test Points and Jumper Locations**

# APPENDIX C: SEL-187V RELAY INFORMATION

## GENERAL SPECIFICATIONS

| | |
|---|---|
| **Voltage Inputs** | 0–150 Vac rms line-to-neutral |
| **Output Contacts** | 30 A make per IEEE C37.90<br>6 A carry continuously, MOV protection provided |
| **Optoisolated Input Ratings** | 24 Vdc: 15 – 30 Vdc; 4 mA at nominal voltage<br>48 Vdc: 30 – 60 Vdc; 4 mA at nominal voltage<br>125 Vdc: 80 –150 Vdc; 4 mA at nominal voltage<br>250 Vdc: 150 –300 Vdc; 4 mA at nominal voltage |
| **Power Supply** | 24/48 Volt: 20–60 Vdc; 12 watts<br>125/250 Volt: 85–350 Vdc or 85–264 Vac<br>10 watts nominal, 14 watts max. (all output relays energized) |
| **Time Code Input** | Relay accepts demodulated IRIG-B time code |
| **Communications** | Two EIA-232 serial communications ports |
| **Dimensions** | 5.25" x 19.0" x 14.5" (13.34 cm x 48.26 cm x 36.83 cm) (H x W x D)<br>Depth "D" is to end of the rear-panel terminal blocks |
| **Mounting** | Available in horizontal and vertical mounting configurations |
| **Dielectric Strength** | V inputs: 2500 Vac for 10 seconds<br>Other: 3100 Vdc for 10 seconds (excludes EIA-232) |
| **Operating Temperature** | –40° to +158°F (–40° to +70°C) |
| **Environment** | IEC 68-2-30 Temperature/Humidity Cycle Test - six day (type tested) |
| **Interference Tests** | IEEE C37.90 SWC Test (type tested); IEC 255-6 Interference Test (type tested) |
| **Impulse Tests** | IEC 255-5 0.5 Joule, 5000 Volt Test (type tested) |
| **RFI Tests** | Type tested in field from a quarter-wave antenna driven by 20 watts at 150 MHz and 450 MHz, randomly keyed on and off one meter from relay |
| **ESD Test** | IEC 801-2 Electrostatic Discharge Test (type tested) |
| **Unit Weight** | 21 pounds (9.1 kg) |
| **Shipping Weight** | 30 pounds (13.6 kg), including one instruction manual |

## INSTALLATION

### Mounting

The relay is designed for mounting by its front vertical flanges in a 19" vertical relay rack. It may also be mounted semi-flush in a switchboard panel. Use four #10 screws for mounting. Front- and rear-panel drawings are included in this section.

### Frame Ground Connection

Connect the terminal marked GND (35 or 36) on the rear panel to frame ground for safety and performance. These terminals connect directly to the chassis ground of the instrument.

### Power Connections

Connect terminals marked + (37) and – (38) on the rear panel to a source of control voltage. Control power passes through these terminals to a fuse and toggle switch, if the unit has one. The power continues through a surge filter and connects to the switching power supply. Control power circuitry is isolated from the frame ground.

### Secondary Circuits

The relay presents a very low burden to the secondary current and potential circuits. Each current and voltage circuit is independent of the other circuits; there is no interconnection of current or voltage circuits inside the instrument.

The relay requires difference-voltage potentials that must be obtained from voltage transformers on both sides of the circuit breaker if flashover and thermal protection functions are to be used.

### Control Circuits

The control inputs are dry. For example, to assert the ET1 input, you must apply control voltage to the ET1 input terminals. Each input is individually isolated, and a terminal pair is brought out for each input. There are no internal connections between control inputs.

Control outputs are dry relay contacts rated for tripping duty. A metal-oxide varistor (MOV) protects each contact.

### Communications Circuits

Connections to the two EIA-232 serial communications ports are made via the two nine-pin connectors labeled PORT 1 and PORT 2 on the rear panel. Pins 1 and 9 connect directly to frame (chassis) ground.


Do not rely upon pins 1 and 9 for safety grounding, since their current-carrying capacity is less than control-power short circuit current and protection levels.

The communications circuits are protected by low-energy, low-voltage MOVs and passive RC filters. You can minimize communications-circuit difficulties by keeping the length of the EIA-232 cables as short as possible. Lengths of 12 feet or less are recommended, and the cable length

should never exceed 100 feet. Use shielded communications cable for lengths greater than 10 feet. Modems are required for communications over long distances.

Route the communications cables well away from the secondary and control circuits. Do not bundle the communications wiring with secondary or control circuit wiring. If these wires are bundled, switching spikes and surges can cause noise in the communications wiring. This noise may exceed the communications logic thresholds and introduce errors. Also route the IRIG-B clock cable away from the control wiring and secondary circuits.

## Jumper Selection

Communication control jumpers are on the front edge of the main board. They are accessed easily by removing the top cover or front panel.

### EIA-232 Jumpers

Jumper block P105 provides EIA-232 baud rate selection. Available baud rates are 300, 600, 1200, 2400, 4800, and 9600. To select a baud rate for a particular port, place the jumper so it connects a pin labeled with the desired port to a pin labeled with the desired baud rate.


**CAUTION**

Do not select two baud rates for the same port. This can damage the baud rate generator.

### Password Protection Jumper

Put JMP103 in place to disable password protection. This feature is useful if passwords are not required or when passwords are forgotten.

### PULSE n Command Enable Jumper

When JMP104 is in place, PULSE n command is enabled. If you remove jumper JMP104, PULSE command execution results in the error message: “Command Aborted.”

### Output Contact Soldered Wire Jumpers

Output contacts, except TRIP, can be configured as “a” or “b” contacts with soldered wire jumpers K501 through K506 (each jumper has positions A and B). The output contact/soldered wire jumper correspondence is as follows:

| Output Contact | Jumper |
|---|---|
| TRIP (terminals 1, 2) | JMP11 |
| TRIP (terminals 3, 4) | JMP10 |
| CLOSE | JMP9 |
| A1 | JMP8 |
| A2 | JMP7 |
| A3 | JMP6 |
| A4 | JMP5 |
| ALARM | JMP4 |

### Optoisolated Input Control Voltage Jumpers

The SEL-187V Relay logic inputs have been improved to prevent operation of the logic input due to the conditions described in ***SEL UPDATE 94.10 SEL-100 Series Relay Direct Trip Input Operation***. If you would like a copy of ***SEL UPDATE 94.10***, please contact the SEL factory.

The new interface board also provides field selectable input voltage selection. The operating voltages and jumper selection for each logic input are shown in the table below.

| | Relay Terminals | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 39/40 | | 41/42 | | 43/44 | | 45/46 | | 47/48 | | 49/50 | |
| Control Voltage | JMP11 | JMP12 | JMP9 | JMP10 | JMP7 | JMP8 | JMP5 | JMP6 | JMP3 | JMP4 | JMP1 | JMP2 |
| 250 V | | | | | | | | | | | | |
| 125 V | | ● — ● | | ● — ● | | ● — ● | | ● — ● | | ● — ● | | ● — ● |
| 48 V | ● — ● | ● — ● | ● — ● | ● — ● | ● — ● | ● — ● | ● — ● | ● — ● | ● — ● | ● — ● | ● — ● | ● — ● |

## IRIG-B Installation

To synchronize the internal time clock to a source of demodulated IRIG-B time code (e.g., from a satellite clock), connect the time source to the auxiliary input connector on the rear panel. Pin definitions appear in Table C.1.

**Table C.1: AUX INPUT Pin Definitions**

| Pin | Name | Description |
|---|---|---|
| 2 | IRIGIN HI | Positive IRIG-B input |
| 3 | IRIGIN LOW | Negative IRIG-B input |
| 6 | +5 | * |
| 7 | +12 | * |
| 8 | –12 | * |
| 1,5,9 | GND | Ground for ground wires and shields |

* Consult the factory before using these power supply outputs

The actual IRIG-B input circuit is a 56-ohm resistor in series with an optocoupler input diode. The input diode has a forward drop of about 1.5 volts. Driver circuits should put approximately 10 mA through the diode when "on."

The IRIG-B serial data format consists of a one-second frame containing 100 pulses and divided into fields. The relay decodes the second, minute, hour, and day fields and sets the internal relay clock accordingly.

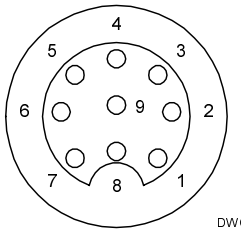
When IRIG-B data acquisition is activated either manually (with the IRIG command) or automatically, two consecutive frames are taken. The older frame is updated by one second and the two frames are compared. If they do not agree, the relay considers the data erroneous and discards it.

The relay reads the time code automatically about once every five minutes. The relay stops IRIG-B data acquisition 10 minutes before midnight on New Year's Eve so the relay clock may implement the year change without interference from the IRIG-B clock. Ten minutes after midnight, the relay restarts IRIG-B data acquisition.

## EIA-232 Installation

The following information contains specific details regarding communications port pinouts.

Figure C.1 shows the pin number convention for the nine-pin (EIA-232) port connectors. The following cable listings show several types of EIA-232 cables. These and other cables are available from SEL. Cable configuration sheets are also available at no charge for a large number of devices. Contact the factory for more information.




(female chassis connector, as viewed from outside rear panel)

**Figure C.1: Nine-Pin Connector Pin Number Convention**

Table C.2 lists port pin assignments and signal definitions.

**Table C.2: SEL-187V Relay Serial Port Connector Pin**

| Pin | Name | Description |
|---|---|---|
| 2 | TXD | Transmit data output. |
| 3 | RTS | The relay asserts this line under normal conditions. When its received-data buffer is full, the line deasserts until the buffer has room to receive more data. Connected devices should monitor RTS (usually with their CTS input) and stop transmitting characters whenever the line deasserts. If transmission continues, data may be lost. |
| 4 | RXD | Receive data input. |
| 5 | CTS | The relay monitors CTS and transmits characters only when CTS is asserted. |
| 6 | +5 volts | |
| 7 | +12 volts | |
| 8 | –12 volts | |
| 1,9 | GND | Ground for ground wires and shields. |

## EIA-232 Cables

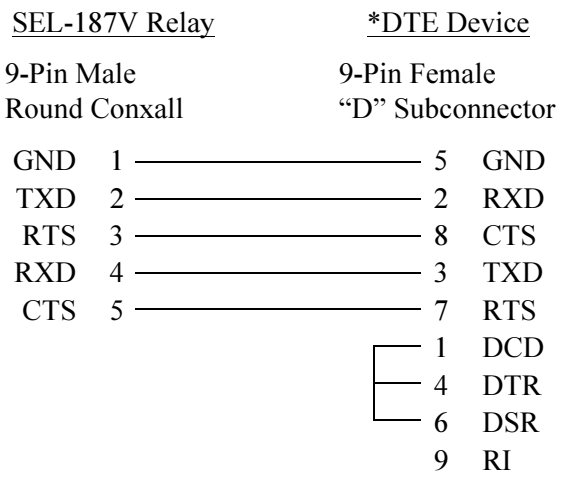
Cable 123

| SEL-187V Relay | | *DTE Device | |
|---|---|---|---|
| 9-Pin Male Round Conxall | | 25-Pin Male "D" Subconnector | |
| GND | 1 | 7 | GND |
| TXD | 2 | 3 | RXD |
| RTS | 3 | 5 | CTS |
| RXD | 4 | 2 | TXD |
| CTS | 5 | 4 | RTS |
| GND | 9 | 1 | GND |
| | | 6 | DSR |
| | | 8 | DCD |
| | | 20 | DTR |

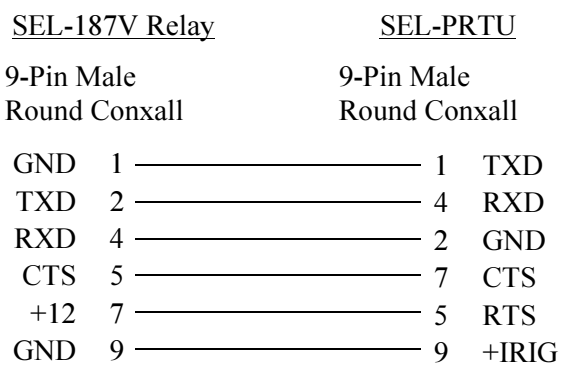
Cable 422

| SEL-187V Relay | | **DCE Device | |
|---|---|---|---|
| 9-Pin Male Round Conxall | | 25-Pin Male "D" Subconnector | |
| GND | 1 | 7 | GND |
| TXD | 2 | 2 | TXD (IN) |
| RTS | 3 | 20 | DTR (IN) |
| RXD | 4 | 3 | RXD (OUT) |
| CTS | 5 | 8 | CD (OUT) |
| GND | 9 | 1 | GND |

Cable 134




Cable 331A




* DTE = Data Terminal Equipment (Computer, Terminal, Printer, etc.)
** DCE = Data Communications Equipment (Modem, etc.)

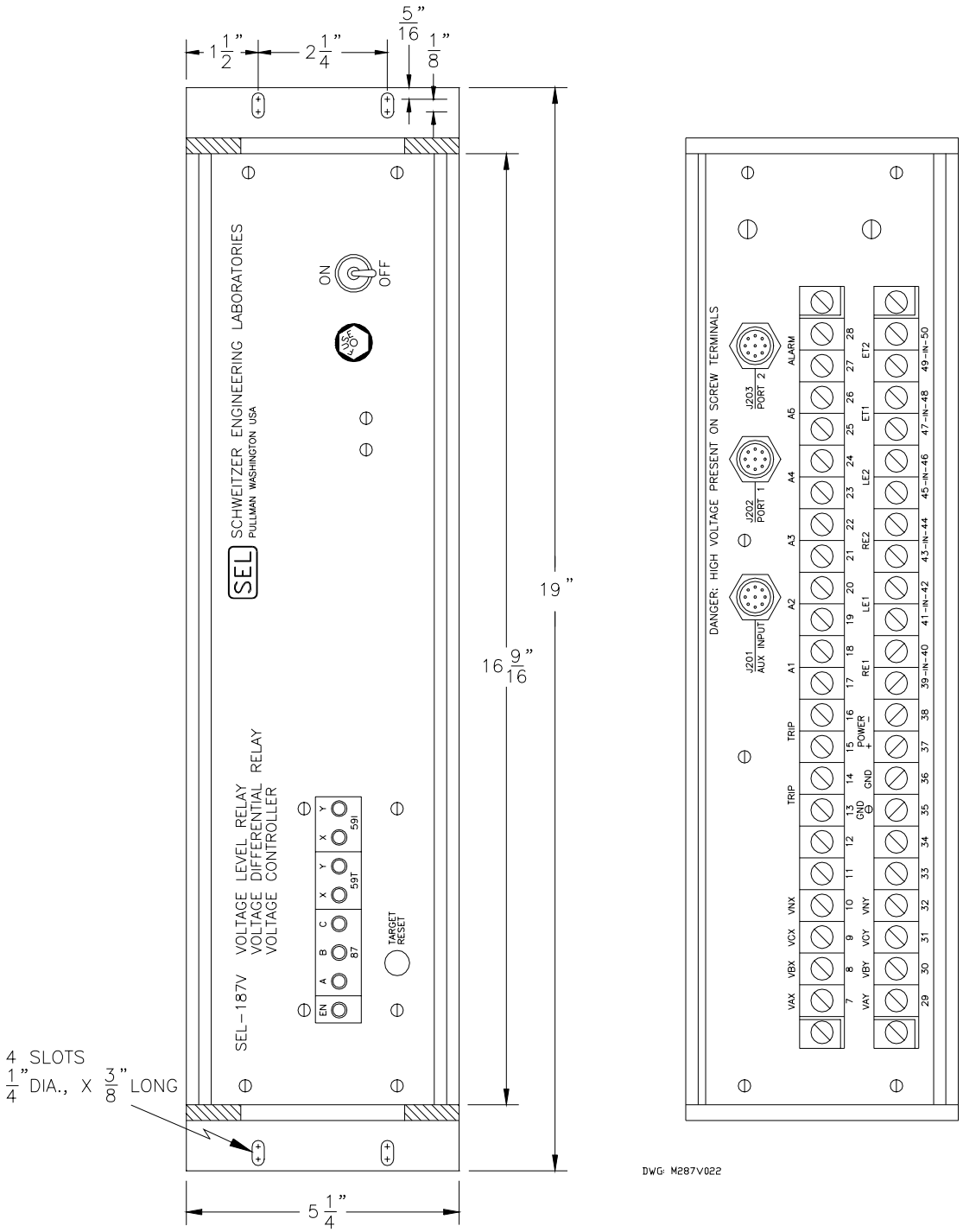



**Figure C.2: Horizontal Front- and Rear-Panel Drawings**

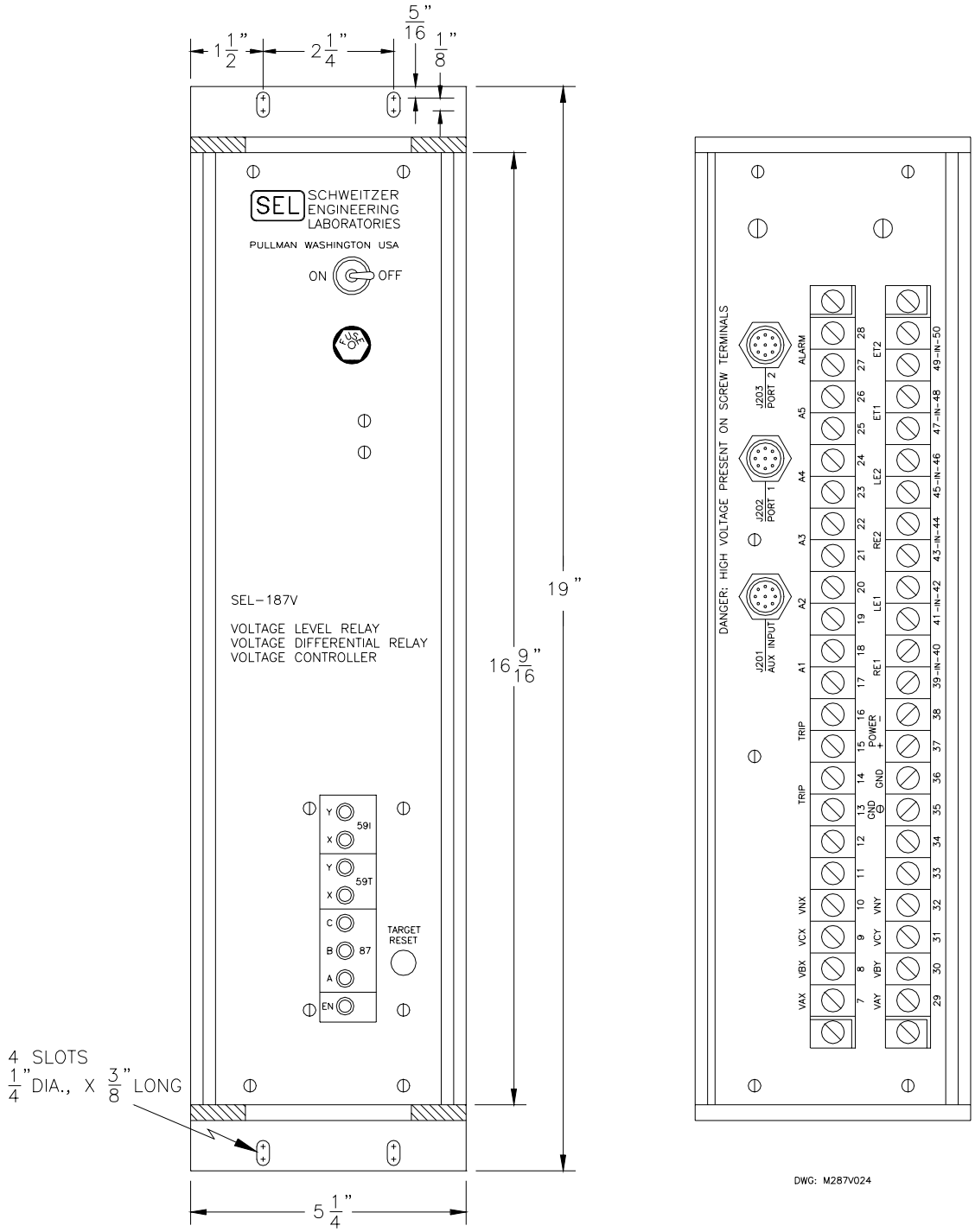



**Figure C.3: Vertical Front- and Rear-Panel Drawings**

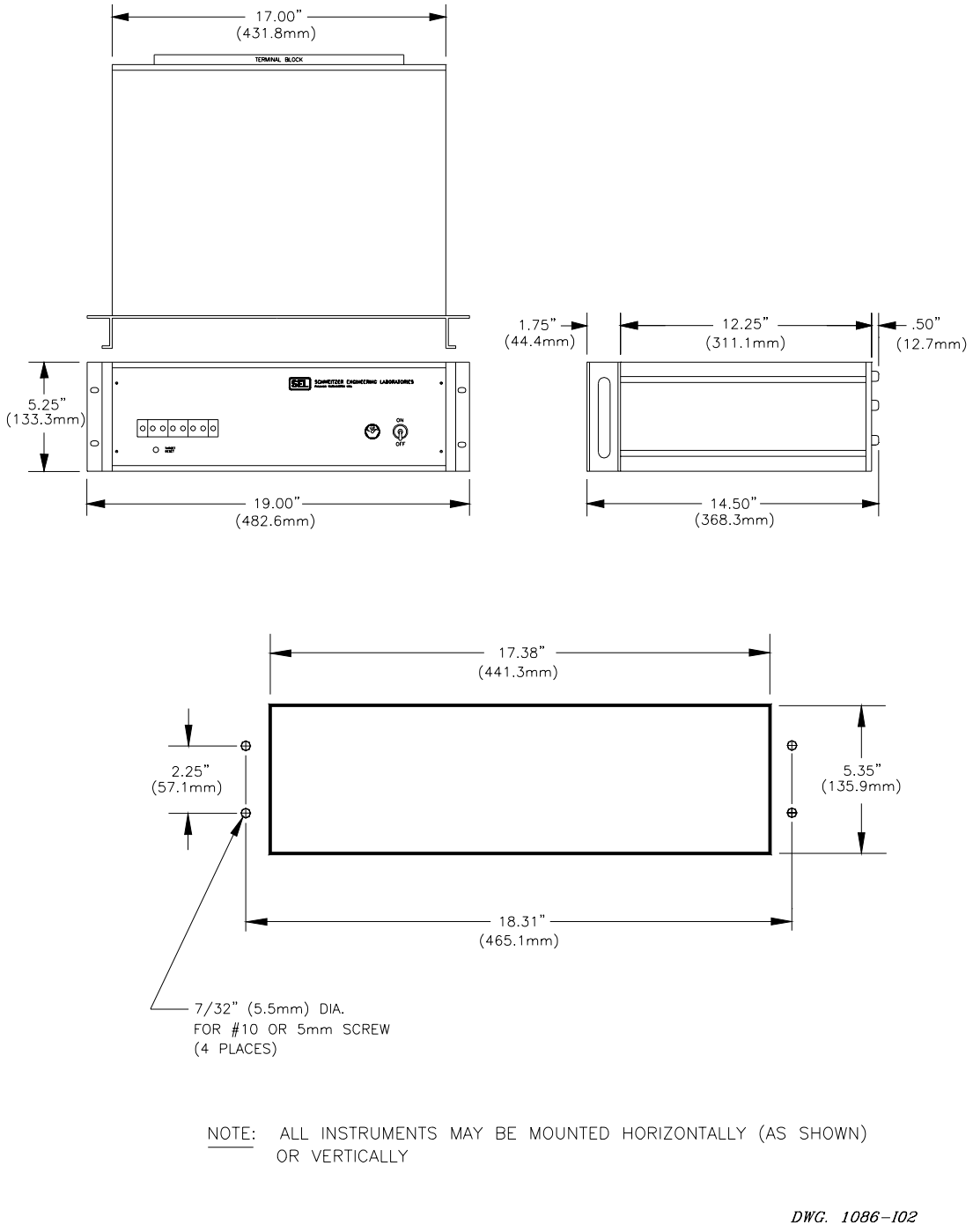



**Figure C.4: Relay Dimensions, Panel Cutout, and Drill Plan**

## FIRMWARE UPGRADE INSTRUCTIONS

SEL may occasionally offer firmware upgrades to improve the performance of your relay. These instructions explain how to install new firmware.

The modifications require that you power-down the relay, remove its front panel, pull out the drawout unit, exchange several integrated circuit chips, and reassemble the relay. If you do not wish to perform the modifications yourself, we can assist you. Simply return the relay and integrated circuit chips to us. We will install the new chips and return the unit to you within a few days.

**CAUTION**

The relay contains devices sensitive to electrostatic discharge (ESD). When working on the relay with front or top cover removed, work surfaces and personnel must be properly grounded or equipment damage may result. If your facility is not equipped to work with these components, we recommend that you return the relay to SEL for firmware installation.

1. If the relay is in service, disable its control functions.
2. Turn control power to the relay off.
3. Remove the front panel by unscrewing the four front-panel screws (one in each corner).
4. With the front panel leaning forward, you can see the aluminum drawout chassis. The main board is attached to the top of the drawout chassis. The power supply and interface board are attached to the bottom of the drawout chassis. Several ribbon cables connect the boards to each other and to other portions of the relay.
5. Disconnect the analog input ribbon cable (the right-most cable) from the main board.
6. The front-panel display cable connects the relay interface board to the front-panel display board. It is located on the left side of the front panel. Disconnect this cable from the display board.
7. Two hex head screws hold the drawout chassis in place. These screws are on the bottom of the chassis in each front corner. Remove both screws.
8. Remove the drawout assembly by pulling the spacers on the bottom of the drawout chassis. You should be able to remove the assembly with your fingers.
9. Because steps 10 through 12 involve handling devices and assemblies sensitive to electrostatic discharge (ESD, perform these steps at an ESD-safe work station. This will help prevent possible damage by electrostatic discharge.
10. Note the orientation of the ICs to be replaced. Use a small screwdriver to pry the indicated ICs free from their sockets. Be careful not to bend the IC pins or damage adjacent components.
11. Carefully place the new ICs in the appropriate sockets.
12. Check the orientation of the ICs. Be sure that each IC is in its corresponding socket. Look for IC pins that bent under or did not enter a socket hole.
13. Slide the drawout assembly back into the relay chassis. Using your fingers, push the assembly in until the retaining screw holes in the drawout assembly align with corresponding holes in the relay chassis.
14. Install the retaining screws and reconnect the two ribbon cables.

15. With breaker control disabled, turn relay power back on and enter your settings. Execute the STATUS, METER, and TRIGGER commands to ensure that all functions are operational. Set and record your Access Level 1 and 2 passwords and the date and time. The relay is now ready to resume protective functions.

16. Please return the old ICs to Schweitzer Engineering Laboratories in the same packing materials. New chips are shipped with a mailing label to simplify this process. When we receive the old parts, we will record a firmware upgrade for each of your relays.

# APPENDIX D: ONEBUS: PROGRAM TO COMPUTE TEST SET SETTINGS FOR TESTING DISTANCE RELAYS

The BASIC program in this note determines voltages and currents that would appear on distance relay terminals for ground and phase faults on a radial system with source impedance at the same angle as line impedance. It is useful in determining test voltage and current settings for SEL distance relays and fault locating equipment.

The program was initially designed to run on a TRS-80 Model 100 briefcase computer but may be installed on virtually any personal computer or laptop.

The program first prompts you for the positive- and zero-sequence impedances of the transmission line. Enter the data in secondary ohms for the entire length of the protected line.

Next, you may enter fault resistance, which is used in the ground-fault computations.

Enter source impedance as a per-unit value with a base of the previously entered transmission line data. For example, if the radial system has a source impedance of about 10 percent of the entered line impedance, enter 0.1 for the per-unit distance from the source to the bus.

Specify the distance from the bus to the fault as a fraction of the total line length. To obtain the voltages and currents for a fault one-half the way down the line from the bus, enter 0.5 for the distance from the bus to the fault.

After you enter these data, the program begins computations. The display then shows voltages and currents for both an AG and BC fault. These data can be entered into any active test source.

The bottom line of the display offers you a choice of entering new impedance data (I), changing the distance from the source to the bus (B), specifying a new fault location (F), or quitting (Q).

```
1     REM SCHWEITZER ENGINEERING LABORATORIES, INC.
2     REM 2350 NE Hopkins Court
3     REM Pullman, WA  99163-5603
4     REM
10    REM COMPUTE DOBLE SETTINGS FOR A ONE-BUS SYSTEM
20    REM HOMOGENEOUS SYSTEM
30    REM SOURCE VOLTS= 67 L-N
40    REM
50    REM ENTER IMPEDANCES FOR 100% OF LINE
60    INPUT "ENTER Z1: R,X";R1,S1
70    INPUT "ENTER Z0: R,X";R0,S0
75    INPUT "ENTER RF FOR GND FLTS";RF
80    REM
90    REM ENTER BUS LOC. FROM SOURCE
100   INPUT "DIST SOURCE TO BUS (PU OF LINE)";S
120   INPUT "DIST BUS TO FAULT (PU OF LINE)";F
130   REM
140   REM  PHASE A TO GROUND
150   REM COMPUTE POS SEQ CURRENT
160   X = R0+2*R1: Y = S0+2*S1
170   R3 = R1-R0:   S3 = S1-S0
180   AR=1/(S+F):  AI=0
190   BR=X      :  BI=Y
195   BR=BR+3*RF/(S+F)
200   GOSUB 2000
210   I = RR    :   J = RI
220   IA = 3*67*I:  JA=3*67*J
225   IB=0:JB=0:IC=0:JC=0
230   AR=X:AI=Y:BR=I:BI=J
232   GOSUB 1000
234   UA=67*(1-S*RR):VA=67*(-S*RI)
240   AR=R3      :AI=S3
250   BR=I       :BI=J
260   GOSUB 1000
270   TR=S*RR    :TS=S*RI
280   UB=67*(-0.5+TR)
290   VB=67*(-SQR(3)/2+TS)
300   UC=67*(-0.5+TR)
310   VC=67*(SQR(3)/2+TS)
315   FF$="A-G"
320   GOSUB 4041
500   REM  B-C FAULT
510   AR=1: AI=0
520   BR=2*R1*(S+F):BI=2*S1*(S+F)
530   GOSUB 2000
540   I=RR:J=RI
550   IA=0:JA=0
560   AR=I:AI=J:BR=0:BI=-67*SQR(3)
570   GOSUB 1000
580   IB=RR:JB=RI:IC=-IB:JC=-JB
590   UA=67:VA=0
600   AR=I:AI=J:BR=S*R1:BI=S*S1
610   GOSUB 1000
620   AR=RR:AI=RI:BR=0:BI=SQR(3)
630   GOSUB 1000
635   TR=RR:TS=RI
640   UB=67*(-0.5+TR)
650   VB=67*(-SQR(3)/2+TS)
660   UC=67*(-0.5-TR)
670   VC=67*(0.5*SQR(3)-TS)
675   FF$="B-C"
680   GOSUB 4041
900   INPUT "IMP BUS FAULT OR QUIT (I,B,F,Q)";A$
910   IF A$ = "I" THEN GOTO 50
920   IF A$ = "B" THEN GOTO  75
930   IF A$ = "F" THEN GOTO 120 ELSE GOTO 999
999   END
1000  REM MULT SUBROUTINE
1010  REM AR,AI * BR,BI = RR,RI
1020  RR=AR*BR-AI*BI
1030  RI=AI*BR+AR*BI
1040  RETURN
2000  REM DIVISION SUBROUTINE
2010  REM AR,AI / BR,BI = RR,RI
2020  D = BR*BR + BI*BI
2030  RR = AR*BR + AI*BI
2040  RR = RR/D
2050  RI = BR*AI - AR*BI
2060  RI = RI/D
2070  RETURN
3000  REM RECT TO POLAR CONV
3010  REM AR,AI, TO RH, TH
3020  PI = 3.14159265358
3030  IF (AR=0 AND AI=0) THEN    RH=0: TH=0: RETURN
3040  IF (AR=0 AND AI>0) THEN    RH=AI: TH=90:RETURN
3050  IF (AR=0 AND AI<0) THEN RH=-AI: TH=-90: RETURN
3060  IF (AR>0) THEN TH=(180/PI)*ATN(AI/AR)
3070  IF (AR<0) THEN TH=(180/PI)*ATN(AI/AR)+180
3080  IF TH>180 THEN TH = TH-360
3090  RH=SQR(AR*AR+AI*AI)
3100  RETURN
4041  AR=UA:AI=VA:GOSUB 3000
4042  UA=RH:VA=TH
4043  AR=UB:AI=VB:GOSUB 3000
4044  UB=RH:VB=TH-VA
4045  AR=UC:AI=VC:GOSUB 3000
4046  UC=RH:VC=TH-VA
4047  AR=IA:AI=JA:GOSUB 3000
4048  IA=RH:JA=TH-VA
4049  AR=IB:AI=JB:GOSUB 3000
4050  IB=RH:JB=TH-VA
4055  AR=IC:AI=JC:GOSUB 3000
4060  IC=RH:JC=TH-VA
4061  VA=0
4100  PRINT " VA   VB   VC   IA   IB   IC"
4130  PRINT USING"##.# ";UA;UB;UC;IA;IB;IC,
4132  PRINT FF$
4140  PRINT USING"#### ";VA;VB;VC;JA;JB;JC
4150  RETURN
```

# SEL-287V VOLTAGE DIFFERENTIAL RELAY COMMAND SUMMARY

## ACCESS LEVEL 0 COMMANDS

**ACCESS** Answer password prompt (if password protection is enabled) to enter Access Level 1. Three unsuccessful attempts pulse ALARM relay closed for one second.

## ACCESS LEVEL 1 COMMANDS

**2ACCESS** Answer password prompt (if password protection is enabled) to enter Access Level 2. This command always pulses the ALARM relay.

**DATE m/d/y** Show or set date. DAT 2/3/90 sets date to Feb. 3, 1990. IRIG-B time-code input overrides existing month and date settings. ALARM contacts pulse when year entered differs from year stored.

**EVENT** Show event record. EVE 1 shows newest event; EVE 12 shows oldest.

**HISTORY** Show DATE, TIME, EVENT, TARGETS for the last 12 events.

**IRIG** Force immediate attempt to synchronize internal relay clock to time-code input.

**METER** Display secondary and difference voltages.

**QUIT** Return control to Access Level 0; return target display to relay targets.

**SHOWSET** Display settings without affecting them.

**STATUS** Show self-test status.

**TARGET n k** Show data and set target lights as follows:

| | |
|---|---|
| TAR 0: Relay Targets | TAR 1: Relay Word #1 |
| TAR 2: Relay Word #2 | TAR 3: Relay Word #3 |
| TAR 4: Relay Word #4 | TAR 5: Relay Word #5 |
| TAR 6: Relay Word #6 | TAR 7: Contact Input States |
| TAR 8: Contact Output States | TAR R: Test and Reset targets |

Option k displays target data k times.

**TIME h/m/s** Show or set time. TIM 13/32/00 sets clock to 1:32:00 PM. IRIG-B overrides this setting.

**TRIGGER** Trigger and save an event record (event type is TRI).

## ACCESS LEVEL 2 COMMANDS

**KSET n** Calculate ratio adjustment k values (allows user to set them directly); n selects number of samples to average over, default = 60. When calculated values are set, relay pulses ALARM contacts closed and clears event buffers.

**LOGIC n** Show or set logic masks MT, MER, MA1–MA5. ALARM contacts pulse and event buffers are cleared when new settings are stored.

**PASSWORD** Show or set passwords. Command pulses ALARM relay closed momentarily after new passwords are set. PAS 1 OTTER sets Level 1 password to OTTER. PAS 2 TAIL sets Level 2 password to TAIL.

**PULSE n** Close specified output contact for one second with JMP104 installed; n= T,1,2,3,4,5, or A.

**SET n** Initiate set procedure. Optional n selects first setting. SET VSS initiates setting procedure at VSS setting. SET initiates setting procedure at beginning. ALARM contacts pulse and event buffers clear when new settings are stored.

# EXPLANATION OF EVENT REPORT

```
Example Settings                              Date: 6/1/92      Time: 10:18:54.362
FID=SEL-187V-R401-V65p-D91061-E2


  Voltage PHASOR COMPONENTS, volts secondary      Relay Word     Outputs  Inputs
                                                                TAAAAAA  RLRLEE
  VAX     VBX     VCX     VAY     VBY     VCY    R1R2 R3R4 R5R6  P12345L  EEEETT
                                                                         112212

  12.06   12.28   12.03   12.19   12.13   12.81  0000 0000 03C1  .....*.  ......
  65.94   65.97   65.97   66.19   65.13   65.00  0000 0000 03C1  .....*.  ......
 -12.03  -12.28  -12.00  -12.19  -12.13  -12.81  0000 0000 03C1  .....*.  ......
 -65.97  -65.97  -66.00  -66.19  -65.13  -64.97  0000 0000 03C1  .....*.  ......

  12.06   12.31   12.00   12.19   12.09   12.78  0000 0000 03C1  .....*.  ......
  65.94   65.94   66.00   66.19   65.13   64.97  0000 0000 03C1  .....*.  ......
 -12.09  -12.31  -12.00  -12.19  -12.03  -12.75  0000 0000 03C1  .....*.  ......
 -65.94  -65.94  -66.00  -66.22  -65.16  -65.00  0000 0000 03C3  *.*.**.  ......

Event   :TRIP  TARGETS: EN,87A
X27L = 50.00    X59I = 80.00    Y27L = 50.00    Y59I = 80.00    3Y59D= 60
X59PU= 75.00    X59D = 1800     Y59PU= 75.00    Y59D = 1800     VSS  = X
59P1 = 70.00    THP1 = 60       THD1 = 60
27P1 = 65.00    TLP1 = 60       TLD1 = 60
59P2 = 70.00    THP2 = 60       THD2 = 60
27P2 = 65.00    TLP2 = 60       TLD2 = 60
KA   = 1.012    KB   = 1.012    KC   = 1.012
87AA = 0.50     87BA = 0.50     87CA = 0.50     87T  = 1.00     87H  = 2.00
87APD= 60       87TPD= 60       87HPD= 30       87DO = 60
A1PD = 0        A2PD = 0        A3PD = 0        A4PD = 0        A5PD = 0
TDUR = 4        LTCHE= N        LOPE1= Y        LOPE2= Y        LOPD = 60
TIME1= 5        TIME2= 0        AUTO = 2        RINGS= 3
```

Voltages are in secondary volts. Rows are quarter-cycle apart. Time runs down page. Obtain phasor RMS value and angle using any entry as Q-component, and the entry immediately underneath as the P-component. For example, from top rows, VAX(Q) = 12.06, VAX(P) = 65.94. Therefore, VAX = 67.03 volts RMS secondary, at an angle of ATAN(12.00/65.94) = 10.40 with respect to the sampling clock.

| | |
|---|---|
| <FID> | Firmware Identification Data |
| <Relay Word> | Row 1 through Row 6 of the Relay Word, each row in hexadecimal representation. |
| <Outputs> | Columns show states of output contacts: ON = "*", OFF = "." TP=TRIP, A1-A5=PROGRAMMABLE, AL=ALARM |
| <Inputs> | Columns show states of input contacts RE1=Raise Enable 1, LE1=Lower Enable 1, RE2=Raise Enable 2, LE2=Lower Enable 2, ET1=External Event Report Trigger 1, ET2=External Event Report Trigger 2 |
| <Event> | Indicates function which triggered event report. TRIP=TRIP output asserted during event report MER= Assertion of an element in MER mask TRI= TRIGGER command execution ET1= ET1 input assertion ET2= ET2 input assertion |
| <Targets> | Indicates front panel targets asserted at instant event report was triggered. |
| X59I,X27L | Source X overvoltage and undervoltage settings |
| Y59I,Y27L | Source Y overvoltage and undervoltage settings |
| 3Y59D | Source Y three-phase overvoltage dropout delay |
| X59PU,X59D | Source X definite-time overvoltage pickup and time delay |
| Y59PU,Y59D | Source Y definite-time overvoltage pickup and time delay |
| VSS | Voltage Control Scheme Selection |
| 59P1,THP1,THD1 | Voltage Control Scheme 1 overvoltage pickup and time delays |
| 27P1,TLP1,TLD1 | Voltage Control Scheme 1 undervoltage pickup and time delays |
| 59P2,THP2,THD2 | Voltage Control Scheme 2 overvoltage pickup and time delays |
| 27P2,TLP2,TLD2 | Voltage Control Scheme 2 undervoltage pickup and time delays |
| KA,KB,KC | Differential overvoltage ratio adjustment factors |
| 87AA,87AB,87AC | A-phase,B-phase,C-phase differential overvoltage alarm thresholds |
| 87T | Differential overvoltage trip threshold |
| 87H | High-set differential overvoltage trip threshold |
| 87APD,87TPD,87HPD | Differential overvoltage alarm and trip pickup delays |
| 87DO | Differential overvoltage alarm, trip, A4 and A5 output dropout delays |
| A1PD-A5PD | Output contact pickup delays |
| TDUR | Minimum trip duration timer |
| LTCHE | Enable Latch Bit function |
| LOPE1,LOPE2 | Loss-of-Potential enables for Voltage Control Schemes 1 and 2 |
| LOPD | Differential overvoltage supervisory LOP condition dropout time delay |

```
TIME1,2              Communications port timeout intervals (automatic log-off)
AUTO                 Port assignment for automatic message transmissions
RINGS                Number of rings to wait before modem answers telephone
<Logic Settings>     See LOGIC command for a description of mask settings
```