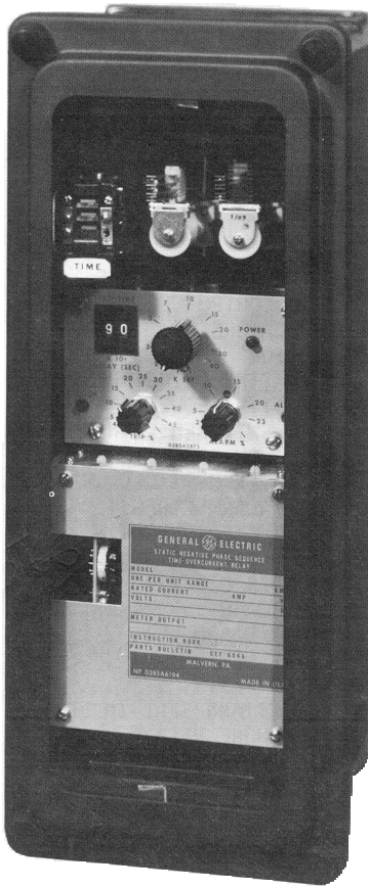
# INSTRUCTIONS

## SGC 21A, 21B, 21C
## Negative-Sequence Time Overcurrent Relays

Manual Part Number: GEK-86069J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## DESCRIPTION

The SGC relays covered in this manual are intended to protect generators against possible damage from unbalanced phase currents. The time-overcurrent function and the alarm function (when included) respond to the negative-sequence component (I2) of generator current.

There are three models available of the Type SGC21 family of relays. The negative-sequence time-overcurrent unit is included in all three models. Other differences are shown in the table below:

**Table 1: SGC RELAY COMPARISON**

| TYPE | ALARM FUNCTION | EXTERNAL METER | INTERNAL CONNECTIONS |
|---|---|---|---|
| 12SGC21A(-)A | Yes | No | Figure 11 |
| 12SGC21B(-)A | Yes | Yes | Figure 11 |
| 12SGC21C(-)A | No | No | Figure 12 |

All models listed are mounted in the M2 size drawout case. The external meter, which is included with the 12SGC21B(-)A models, is calibrated in percent of negative-sequence current (I2). Models 12SGC21A(-)A and 12SGC21C(-)A, which do not include the external meter, do include a metering output at the relay terminals so that the external meter can be added later if desired.

For 220 or 250 V DC supply voltages, see the RATING section.

*These instructions do not purport to cover all details or variations in equipment nor provide for every possible contingency to be met in connection with installation, operation or maintenance. Should further information be desired or should particular problems arise which are not covered sufficiently for the purchaser's purposes, the matter should be referred to the General Electric Company (USA).*

*To the extent required the products described herein meet applicable ANSI, IEEE and NEMA standards; however, no such assurance is given with respect to local codes and ordinances because they vary greatly.*

## APPLICATION

The SGC21 relays are negative-sequence, time overcurrent relays designed to protect generators against possible damage from unbalanced currents resulting from prolonged faults or unbalanced-load conditions. External connections to the relay for such an application are shown in the typical elementary diagram (Figure 1).

When a generator is subjected to an unbalanced fault or load, its stator current will include a negative-sequence component (I2) that sets up a counter-rotating flux field in the machine. This in turn causes double-frequency currents to flow in the rotor iron, which result in local heating. The heating of machines operating with unbalanced stator currents has been expressed, in terms of negative sequence and time, by the following relationship.

$$\text{Heat Energy} = \int_0^T i_2^2 dt \qquad \text{(Equation 1)}$$

If $i_2 = I_2$ (a constant), then $\text{Heat Energy} = I_2^2 T$. To protect the generator, heat energy must be less than K, that is:

$$\text{Heat Energy} = \int_0^T i_2^2 dt < K$$

Where: $I_2$ = negative phase-sequence current in per-unit of full-load stator current
$i_2$ = instantaneous negative-sequence current
$T$ = duration of the unbalanced condition in seconds
$K$ = a constant for the protected machine, representing maximum permissible heating
$dt$ = time difference in seconds

The values of the constant *K* may vary over an approximate range of 5 to 40, depending on the type, rating and design of the generator to be protected. Also the range of time, *T*, over which the relationship applies may vary for machines of recent manufacture and for older machines. The manufacturer of the machine to be protected should be consulted to determine the correct value of *K* and range of *T* for each application.

Since the capability of machines to withstand the heating caused by unbalanced faults or loads has been expressed in terms of $I_2^2T$, it is logical that the relay used to protect the machine from such conditions should be sensitive only to the matching the $I_2^2T$ characteristic of the protected machine. The SGC relays meet this requirement. Their trip and alarm functions are responsive only to negative-sequence current and the time current characteristic of the trip circuit is expressed as $I_2^2T = K$ being continuously adjustable from 2 to 40. This permits matching the characteristics of the negative-sequence protective relay with the capability curve of the machine to be protected.

The Type SGC relays protect the generator from damage due to abnormal conditions on the system rather than from damage caused by internal faults. The relays are therefore in a sense providing backup protection for other relays, and hence should act selectively with these relays. In other words, while it is essential that the time characteristic (i.e., *K* value) be selected so that the machine will be cleared before it suffers damage from an unbalanced condition, it is also necessary that the relaying schemes responding to external faults on the system be selected so that their correct operation will remove the fault before the SGC operates, even in the event of a circuit-breaker failure following an automatic reclosure onto a sustained phase-to-phase fault. This requirement is discussed in more detail in the CALCULATION OF SETTINGS section.

Note that the current $I_2$ in Equation 1 is defined as per unit of full-load stator current. The relay is matched to the CT-secondary full-load current by means of a tap switch on the front panel. This tap switch serves to match this secondary full-load current over a range of 3.1 to 4.9 A in 0.2 A steps. All references throughout this instruction book to per unit or percent $I_2$ are based on the relationship of the negative-sequence current ($I_2$) to the tap selected, that is:

$$\text{Per Unit } I_2 = \frac{I_2 \text{ (in amperes)}}{\text{Tap selected}}$$

$$\%I_2 = 100 \text{ per unit } I_2$$

The SGC relay can trip in one of two ways. In either case the negative-sequence current must exceed the trip-threshold setting. When this occurs, a timer, settable from 10 to 990 seconds in 10 second steps, begins timing. When the timer reaches the preset time, a trip output occurs. In addition, when the trip threshold is exceeded, the $i_2^2dt$ quantity is continuously computed and compared with the *K* setting (maximum permissible $i_2^2dt$ for the generator). When it exceeds *K*, a trip output occurs. When the negative-sequence input drops below the trip threshold, both the timer and the integrator begin to return to zero at a rate corresponding to the generator cooling rate.

## CALCULATION OF SETTINGS

A number of considerations are involved in determining the settings and adjustments of the SGC21 negative-sequence time-overcurrent relays. The principle purpose of these relays is to prevent the generator from being damaged by the negative-sequence current present during unbalanced-load conditions or during prolonged exposure to unbalanced faults. But it is equally important that there be coordination between these relays and the system protective relays on the high side of the step-up transformer, to avoid unnecessary shutdown of the generator during faults that will be correctly cleared by the system relaying. This requires consideration of the line protection, bus differential, and breaker-failure backup schemes.

The most severe condition for which coordination of the SGC and system relaying will be necessary is a phase-to-phase fault on the high side of the unit transformer, or more specifically, for a fault just beyond the breaker in a circuit off the high-side bus, where the breaker initially trips correctly, is automatically reclosed and fails to trip the second time, so that another breaker (or breakers) must be tripped by the breaker-failure backup scheme. For this situation the time, *T*, in the expression $I_2^2T = K$, defining machine capability, is the initial relay and breaker time, plus the total backup-breaker clearing time following the automatic reclosure, omitting the dead time in the reclosing cycle. The breakers, protective relaying and breaker-failure backup scheme must be selected or

designed so that the total time does not result in an $I_2^2T$ that exceeds the capability of the specific generator. Or more specifically, it must not result in an $I_2^2T$ that exceeds the setting of the SGC relay protecting the machine if an undesired trip is to be avoided.

The following settings or adjustments of the SGC functions are required:

1. Switch setting to establish the per-unit reference for the pickup and time characteristics.
2. Setting of the "*K*" function.
3. Setting of the trip threshold function.
4. Setting of the maximum trip time.
5. Setting of the alarm threshold function.

### TAP SWITCH SETTING

In the equation $I_2^2T = K$, the $I_2$ term is expressed in per unit of stator full-load current. The input tap-switch setting should be selected that is closest to the generator full-load current, referred to the CT secondaries. Then the relay time characteristic will be referenced to essentially the same base as the generator heating characteristic.

Tap-switch settings are available in 0.2 A steps between 3.1 and 4.9 A for the 5 A model, and in 0.04 A steps between 0.62 and 0.98 for the 1 A model. Switch positions are marked from 1 to 10, with corresponding ampere input ratings as tabulated below:

**Table 2: TAP SWITCH SETTING**

| SWITCH MARKING | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| 5 A MODEL | 3.1 A | 3.3 A | 3.5 A | 3.7 A | 3.9 A | 4.1 A | 4.3 A | 4.5 A | 4.7 A | 4.9 A |
| 1 A MODEL | 0.62 A | 0.66 A | 0.70 A | 0.74 A | 0.78 A | 0.82 A | 0.86 A | 0.90 A | 0.94 A | 0.98 A |

### "*K*" FUNCTION SETTING

The setting of the *K* function must be made so that the relay $I_2^2T$ characteristic matches the heating characteristic of the protected machine. Since the purpose of the relay is to protect the machine from thermal damage, its time-current characteristic should be set, by choice of the *K* factor, so that it falls slightly below the machine characteristic. This is illustrated in Figure 2, where a machine characteristic of $I_2^2T = 10$ has been assumed. A relay time characteristic of $I_2^2T = 8$, as shown by the dashed line in Figure 2, has been selected as typical of a setting that would provide margin below the machine characteristic. However, the user must decide for themselves what margin they desire between relay and machine characteristics.

Calibration markings are shown on the dial plate for the *K* adjustments. These markings are intended to provide an approximate trial setting, which should then be refined by test (see the INSTALLATION section).

### TRIP THRESHOLD SETTING

The negative-sequence operating point of the trip threshold function is continuously adjustable between 0.04 and 0.40 per unit, referred to the input switch setting as the base. While it is ultimately the responsibility of the user to select the setting of the trip threshold, some alternatives can be offered.

a) The setting can be based on the continuous negative-sequence current ($I_2$) rating of the machine, or on the minimum available setting of the trip threshold, whichever is higher. Using this basis for the setting, the machine may be "overprotected" depending on the *K* function setting that has been selected. For example, assume that the continuous $I_2$ rating of the machine is 0.08 per unit. If the protected machine has a capability of $I_2^2T = 10$, it can carry a negative-sequence current of 0.08 per unit for 1560 seconds without damage. However, since the maximum possible operating-time setting is 990 seconds, the relay will "overprotect" for $I_2$ currents between 0.08 and 0.10 per unit. For currents of 0.10 per unit and above, the relay will provide "exact" protection of the machine as indicated by its $I_2^2T = 10$ capability.

b) The setting of the trip threshold can be based on the value equivalent to the 990 seconds maximum-time setting for the particular *K* curve. If $I_2^2T = 10$, a setting of 0.10 per unit would correspond approximately to the 990 second maximum-time setting. Although this approach avoids the "overprotection" of the machine, it does

introduce a wider "dead zone" between the $I_2$ continuous machine rating and the trip-threshold setting. But as in the approach in a) above, the operator will be warned by the operation of the alarm function when the $I_2$ magnitude falls in this range and will have time to take corrective action.

Calibration markings on the dial plate permit an approximate setting of the trip threshold. However, it is recommended that the final setting be confirmed by test, using the test circuit and procedure described in the ACCEPTANCE TESTS section. In most cases, the input switch setting will not exactly match the generator full-load current, since the switch positions are in finite steps of 0.2 A. But the trip threshold can be set at the desired percentage of full-load current during test by setting the test current at a value equivalent to the desired negative-sequence current and adjusting the trip threshold to operate at that value.

Do not set the trip time to zero seconds. Otherwise the relay will operate as an instantaneous negative-sequence overcurrent relay. Do not attempt to use control settings outside the calibrated range. The results are unpredictable.

### MAXIMUM TRIP TIME

As previously noted, when the negative-sequence current exceeds the trip threshold setting, the trip timer is energized. This timer can be set from 10 to 990 seconds in 10 second steps. Its setting is determined by the continuous negative-sequence current ($I_2$) rating and the *K* characteristic of the machine. This is described in the previous TRIP THRESHOLD SETTING sub-section.

### ALARM THRESHOLD SETTING

The negative-sequence current pickup of the alarm threshold is continuously adjustable between 0.02 and 0.2 per unit, referred to the tap setting as a base. It is essential that this setting be sufficiently sensitive to detect any negative-sequence current that approaches or exceeds the continuous $I_2$ rating of the protected generator as determined from the manufacturer. For example, if a conductor-cooled generator has an $I_2$ continuous rating of 0.06 per unit, the alarm threshold should be set at or below 0.06 per unit (referred to generator full load). For negative-sequence current levels that fall between this value and the operation point of the trip threshold, the alarm unit contacts can be used to sound an alarm to warn station attendants that corrective action must be taken.

The operating point of the alarm threshold should be set by test, using the circuit and procedure described in the ACCEPTANCE TESTS section, and using a test current that simulates a negative-sequence current that is the required percentage of the generator full-load current.

### CALCULATION EXAMPLE

Assume that the SGC relay is to be applied on a unit generator-transformer installation having the following characteristics:

- Generator: 400 MVA, 25 kV
- Transformer: 400 MVA
- Generator CT Ratio: 10000:5
- Base: 400 MVA, 25 kV
- "*K*" for generator: 10

The generator full-load current, on the basis of the 400 MVA rating, should be calculated as follows:

$$\text{MVA} = \frac{\sqrt{3} \cdot I \cdot \text{generator kV}}{1000}$$

$$\Rightarrow I = \frac{\text{MVA} \cdot 1000}{\sqrt{3} \cdot \text{generator kV}} = \frac{400\,\text{MVA} \cdot 1000}{\sqrt{3} \cdot 25\,\text{kV}} = 9238\ \text{A primary}$$

$$\Rightarrow I = \frac{9328\ \text{A}}{2000} = 4.62\ \text{A secondary}$$

The input current selection switch should be placed in the 4.7 A position (number 9 position), which is the position closest to the calculated full-load current.

The trip threshold should now be set with sufficient sensitivity to ensure operation at the expected minimum load with one pole of the main generator breaker open. If we assume that the corresponding value of $I_2$ is 0.9 A, or 0.19 per unit, for our example the trip threshold must be at least this sensitive. This value, however, should be considered as an upper limit of trip threshold pickup. It is recommended that it be set nearer its minimum; a setting of 0.12 per unit based on full load is suggested. For our example, this would be an $I_2$ pickup of 0.12 (4.62) = 0.554 negative-sequence amps, using the procedure outlined under ACCEPTANCE TESTS.

Prior to setting the *K* factor, the user should determine the negative-sequence current from the generator for a phase-to-phase fault on the high side of the step-up transformer for typical system conditions. Assume that this is determined to be 8.35 A, which is 8.35/4.62 = 1.81 per unit, referred to generator full load as a base. The *K* factor should be set by test, recognizing that the input switch setting of 4.7 does not exactly match the full-load current. To compensate for this, the *K* factor setting should be made at the calculated secondary negative-sequence current, 8.35 A in this example, but the operating time should be set by test on the basis of per unit current referred to the machine full load as a base, that is:

$$\frac{8.35\ \text{A}}{4.62\ \text{A}} = 1.81\ \text{per unit}$$

Assuming that the desired relay characteristic is $I_2^2T = 8$, the time setting at 8.35 A should be calculated as follows:

$$I_2^2 T = 8 \Rightarrow T = \frac{8}{I_2^2} = \frac{8}{(1.81)^2} = 2.45\ \text{seconds}$$

Using the test procedure and connections described in the INSTALLATION section, the *K* adjustment should be set to obtain the desired 2.45 seconds operating time with a negative-sequence current of 8.35 amperes applied to the relay. Note that the integrator reset time from the fully-operated condition is normally 250 seconds. To expedite testing of the relay to verify the setting, it is recommended that the DC supply to the relay be opened for 10 seconds following each test, to discharge the integrator. The time should be checked at a lower multiple, again recognizing that the 4.7 A relay tap does not exactly match the machine full load. Referred to the relay tap-switch setting, the 8.35 A negative-sequence test current is equivalent to 8.35 A /4.7 A = 1.78 per unit. Hence, the actual relay characteristic (i.e., *K* of the relay) is:

$$K = \left(\frac{8.35\ \text{A}}{4.70\ \text{A}}\right)^2 \times 2.45\ \text{sec.} = 7.73$$

If a lower test current of 4.7 A negative sequence is now applied to the relay, it will be 1 per unit on the relay tap base, and the operating time should be $T$ = 7.73 seconds ±10%. Referred to the machine-full-load base, this is equivalent to:

$$K = \left(\frac{4.70\ \text{A}}{4.62\ \text{A}}\right)^2 \times 7.73\ \text{sec.} = 8$$

## RATINGS

The SGC relay is designed for continuous operation in ambient temperatures between –20°C and +65°C. These relays will not be damaged if stored at ambient temperatures of –40°C to +85°C (trip level will not shift more than 0.005 or 0.5% or pickup).

### INSULATION

Type SGC relays will meet the specifications of ANSI C37.90 between CT input and case, DC inputs and case, and sets of output contacts and case.

### OPERATE FREQUENCY RANGE

Type SGC relays have less than 0.5% shift in alarm and trip setting over a 57 to 63 Hz input range (47.5 to 52.5 Hz for the 50 Hz model).

### OVERLOAD CURRENT

The overload current for the SGC relay is:

- Five ampere rating: 250 A for 1 second
- One ampere rating: 50 A for 1 second

### SUPPLY VOLTAGE RANGE

These relays can be set to operate on one of two ranges:

- 48 V DC operating range: 33.6 to 56 volts
- 110/125 V DC operating range: 87.5 to 140 volts

If the DC supply voltage is 220 or 250 V DC, there are several relay models available that use an external pre-regulator. The pre-regulator is supplied with the relay and is listed on the SGC relay nameplate. It is used to reduce the DC supply voltage to the relay's DC rated voltage. Those relays that have a DC voltage selection option should be set on the 125 V DC position.

The pre-regulator mounting is shown in Figure 23, and electrical connections are shown in Figure 24. The DC voltage operating range of the pre-regulator input is:

- 220 V DC: 165 to 242 volts
- 250 V DC: 187.5 to 275 volts

If the supply goes below the minimum value, the relay automatically disables itself to prevent improper operation. Supply voltages above the maximum value increase heating and reduce life. Voltages 25% or more above the maximum may cause immediate failure. Supply variations within the rating will not change calibration by more than 0.5%.

### CONTACT CURRENT RATINGS

The contacts of these relays will carry 3 A continuously, and they will make and carry 30 A for tripping duty.

### TARGETS

The Type SGC relays can be supplied with either the 0.2/2.0 or the 0.6/2.0 target seal-in unit (see table below):

**Table 3: SGC TARGET RATINGS**

| TARGET SEAL-IN UNITS | 0.6/2.0 UNIT | | 0.2/2.0 UNIT | |
|---|---|---|---|---|
| | 0.6 A | 2.0 A | 0.2 A | 2.0 A |
| Maximum to Ensure Operation | 0.6 A | 2.0 A | 0.2 A | 2.0 A |
| Carry Continuously | 1.5 A | 3.5 A | 0.4 A | 3.5 A |
| Carry 30 A for | 0.5 sec. | 4.0 sec. | --- | 4.0 sec. |
| Carry 10 A for | 4.0 sec. | 30 sec. | 0.1 sec. | 30 sec. |
| DC Resistance | 0.6 Ω | 0.13 Ω | 7 Ω | 0.13 Ω |
| 60 Cycle Impedance | 6.0 Ω | 0.53 Ω | 52 Ω | 0.53 Ω |

### BURDENS

The AC current input to the SGC relay has a burden of less than 0.2 ohm. At nominal supply voltage, the DC power supply presents a burden of 8 watts untripped, and 12 watts tripped.

## CHARACTERISTICS

### OPERATE TIME

The SGC relay has a timer trip time of from 10 to 990 seconds, settable in 10 second steps. The *K* trip time depends on the *K* setting and current used (see the APPLICATION section for settings).

### CURRENT (BASE CURRENT RANGE)

The current corresponding to 1 per unit is adjustable from 3.1 to 4.9 A in 0.2 A steps.

### ALARM UNIT

The alarm unit threshold is continuously adjustable between 2 and 20% of the base-current setting.

### TRIP RANGE

The trip-current pickup of the SGC relay is continuously adjustable between 4 and 40% of the base-current setting.

### *K* SETTING

The *K* setting of the SGC relay is continuously adjustable between 2 and 40. *K* is the maximum permissible value of $i_2^2 dt$, where *i* is expressed in per unit values of negative-sequence current and *dt* is expressed in seconds. *K* is a characteristic of the generator and is specified by the manufacturer.

### DELAYS

There is a minimum trip delay of 0.2 second. The alarm delay is 3 seconds.

### MAXIMUM RESET TIMES

The maximum reset for time trip is the same as the time-trip setting. For *K* trip it is 250 seconds, maximum. The maximum occurs when the input current has caused $I_2^2 T$ to be almost equal to the *K* setting.

### METER OUTPUT

One per unit negative-sequence component is 2.5 V DC. This output is a linear function of the negative-sequence component. If a meter other than the one supplied with the SGC21B is used, the external meter should have a resistance greater than 10 MΩ, if it is a voltmeter. For current meters, the series R should be adjusted to obtain the desired reading. Maximum output to the meter is approximately 7 V under worst-case conditions (3 per unit negative sequence).

### INDICATORS

There are three indicators provided in the SGC relay: the POWER SUPPLY indicator indicates that the power supply is on, the ALARM LEVEL indicator indicates that the alarm level has been exceeded (not necessarily that an alarm output has occurred), and the TRIP LEVEL indicator indicates that the trip level has been exceeded, (not necessarily that a trip output has occurred).

## CONSTRUCTION

### OPERATING PRINCIPLES (SEE FIGURE 4)

The first section of the SGC relay consists of a negative-sequence network, an adjustable gain stage to set the nominal current, low pass filters to eliminate harmonics, and a rectifier. The DC from the rectifier is filtered, and then used for several purposes. The filtered DC is proportional to the negative-sequence current, and is compared with the alarm threshold to give an alarm output. This same DC is also compared with a trip threshold to start integration of $i_2^2$ ($i_2$ equals negative-sequence current) if the negative-sequence level exceeds the trip threshold. The DC also goes to a squarer circuit that gives a pulse output, the average frequency of which is proportional to the square of the negative-sequence current. The pulse rate is counted (integrated) if the negative-sequence input

exceeds the trip threshold. This count is converted into a proportional analog voltage, which is then compared with the *K* potentiometer voltage. *K* pot voltage represents the permissible generator heating. When the count voltage exceeds the *K* pot voltage, the SGC outputs a trip signal. In addition, when the negative-sequence level crosses the trip threshold, a timer, set by front panel controls, is also started. When the timer setting is exceeded, a trip output also results.

Should the negative-sequence input exceed the trip threshold for a short period, and than drop below the threshold, the integrator counter and the timer counter both will count back to their original values.

From the foregoing, it is seen that the SGC can trip in one of two ways. In either case, the negative-sequence input must exceed the trip threshold current. When this threshold is exceeded, the relay will trip when the timer setting is exceeded, or the integral of $I_2^2T$, with respect to time, exceeds the *K*-pot setting. Negative-sequence inputs slightly above the threshold will normally result in timer trips, since the integral of $I_2^2T$ does not build up rapidly in this case. Larger negative-sequence inputs will result in an $I_2^2T$ integral or *K* trip.

**NEGATIVE SEQUENCE NETWORK**

The SGC relay employs a frequency-compensated negative-sequence network. This minimizes the effect of input frequency variations on the negative-sequence network performance. The operation can best be described by referring to the simplified negative-sequence network diagram, Figure 4, and to the negative-sequence network phasor diagram, Figure 5.

The phase currents are applied through current transformers that transform the input current to low level values suitable for input. The secondary currents result in voltages $e_1$, $e_2$, and $e_3$ across the wye-connected resistors R1, R2, and R3. Voltage $e_1$ contributes a current at the operational amplifier input, consisting of two components. One current goes through the R13, C1 path. This is represented by the phase marked $I_{C1}$ on the phasor diagram. The other current is obtained from voltage divider R4, R5, R6, and passes through C2. This current is marked $I_{C2}$ on the phase diagram. Its amplitude is much smaller that $I_{C1}$, and it is at right angles to voltage $e_1$. The sum of $I_{C1}$ and $I_{C2}$ is labeled $I_1$, and is 15° ahead of $e_1$. This compensating variation of the two current components with input frequency variation minimizes the effect of input frequency on $I_1$ and on the negative-sequence network.

Voltage $e_2$ gives a current $I_2$ at the summing junction (operational amplifier input), which also consists of two components that provide frequency compensation. One component goes through R11 and R12, with C3 shifting its phase. The other component comes from inductor L1, then through R8, R7, and R6. The components are shown in Figure 4.

In effect, currents $I_1$ and $I_2$ are summed in the operational amplifier to give resultant $I_R$. $I_R$ is out of phase with $e_3$. The exact phase angle can be set by trimmer R6. The operational amplifier receives current $I_3$, through resistors R9 and R10, which is in phase with $e_3$. The amplitude of this current is set by R9 and R10 to match that of $I_R$. The result is $I_3$ and $I_R$ cancel when R6 and R9 are properly set. This means the network rejects the phase sequence shown.

If the opposite phase sequence is applied, then the situation shown in Figure 6 occurs. Voltage $e_2$ still gives a current $I_2$ lagging by 15° and $e_1$ still gives a current $I_1$ leading by 15°. The result when these two are combined, $I_R$, is totally different from the previous phase sequence, and cancellation does not occur. The network will give an output for one phase sequence and not the other. When the two-phase sequence components are combined, as they are in many actual three-phase systems, this network will see only one of the two. In the case of this relay, only the negative-sequence component is seen, since the positive-sequence component cancels. The zero-sequence component of any input is eliminated by the delta connection of the CT secondaries.

The full details of this network, which is on the negative-sequence/analog board, plus off-board components, are shown in the board internal connections diagram, Figure 14, and the relay internal connections diagram, Figure 11 or 12.

**SWITCHED GAIN AMPLIFIER**

The operational amplifier associated with the negative-sequence network is provided with switch-selectable gain control resistors. Switch S1 selects one of ten resistors to set the nominal current rating of the relay (tap setting). Zener diodes Z1 and Z2 in the feedback path limit the operational amplifier output to a level that will not overload the subsequent stages.

**LOW PASS FILTERS**

The switched gain stage is followed by four identical cascaded low pass filters. Their purpose is to provide 30 decibels rejection of third harmonics at 150 and 180 Hz. This means a 150 Hz signal into the filter will be attenuated to about 1/30 of the input value (voltage ratio) where a 50 or 60 Hz signal would have been amplified slightly to 1.27 times the input value. The slight gain at 50 and 60 Hz is due to peaking the filter gain at 55 Hz. This peaking gives the filter a reasonably constant gain in the 47 to 63 Hz range. If peaking were not used, the gain would drop and the trip level would increase significantly between 47 and 63 Hz.

Each filter consists of an operational amplifier and its associated resistors and capacitors. The operational amplifier not only acts as a buffer, but the feedback from its output to input via the 0.1 μF capacitor significantly affects the filter response curve. Four of these filters are used, since one such filter cannot provide enough rejection at 150 Hz. These filters introduce a time delay in the signal of approximately 8 milliseconds; this introduces a small delay in the relay's operate time.

The output of the filters is capacitively coupled through C13 to a "perfect" rectifier. The coupling capacitor eliminates DC offset voltages arising in the preceding direct-coupled stages. The perfect rectifier is called "perfect" because it does not exhibit the diode drop losses and non-linearities that occur in simple diode rectifiers. The rectifier operates as follows: The input signal causes a current to flow through R33 to the inverting input of operational amplifier U2. This produces a voltage at the input, causing an output signal, which is fed back to the input via either diode CR3 or CR4, depending on the output polarity. On positive input, diode CR3 conducts and the diode end of R35 carries a negative replica of the input. The diode end of R36 is at zero (0) volts. On negative inputs, the situation is reversed with the diode end of R36 carrying a positive replica of the negative input. The diode end of R35 is at zero (0). The output pin 8 of operational amplifier U2 exhibits non-linearities as the input varies, due to drops across diodes CR3 and CR4. This non-linearity is reduced in the half-wave rectified signals at R35 and R36 by the high voltage gain of the operational amplifier (50000 to 100000). The negative-going half-wave signal at R35 is buffered in one section of U3, and inverted by going to the inverting input of the summing section. The positive-going half-wave signal at the diode end of R36 is buffered in another section of U3 and is applied to the positive input of the summing section of U3. The output is a full wave rectified signal, derived from the input. Resistors R39 and R41 associated with the summing section of U3 give a gain of 1 from the inverting input to the output. These same two resistors give a gain of 2 from the non-inverting input of the summing section to its output. Divider resistors R40 and R42 make the rectified output half-cycles, have the same amplitude. The waveforms are shown in Figure 7.

**TEN HERTZ LOW PASS FILTER**

Following the rectifier is a 10 Hz low pass filter to smooth the rectified DC. This low pass filter is similar to the previously described low pass filter, except for those components that determine cut-off frequency. The output of this low pass filter drives four circuits: the alarm threshold, the trip threshold, the meter output and the integrator (*K* circuit). A DC level of 2.5 V at the low-pass-filter output corresponds to 1 per unit negative-sequence input.

**ALARM CIRCUIT**

The filtered DC from the rectifier goes through resistor R46 to pin 5 of one comparator in quad comparator U4. The other input to this comparator is from the alarm-set potentiometer on the front panel. The alarm pot output is adjustable from 25 to 625 mV, corresponding to an alarm range of 1 to 25% negative sequence, with a usable range from 2 to 20%. When the filtered DC from the rectifier exceeds the alarm pot voltage, the comparator output at pin 2 goes positive. The positive feedback through resistor R48 latches the comparator on. The comparator is pulled up almost to the positive supply by R56. This turns on the alarm LED driver, Q3, so that card pin 16 goes high, turning on the front panel LED.

At the same time, the positive comparator output at pin 2 of U4 starts charging capacitor C37 through R58. When his capacitor charges to 7.4 V (the voltage at the junction of R59 and R60), the comparator in U4 with input pins 8 and 9 turns on. When its output pin 14 goes positive, it turns on the alarm relay driver, consisting of Q1 and Q2, in a Darlington configuration. Varistor VR4 is provided to limit inductive spikes.

**METER OUTPUT**

The filtered DC from the low pass filter goes through resistor R63 to card pin 19. This meter output is protected by varistor VR5 to prevent excessive voltage surges from entering the relay. Capacitor C33 is provided to filter high frequency noise.

The original relay uses a value of 806 Ω for R63 and a meter with a 195 Ω resistance. In the Rev. "A", "B", and "C" relays, R63 equals 374 Ω and the meter resistance is 630 Ω.

**TRIP THRESHOLD CIRCUIT**

The filtered DC from the low pass filter also goes to pin 7 or U4, which is a comparator input. The other input of this comparator is pin 6. Pin 6 gets its voltage from the trip level potentiometer on the front panel. The pot voltage ranges from 75 mV to 1.12 volts, representing a trip range of 3 to 44%. As in the alarm circuit, positive feedback is used to provide hysteresis so all threshold crossings are unambiguous. The output of the comparator drives trip LED driver Q4 and card pin 13. This trip output signal serves many functions. It serves as a count-up/down signal for the integrator (*K* counter) and the timer. It selects the integrator signal source, as will be described later.

**SQUARER CIRCUIT (FIG. 15)**

The filtered DC from the rectifier enters this board on pin 6 and goes to U15, which, together with the following operational amplifier, is a multiplying digital-to-analog converter (D/A). Here it is used as a digitally-controlled attenuator. Its output is a replica of the input, except it is scaled down by an amount depending on the digital signals at pins 5, 6, 7, and 8 of U15. This negative output signal is applied to pin 3 or U20, which functions as single-pole double-throw (form C) switch, whose output is obtained from inputs at either pin 3 or pin 6. The selection of the input pin is determined by the digital level at pins 1 and 8. The input signal comes from the analog board via card pin 6 when the trip level is exceeded and from the K board via card pin 19 when the input is below the trip setting. These signals control count-up and count-down rates of the K counter, respectively. The output appears at either pin 2 or pin 7 and from there goes to U14, which is a voltage-to-frequency converter (V/F). The output of U14 is a pulse train whose frequency is proportional to the input voltage. It has two adjustments. R64 is an offset adjustment, which gives the correct frequency at low input voltages. R67 adjusts the frequency at high input voltages. The output frequency is about 20 KHz at 1 per unit negative sequence. The output pulse train goes to U16, which is a binary counter. Two outputs from this chip are used. Pin 4 (divide by 128) is used during count down. During count up (trip level exceeded), the output from pin 14 (divide by 1024) is used. The output from pin 14 is used to drive 4-bit counter U17, whose purpose will be described later. In addition, it drives one-shot U18 to generate 0.01 second pulses. These 0.01 second pulses are ANDed with the V/F output pulses in an AND gate, which is in integrated circuit U22. Any V/F output pulses occurring during the 0.01 second one-shot output pulses appear at the output of the AND gate at pin 11 and go to card pin 18. The output at card pin 18 consists of bursts of V/F output pulses. Each burst lasts for 0.01 second, and the V/F frequency determines how often the 0.01 second pulses occur, and how many pulses are in each burst. The higher the input voltage to the V/F, the more frequent the one-shot pulses, and the more V/F output pulses within each 0.01 second one-shot pulse. See the squarer output wave forms, Figure 8. The result is that the average output rate over many bursts is proportional to the square of the V/F input voltage. Since this input voltage is proportional to the negative-sequence current, the average pulse rate is proportional to the square of the negative-sequence current. The ideal and actual average pulse rate versus negative-sequence current curves is shown in Figure 9.

If the squarer circuit worked as described to this point, the average frequency of the output would exhibit pronounced jumps at low input levels. These occur because the number of V/F pulses within each 0.01 second one-shotgate pulse is small, perhaps only four pulses. As the V/F input increases, the spacing between 0.01 second gate pulses decreases, so in a given period there are more bursts of four pulses each. As the input to the V/F increases still more, at some point the V/F frequency will get high enough so a fifth pulse falls within the 0.01 second gate width. When this happens, the average output frequency shows an abrupt jump, as shown in the output curve for a simple squarer in Figure 9.

The circuit contains provisions to minimize this effect. As already mentioned, the counter output at pin 14 of U16 is used to clock counter U17. Counter U17 is a 4-bit binary counter. Its four digital output lines feed multiplying D/A U15. Every time pin 14 of counter U16 outputs a pulse, counter U17 steps and shifts the gain of multiplying D/A U15. After 16 counts, the gain sequence repeats. The series of identical bursts but rather a sequence of 16 non-

identical bursts, with this sequence then repeating. At low input levels to the V/F, instead of having a series of bursts all containing four pulses, some bursts will contain 2, 3, 4, 5, 6 ... etc. As the V/F input increases, not all bursts will gain extra pulses simultaneously, so the effect is to greatly reduce the size of the jumps in the average output frequency and make many more smaller jumps. This gives a much closer approximation to the ideal squarer curve (see Figure 10). The same effect occurs at high V/F input levels.

The output pulse train at card pin 18 is obviously a complex signal with many burst-to-burst variations. However, the average frequency is correct and this is all that matters, since the output pulse train is counted over may bursts before any operate decision is made.

**"*K*" BOARD (FIG. 16)**

The K board contains an up/down counter, which counts squarer output pulses when the trip threshold (on the analog card) is exceeded. This counter serves as an integrator for $i_2^2$. The counter output is converted to an analog voltage by a D/A converter. The analog output feeds two analog comparators. The outputs of these comparators control the maximum and minimum count. One of the comparators receives voltage, the up count is stopped and a trip signal is output.

If the counter contains other than the minimum count and the negative-sequence input signal is below the trip level, then the counter counts down at a rate such that it will drop from the value corresponding to *K*, down to the minimum in 250 seconds. This corresponds approximately to the cooling rate of the generator.

The details of the *K* card operation are as follows. The squarer card output pulses are applied to *K* card pin 33. They are ANDed in part of U34 with the count-up/down signal (output of the trip level comparator) and with a "permit up-count signal" from the *K* comparator via an inverter. The squarer output pulses go to the counter only when the input negative sequence exceeds the trip level, and only so long as the count does not exceed the K setting. The squarer pulses from the AND gate are ORed in part of U38 with "count-down" pulses from part of AND gate U34. In practice, only one type of pulse of the other actually is present. The pulses out of the OR gate in U38 go to U37, which is used as a divide-by-eight prescaler.

The output of this prescaler goes to the clock inputs of three integrated circuits, U36, U32, and U31, each of which is a 4-bit binary up/down counter. The counting direction, up or down, is controlled by the count-up/down signal from the trip level comparator, card pin 3.

As already mentioned, the count-up/down level controls the source of count pulses. These are either the squarer pulses already described, or the count-down pulses to be described later. The ten most significant bits (outputs) of the 12-bit counter are used to drive U35, which is a 10-bit digital-to-analog converter (D/A). This D/A requires a positive 10 volt reference signal. This is obtained from voltage dividers R77 and R78 off the positive 15 V supply. It is buffered in a section of U41, and applied to pin 15 of D/A U35. The D/A voltage output appears at pin 1 of operational amplifier U41 as a negative voltage, proportional to the count. It is compared to the *K* voltage in comparator U40 (pins 6 and 7). The output of this comparator, pin 1, is pulled up by resistor R89 through a LED that indicates the comparator state. The comparator output is coupled through diode CR4 to change the comparator output swing of approximately ±10 V to a 0 to +10 V swing compatible with CMOS logic. This logic output goes positive when the counter count gives a D/A output greater than the *K* voltage. It goes to pin 11 of inverter U33, whose low output will stop squarer pulses from passing the AND gate in U34.

The logic output also is a trip signal and goes to one input of an OR gate in U38. In this OR gate, it is ORed with a trip signal from the timer card, which comes in on card pin 8. The OR gate output, which indicates either a *K* trip or timer trip, is ANDed in part of U34 with a one-shot signal. The one-shot is triggered by an output at pin 3 of trip OR gate U38 when a trip signal occurs. The one-shot, U39, generates a 0.2 second pulse with the output taken off U39 pin 7. Pin 7 gives a low-going pulse that blocks the AND gate in U34 connected to pins 1, 2, and 8. This prevents a *K* or timer-trip signal from causing a trip until 0.2 seconds after the trip decision is made. Pin 9 of the AND gate in U34 is the output and drives a relay driver for the trip relay.

The *K* voltage has been mentioned previously. It is obtained from the front panel *K* potentiometer. This potentiometer is connected so the ends of the pot go to card pins 20 and 50. The wiper goes to card pin 19. With this connection, the *K* pot controls the gain of an operational amplifier in U41. The positive voltage from voltage divider R83 and R84 is amplified to form the negative *K* voltage. The potentiometer connections to the amplifier

give a non-linear relationship between pot rotation and K voltage. This improves the settability at low *K* settings by spreading the low *K* portion of the scale over a larger range.

The count-down pulses for the counter were mentioned earlier. Their purpose is to make the counter down when the negative-sequence input drops below the trip level. The count in the counter represents generator temperatures and the counting down represents cooling when the negative-sequence input drops back to a safe value. Normal practice is to count, from the count representing the maximum temperature (*K*0 for the generator, down to the minimum count, in 250 seconds. Since different generators have different *K*'s corresponding to different maximum counts, it is necessary to match the count-down pulse rate to the *K* if a fixed 250 second count-down time is needed. This is done by taking the voltage out of the K pot amplifier and applying it to pot R91. The wiper voltage of R91 leaves the K board via card pin 14, and goes to the squarer board, card pin 19. The voltage goes to one input of analog switch U20. This input is selected when the trip level is not exceeded. The voltage goes to the voltage-to-frequency converter U14, and controls its frequency. The V/F frequency is divided down by counter U16. The divided-down output from U16 pin 4 leaves the squarer board via card pin 4. It enters the K board by card pin 4 and goes to an AND gate with input pins 3, 4, and 5, which is part of U34. The count-down pulses will pass this AND gate only if the other two inputs are high. This occurs only when the trip threshold is not exceeded, and when the counter is above the minimum value. Under these conditions, the count-down pulses go to OR gate U38 pin 6, whose function has previously been described. Returning to pins 3 and 5, the other two input signals to the U34 AND gate pin 3 are fed through an inverter, part of U33, from the count-up/down line. Pin 5's signal is obtained by comparing the negative voltage from the counter D/A with a –20 mV signal from dividers R81 and R82 in comparator U40, pins 4 and 5. When the counter D/A output goes below –20 mV in amplitude, the comparator output goes low, preventing any more count-down pulses from passing the U34 AND gate connected to pins 3, 4, and 5.

When power is first applied to the relay, the counter is set to zero (0) by a reset signal from the power supply board.

**TIMER BOARD (FIG. 17)**

The timer board counts the time the relay input has exceeded the trip threshold. When this time reaches the time set by the operator, a trip signal is generated. The range of time settings id 10 to 990 seconds. If the relay input drops below the trip level, the timer counts down until it reaches zero or until the trip level is exceeded again.

The timer board has a 256 Hz oscillator made up of two inverters in U55 using pins 1, 2, 3, and 4, plus C24, R98, R99, and R100. Trimmer R100 permits the oscillator frequency to be trimmed to the right value. The oscillator output is divided by 256 in 8-bit binary divider U56. The divider output is 1 Hz and goes to NOR gate U57 pins 2 and 3. The NOR gate is actually used as an AND gate, using low true logic. To avoid confusion, the operation will be described without reference to high or low true logic since the logic is mixed on this card. The clock pulses appear at pin 1 of U57 only if pins 4 and 5 are low. Otherwise, the output is low continuously. When pins 4 and 5 are low, the clock pulses from U57 pin 1 go to inverter U55 pin 5. The inverter output from pin 6 goes to the clock inputs on BCD (binary-coded device) up/down counter chips U59, U60 and U61. The counter will count either up or down, depending on the voltage on the up/down line from card pin 14. A positive level will result in counting up, while zero volts results in counting down. A "normal-test" jumper is provided that speeds up testing by 16 times in "test."

It is necessary to avoid counting beyond the preset count or below zero. To avoid counting below zero, the circuitry involving U62, input pins 9, 10, 11, and 12 of U58, as well as input pins 1 and 2 of U58, senses when the count is zero and applies a high signal to pin 5 of U58 indicating that the count is zero. If the count-up/down signal, which enters the board on card pin 14, is low, then after it goes to pin 9 of inverter U55 and exits inverted from pin 8, it will be high. This signal is applied to pin 6 of U58. If U58 pins 5 and 6 are both high, the output at pin 4 will be high and block the gate U57 input pins 2, 3, 4, and 5. This means no further count can occur once the count is zero in the count-down mode.

To avoid counting beyond the maximum time, comparators U63 and U64 detect when the counter contents equal the BCD panel-switch settings and output a high signal from U64, pin 3. This signal goes to pin 9 of U58. The input to pin 8 of U58 is the count-up/down signal, which is high in the count-up mode. When both 8 and 9 are high, U58 pin 10 is high, and this goes to pin 4 or U58 to block further counting. Therefore, counting up halts as soon as the

counter contents equals the front panel switch setting. Note that the inputs from the BCD panel switches have capacitors for noise filtering and pull down resistors on every switch input line.

The output of AND gate U58 pin 10 also serves as a trip signal that is output on card pin 13. From there it goes to the K card where it is ORed with the K trip signal.

The reset signal from the power supply enters the timer board on card pin 4 and initializes the dividers and counters at the time of turn on.

### RELAY WIRING

Figures 11 and 12 are schematics of the relay wiring. They show the interconnection between the printed circuit cards and other components.

## ACCEPTANCE TESTS

### TARGET AND SEAL-IN UNIT

1. With the target reset, and the telephone relay contacts closed, check the pickup at both the minimum and maximum ampere taps, using direct current (DC). The armature should pick up with a snap action and seat itself against the pole piece. The permissible pickup ranges are shown in the table below.

| TAP | PICKUP WITH GRADUALLY INCREASED CURRENT |
|---|---|
| 0.2 | Less than 0.2 A |
| 0.6 | Less than 0.6 A |
| 2.0 | Less than 2.0 A |

2. Check that dropout of seal-in unit on 2.0 A maximum tap is 0.5 A or more.
3. Check the latch-in of the target by energizing the seal-in unit at rating. With the unit in the picked-up position, check the overtravel of the orange target, using a sharp tool, such as a knife. The orange target should move at least 1/64-inch. De-energize the seal-in unit and tap the top of the unit several times with the handle of a screwdriver. The target should not fall down.
4. Leave the tap screw in the desired tap when the tests are completed. During relay operation, tap screws should not be in both taps at the same time. If they are, pickup will occur at the higher tap value. The relays are shipped with the tap screw in the 2.0 A tap.

### TELEPHONE RELAYS

1. Check that each normally-open contact has a gap of 0.015 inch.
2. Check that each normally-open contact has at least 0.005 inch overtravel after contact closure.

### HIGH POTENTIAL TEST

**CAUTION:**
**Disconnect the surge capacitors before proceeding with this test.**

1. Printed circuit boards and nameplate must be in place. The relay must be in its case with the cover installed.
2. Connect all studs of case together **except studs 15 and 16**.
3. Apply voltage from all **connected** studs to metal of case.
4. Smoothly raise voltage from zero (0) to 1650 V RMS at 60 Hz, hold for one (1) minute, then smoothly lower voltage to zero (0).
5. Any breakdowns must be corrected before proceeding with test.

**INSPECTION**

1. Check that all four cards are properly installed.
2. Check that the power supply card is set for overvoltage operation and for 125 V DC operation (as shipped) or as required for a particular installation.
3. Check that the knob pointers are properly positioned. In its extreme position, the pointer should fall on the last scale marks.
4. Check that the targets operate. Trip and reset by hand.

## ELECTRICAL TESTS

The purpose of this section is to verify that the relay has been received in working order, if the relay should fail any of the following tests refer to the trouble shooting section for expanded test procedures and calibration instructions. Note the TEST link on the timer board should be in the NORM position, the TEST position increases the clock frequency for factory testing.

- **Response to Negative Sequence**: Connect the relay per Figure 19 except flip "A" and "B", with the Tap Switch set to 10 and 4.9 A applied to the relay the voltmeter should read 2.5 V ±10%. Change the TAP Switch to 6 and the voltage should increase to 3.0 V ±10%, now move the Tap Switch to 3 and the voltage should increase to 3.5 V ±10%. Return the Tap Switch to 10.
- **Alarm and Trip Threshold**: Apply current to phase A only, set the current to 3.0 A and adjust the alarm pot until the ALARM LED on the front panel lights, the pointer should be between 17 and 23. Reduce the current to 0.3 A and the adjust the alarm pot until the ALARM LED lights, the pointer should be between 1 and 3, leave the alarm pot at this setting for the operating time tests.

  Set the current to 6.0 A and adjust the trip level pot until the TRIP LEVEL LED lights, the pointer should be between 35 and 45. Reduce the current to 0.6 A and adjust the trip level pot until TRIP LEVEL LED lights, the pointer should be between 3 and 5, leave the trip level pot at this setting for the operating time tests.
- **Operate Times**: With the Alarm and Trip settings from the last test set the *K* dial to 40 and the Time setting to 10 seconds, turn on the DC and apply 0.72 A to phase A, the trip output relay should close in 8.3 to 11.3 seconds. Remove the AC and then the DC, change the time to 100, apply the DC supply followed by the AC source, and the output relay should operate in 97 to 103 seconds.
- **"*K*" setting**: Set the time to 990 the Tap Switch to 10 and set *K* to 2, turn on the DC and then apply 2 A to phase A the relay should operate in 86 to 129 seconds. If the relay should fail any of the above tests refer to the trouble shooting section for expanded test and calibration instructions.

## TROUBLESHOOTING

**Adjust Negative-Sequence Network:**

**CAUTION:**
**This adjustment requires special equipment (see Figure 19) when setting alarm unit for less than 3% and trip unit for less than 5%.**

Remove the cover from the printed circuit card cage. Use the test setup of Figure 19. Adjust the accurate three-phase source to provide pure positive sequence to the relay. Each phase current should be 4.9 A and each phase current should be 120° from the others. The amplitude must be accurate within ±0.2%, and the phase must be accurate within ±0.2°. Set the SGC current switch to the 4.9 A position. Adjust trimmers R6 and R9 on card 1 (negative-sequence analog board) for minimum DC voltage on the meter. The minimum must be below 15 mV.

**Check Response to Negative-Sequence (normal three-phase sources are adequate):**

Switch the connections between the "A" input and the "B" input. The voltmeter should read 2.5 V ±10% with the switch setting of #10 and 4.9 A applied.

Check the operation of the current-selection switch as follows. It is initially set at 4.9 A so that 4.9 A gives 2.5 V DC on the meter. As the current-selection switch is varied and the current is maintained at 4.9 A, the DC voltage readings shown in the table below should be obtained:

| SWITCH SETTING | EQUIVALENT PER UNIT CURRENT | | VOLTAGE ±10% |
|---|---|---|---|
| | 5 A UNIT | 1 A UNIT | |
| 10 | 4.9 A | 0.98 A | 2.50 V |
| 9 | 4.7 A | 0.94 A | 2.61 V |
| 8 | 4.5 A | 0.90 A | 2.70 V |
| 7 | 4.3 A | 0.86 A | 2.85 V |
| 6 | 4.1 A | 0.82 A | 3.00 V |
| 5 | 3.9 A | 0.78 A | 3.15 V |
| 4 | 3.7 A | 0.74 A | 3.31 V |
| 3 | 3.5 A | 0.70 A | 3.50 V |
| 2 | 3.3 A | 0.66 A | 3.71 V |
| 1 | 3.1 A | 0.62 A | 3.95 V |

Change the current-selection switch back to 4.9 A. Increase the input current to 9.8 A and meter M should read 4.6 to 5.5 V.

**Test Alarm and Trip Threshold:**

Short two of the three relay-input CTs to neutral (disconnect from generator). Set the alarm and the trip levels to the values in Table V below.

NOTE: The faceplate markings for the alarm and trip settings are approximate. To ensure that the desired setting has been made, the setting must be checked by test.

The 2% alarm setting falls between the minimum (fully CCW position) and 3% settings.

| ALARM SETTING | TRIP SETTING | ALARM OPERATES AT | | TRIP OPERATES AT | |
|---|---|---|---|---|---|
| | | CURRENT IN | METER READING | CURRENT IN | METER READING |
| 2 | 4 | 0.220 to 0.375 A | 40 to 60 mV | 0.52 to 0.75 A | 90 to 115 mV |
| 20 | 40 | 2.3 to 3.5 A | 0.45 to 0.54 mV | 5.4 to 7.0 A | 0.90 to 1.15 mV |

**Test Operate Times:**

Using the same set up as described above (Figure 19), set the *K* dial to 40, the alarm knob to 2% and the trip knob to 4%. Set the AC input 20% above the point where the trip LED just comes on. Set the time thumb switches to the desired value. Turn off DC power to the relay. Apply DC power. Wait approximately 10 seconds; then apply AC and time the interval before the trip LED lights. This test should be run for all the time values in the table below:

| TIME SETTING | TIME TO TRIP |
|---|---|
| 10 seconds | 8.3 to 11.3 seconds |
| 40 seconds | 38 to 42 seconds |
| 70 seconds | 67 to 73 seconds |
| 80 seconds | 77 to 83 seconds |
| 100 seconds | 97 to 103 seconds |
| 400 seconds | 388 to 412 seconds |
| 700 seconds | 679 to 721 seconds |
| 800 seconds | 768 to 824 seconds |

**"K" Setting**

Set the time thumb switches to 990 seconds. Set the K dial and the AC input current (*I*) (one phase only) to the values in the table below and verify that the external trip LED operates in the time shown. DC must be turned off, then on, between tests to reset the *K* counter. Trip level must be well below the test value of AC; note the time from the application of AC to the relay until trip LED operates (if adjustment is needed, R64 and R67 are on the Squarer Circuit Board).

| K Dial | Current In * | Operate Time |
|---|---|---|
| 2 | 2 A | 86 to 130 seconds<br>Adjust R64 (bottom) |
| | 15 A | 1.7 to 2.5 seconds |
| 20 | 15 A | 15 to 24.2 seconds<br>Adjust R67 (top) |
| 40 | 15 A | 30 to 50 seconds |

* Note that $I_2$ (negative sequence) = 1/3 *I*

**Check Three Second Alarm Delay:**

Set the alarm knob to 2%. Set the single input current to 3 A. Turn off the AC input to the relay for 20 seconds. Turn on the AC and time the interval until the external alarm LED comes on. This interval should be 2.5 to 4 seconds.

**Check DC Supervision Operation (relay set for 48 volt operation):**

With the alarm LED lit as above, drop the DC supply voltage to the SGC until the alarm telephone relay drops out. Measure the DC supply voltage. It should be 30 to 31 V. If this voltage is out of limits, then trimmer R17 on the power supply board must be adjusted. The relay must be removed from its case for this adjustment. Set the supply voltage to 31 V. Adjust R17 while monitoring the +48 V (varies 30 to 60 V) from the supply. R17 should be set so the output is just "on" at 31 V and drops out at any supply voltage below 31 V.

Since the SGC21C has no alarm relay, the DC supervision must be tested by monitoring the supply voltage to the trip relay while the DC input is varied.

## INSTALLATION

### RELAY SET-UP PROCEDURE

- **Power Supply**: It is necessary to set the jumpers on the power supply to match the supply (control) voltage. These jumpers are marked on the power supply card, or refer to Figure 13 for their position.
- **Current-Selection Setting**: The desired current setting must be computed as described in the APPLICATION section. When this has been done, the switch on the board (analog and negative-sequence) must be set accordingly.
- **Alarm and Trip Settings**: These are front panel controls and should be set as described in the CALCULATION OF SETTINGS section.
- **"K" Setting**: The setting of this control depends on the generator heating characteristics. This is discussed in the APPLICATION and CALCULATION OF SETTINGS sections.
- **Time Trip Set**: This setting controls the time required for tripping when the negative-sequence component barely exceeds the trip level. This is discussed in the APPLICATION and CALCULATION OF SETTINGS sections.

### VERIFICATION OF SETTINGS

When calibrating the controls, make sure the current tap switch is in the desired position before calibrating.

To test the time trip it is necessary to set in the desired time, then slightly exceed the trip level and begin timing the actuation of the trip relay. This time should match the time setting.

Testing the operation of the *K* trip requires computing a trip time for a particular negative-sequence input for the desired K setting. This negative sequence can be applied and the time-to-trip measured. Increasing the *K* setting will increase trip time and vice versa.

In both cases above, it is **essential** that the time and *K* counters both start at zero. Turn the DC power "off" and then "on" to zero them.

The **alarm** and **trip** thresholds may be set precisely by applying to the relay the negative-sequence current at which they are to operate, and adjusting them to just operate. Applying a known amount of negative-sequence current may be accomplished by applying a single-phase current to any input current transformer. The negative-sequence component is 1/3 of the applied current. The input current contains other sequence components but they are rejected by the relay.

DO NOT try to adjust the negative-sequence network using this negative-sequence current technique. Pure positive sequence is required for this adjustment, which can be found under ELECTRICAL TESTS procedures.

## PERIODIC CHECKS AND ROUTINE MAINTENANCE

It is recommended that relays in operation be tested once a year by repeating the acceptance test procedures. Relays stored for a year or more should be tested prior to installation using the ACCEPTANCE TEST procedures.

## SERVICING

**CAUTION:**
**Remove ALL power from the relay before removing or inserting any of the printed circuit boards. Failure to observe this caution may result in damage to and/or misoperation of the relay.**

Should the relay fail to operate, check that the power supply indicator is on. If it is not, there may be no DC control voltage applied to the relay. If DC is present, the power supply board may be defective, and a new one should be tried.

If the power supply indicator is on, and the relay does not operate, check that all the power supply output voltages are present on the power supply card test points.

If the power supply voltages are satisfactory, the problem may be in card 1, the analog and negative-sequence card. Try a new card.

If only the time trip works, try new cards 2 and 3, the squarer and the K cards. If only the *K* trip works, try a new card 4, the timer card.

If none of these measures solves the problem, then conventional troubleshooting techniques can be used. Note that substitution or readjustment of card 1 can reduce the relay accuracy, so recalibration will be required. Specialized test equipment is required to adjust card 1, the analog and negative-sequence board.

An extender board is available for servicing. Order board extender 0184B5645.

## RENEWAL PARTS

It is recommended that sufficient quantities of renewal parts be carried in stock to enable the prompt replacement of any that are worn, broken or damaged.

Should a printed circuit card become inoperative, it is recommended that this card be replaced with a spare. In most instances, the user will be anxious to return the equipment to service as soon as possible and the insertion of a spare card represents the most expeditious means of accomplishing this. The faulty card can then be returned to the factory for repair or replacement.

Although it is not generally recommended, it is possible with the proper equipment and trained personnel to repair cards in the field. This means that a troubleshooting program must isolate the specific component on the card that has failed. By referring to the internal connection diagram for the card, it is possible to trace through the card circuit by signal checking and, hence, determine which component has failed. This, however, may be time consuming and if the card is being checked in place in its unit, as is recommended, will extend the outage time of the equipment.

**CAUTION:**

**Great care must be taken in replacing components on the cards. Special soldering equipment suitable for use on the delicate solid-state components must be used and, even then, care must be taken not to cause thermal damage to the components, and not to damage or bridge over the printed circuit buses. The repaired area must be re-covered with a suitable high dielectric plastic coating to prevent possible breakdowns across the printed circuit buses due to moisture or dust.**

**Dual in-line integrated circuits are especially difficult to remove and replace without specialized equipment. Furthermore, many of these components are used in printed circuit cards that have bus runs on both sides. These additional complications require very special soldering equipment and removal tools as well as additional skills and training that must be considered before field repairs are attempted. Some of the integrated circuits are static sensitive.**

When ordering renewal part, address the nearest Sales Office of the General Electric Company, specify quantity required, name of the part wanted, and the complete model number of the relay for which the part is required.

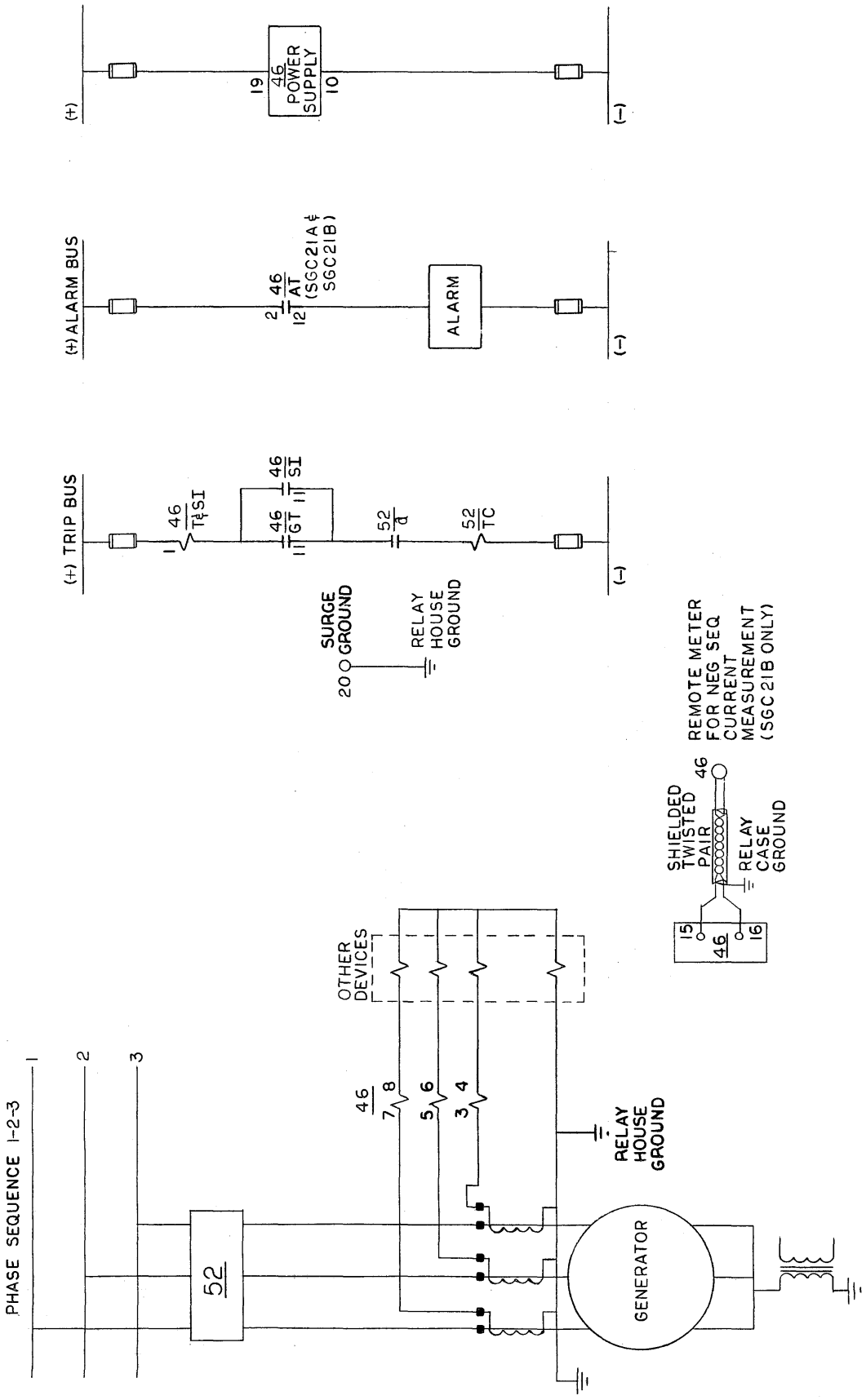



**Figure 1 (0165B2496): TYPICAL ELEMENTARY DIAGRAM**

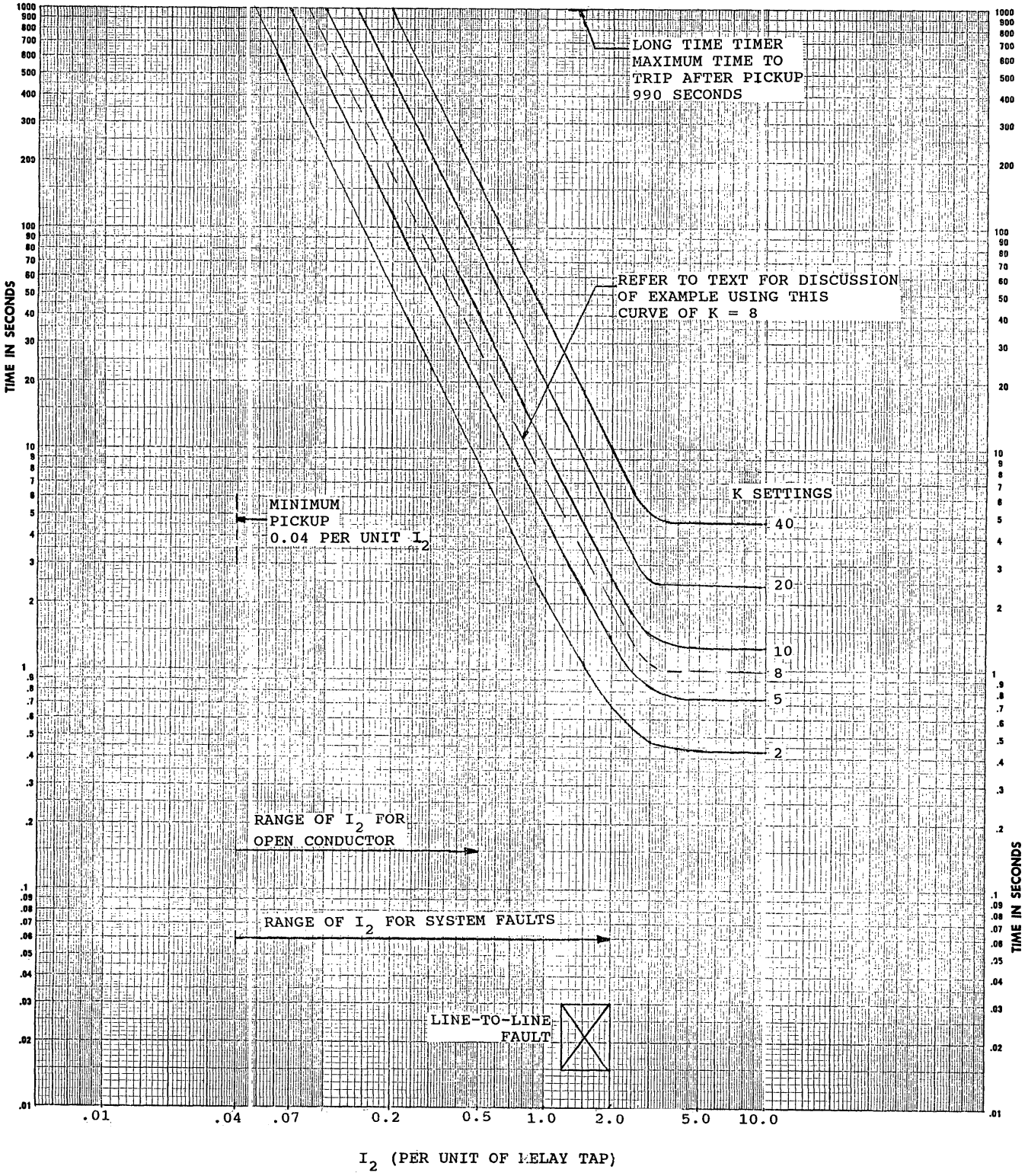



**Figure 2 (0138B7691): SGC21 TYPICAL TIME OVERCURRENT CURVES**

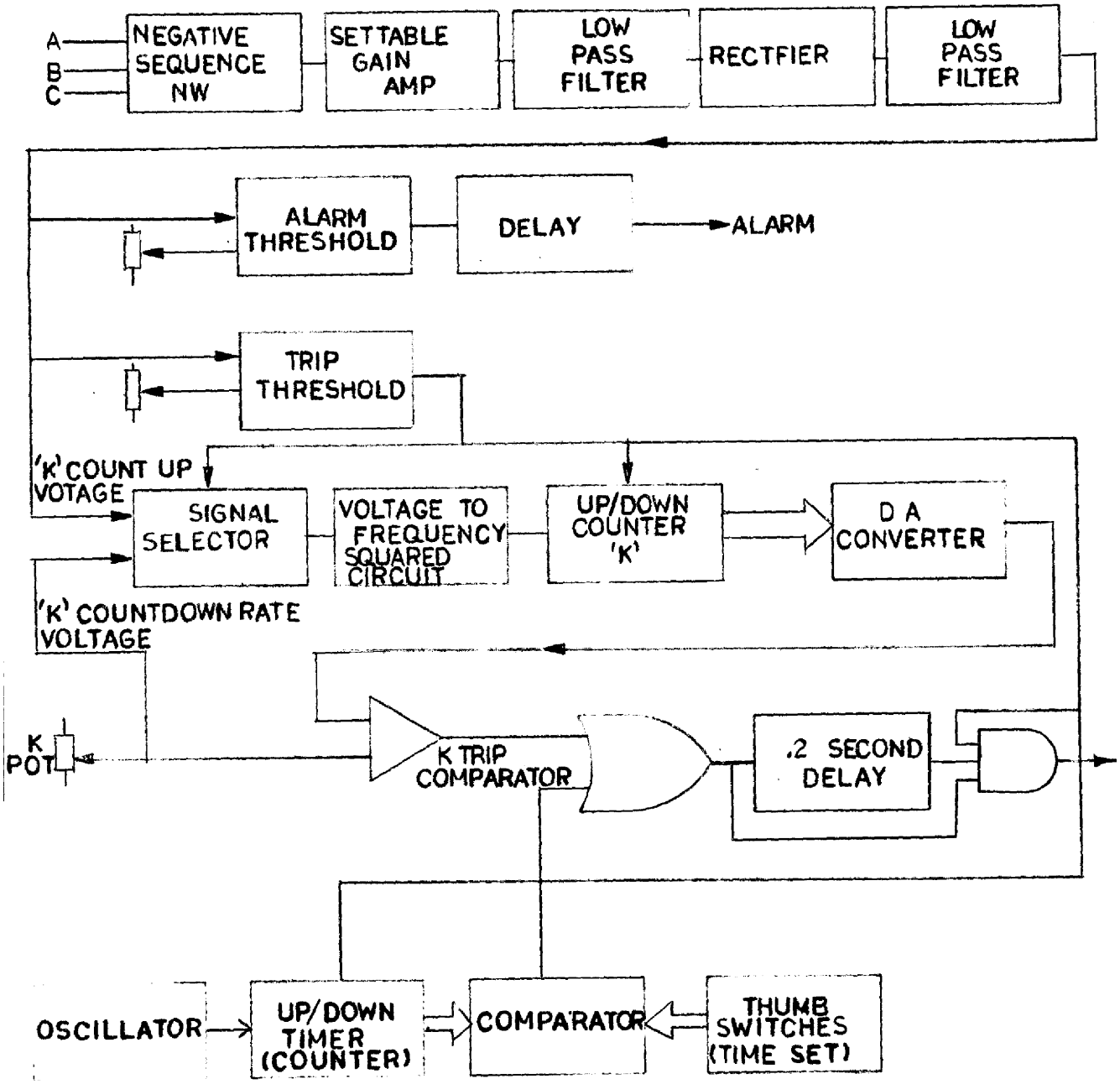



**Figure 3 (0285A7029): FUNCTIONAL BLOCK DIAGRAM**

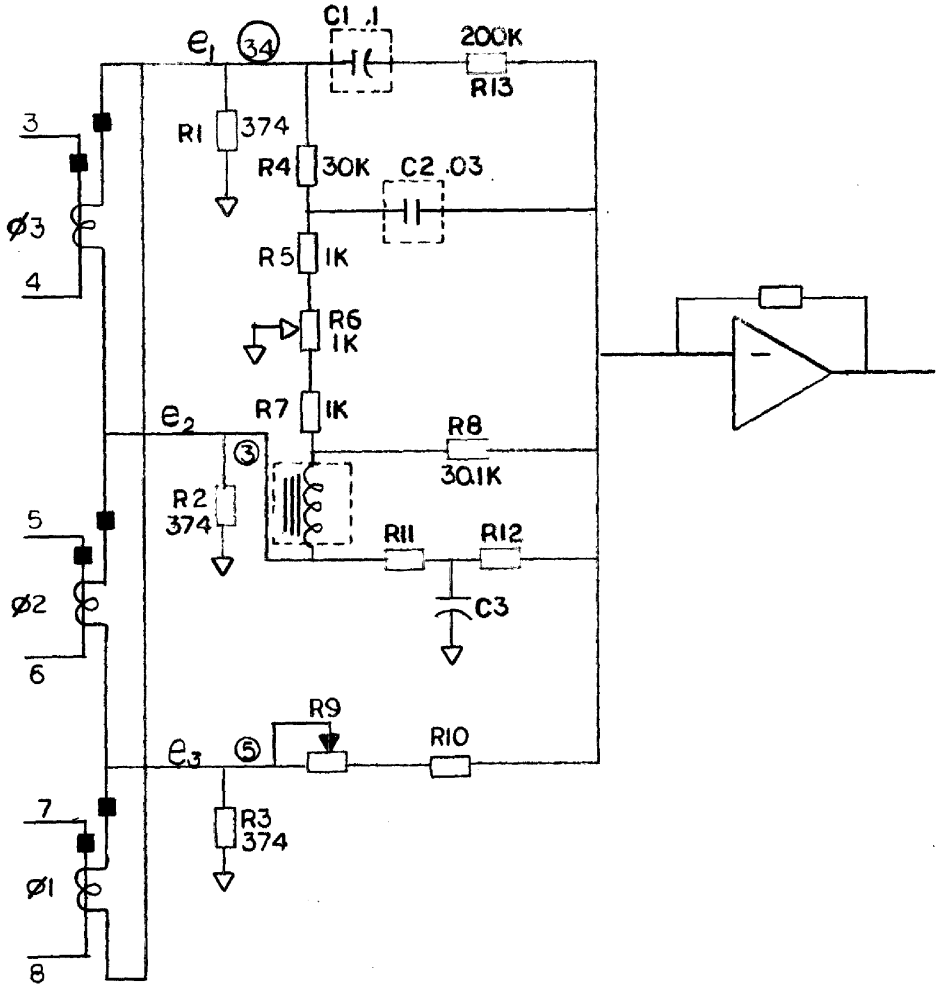



**Figure 4 (0285A7030): SIMPLIFIED NEGATIVE-SEQUENCE NETWORK DIAGRAM**

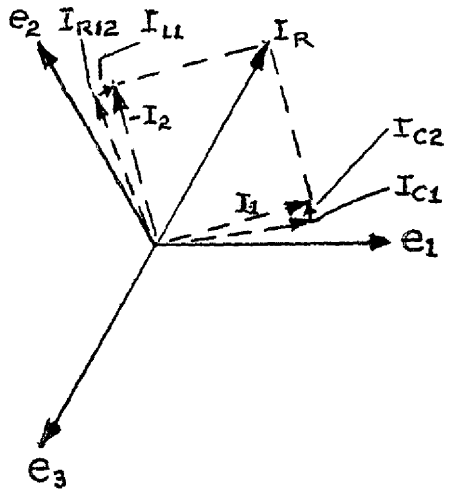



**Figure 5 (0285A7031A): NEGATIVE-SEQUENCE PHASOR DIAGRAM**

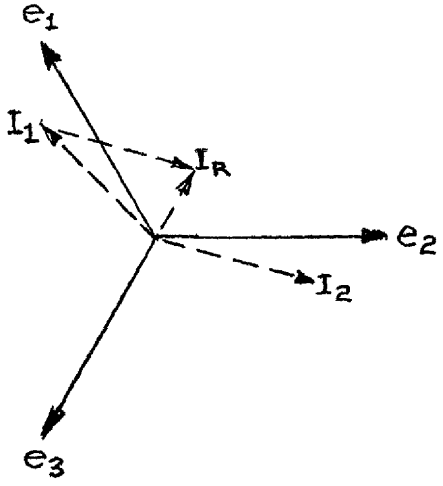



**Figure 6 (0285A7031B): REVERSED-PHASE-SEQUENCE PHASOR DIAGRAM**

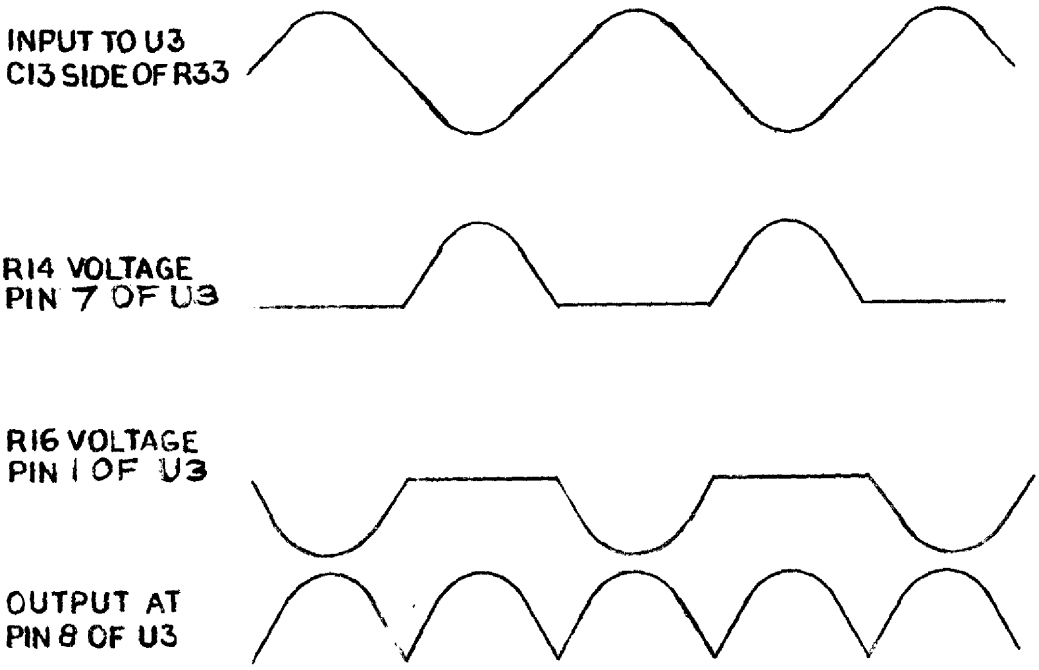



**Figure 7 (0285A7032): PERFECT RECTIFIER OPERATION**

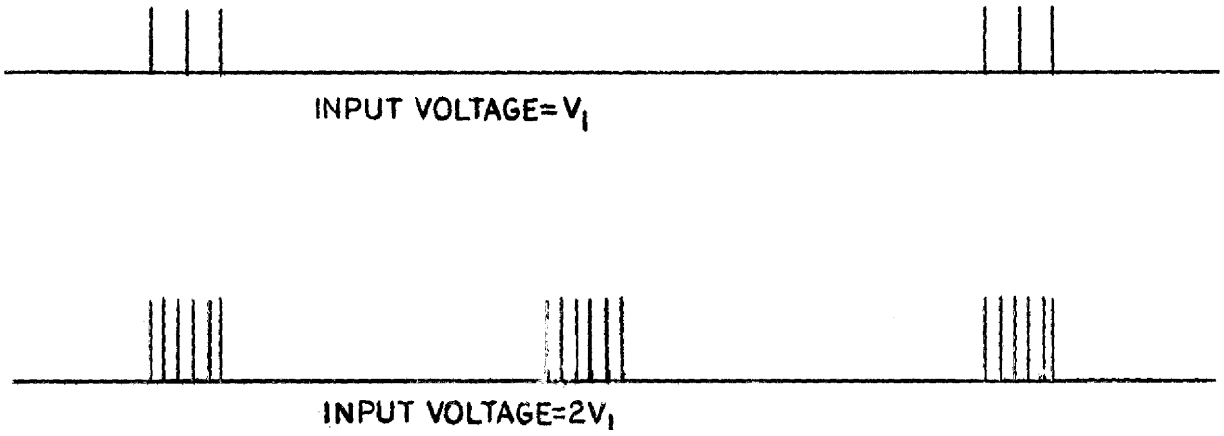



**Figure 8 (0285A7033): SQUARER OUTPUT WAVEFORMS**

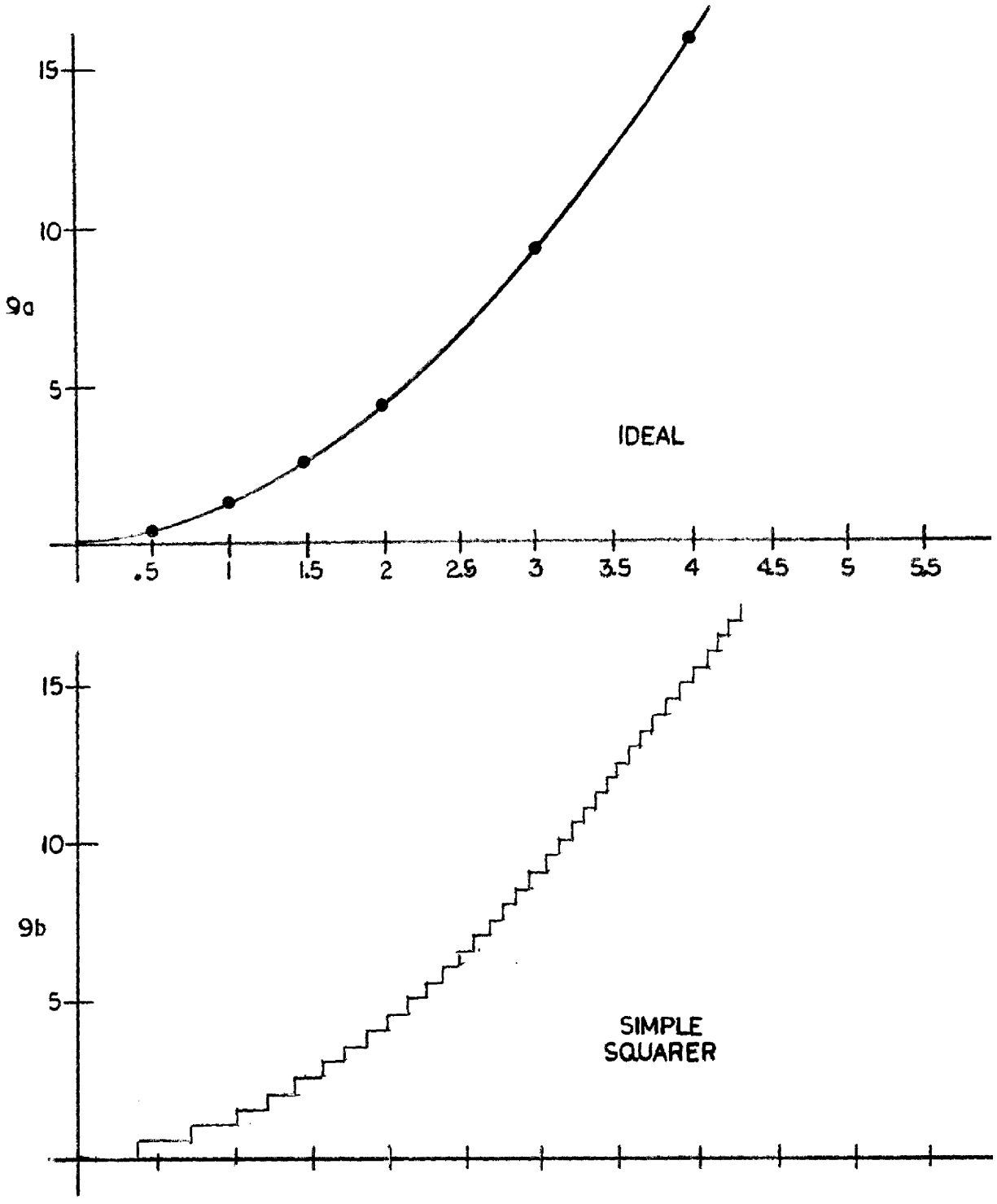



**Figure 9 (0285A7034): IDEAL vs. SIMPLE SQUARER OUTPUT WAVEFORMS**

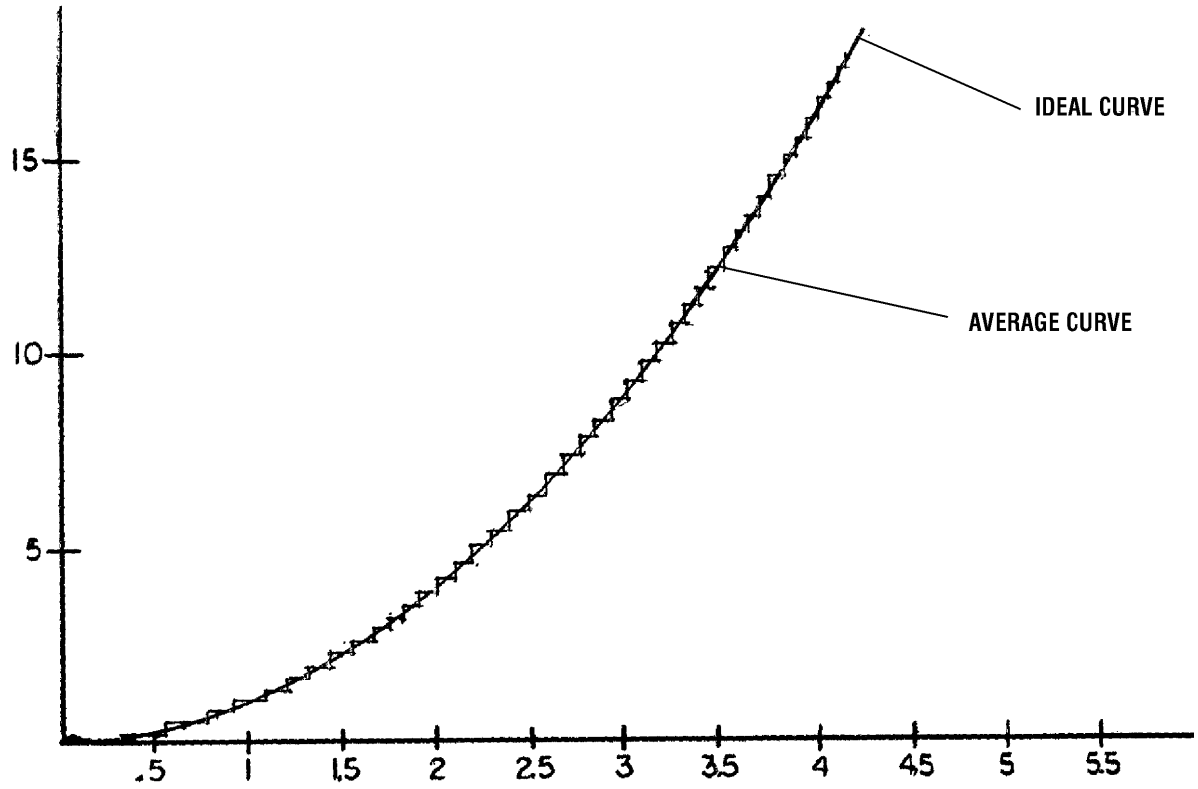



**Figure 10 (0285A7036): IDEAL and AVERAGE PULSE RATE vs. NEGATIVE-SEQUENCE CURRENT**

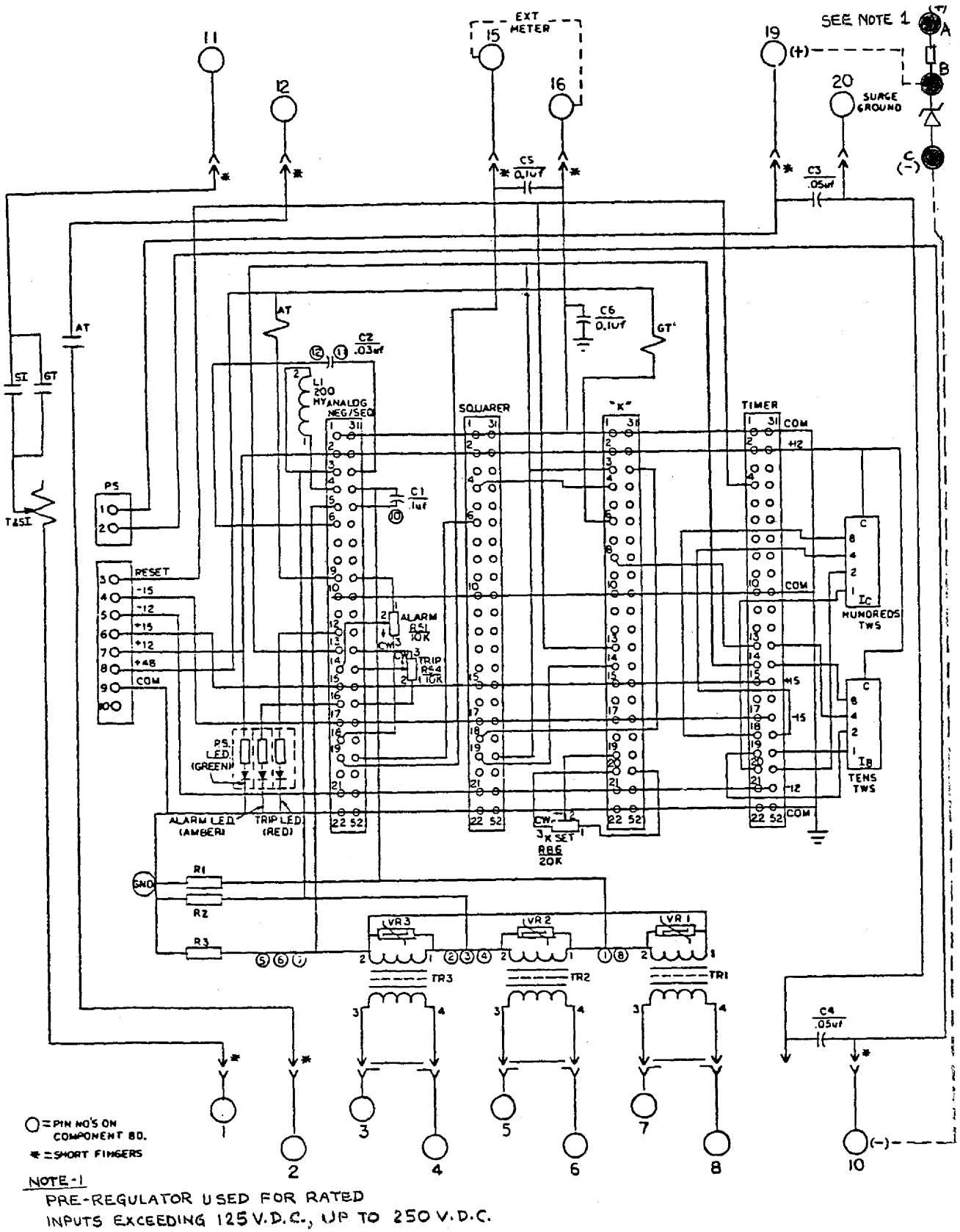



**Figure 11 (0285A5866): INTERNAL CONNECTIONS DIAGRAM FOR SGC21A/21B RELAYS**

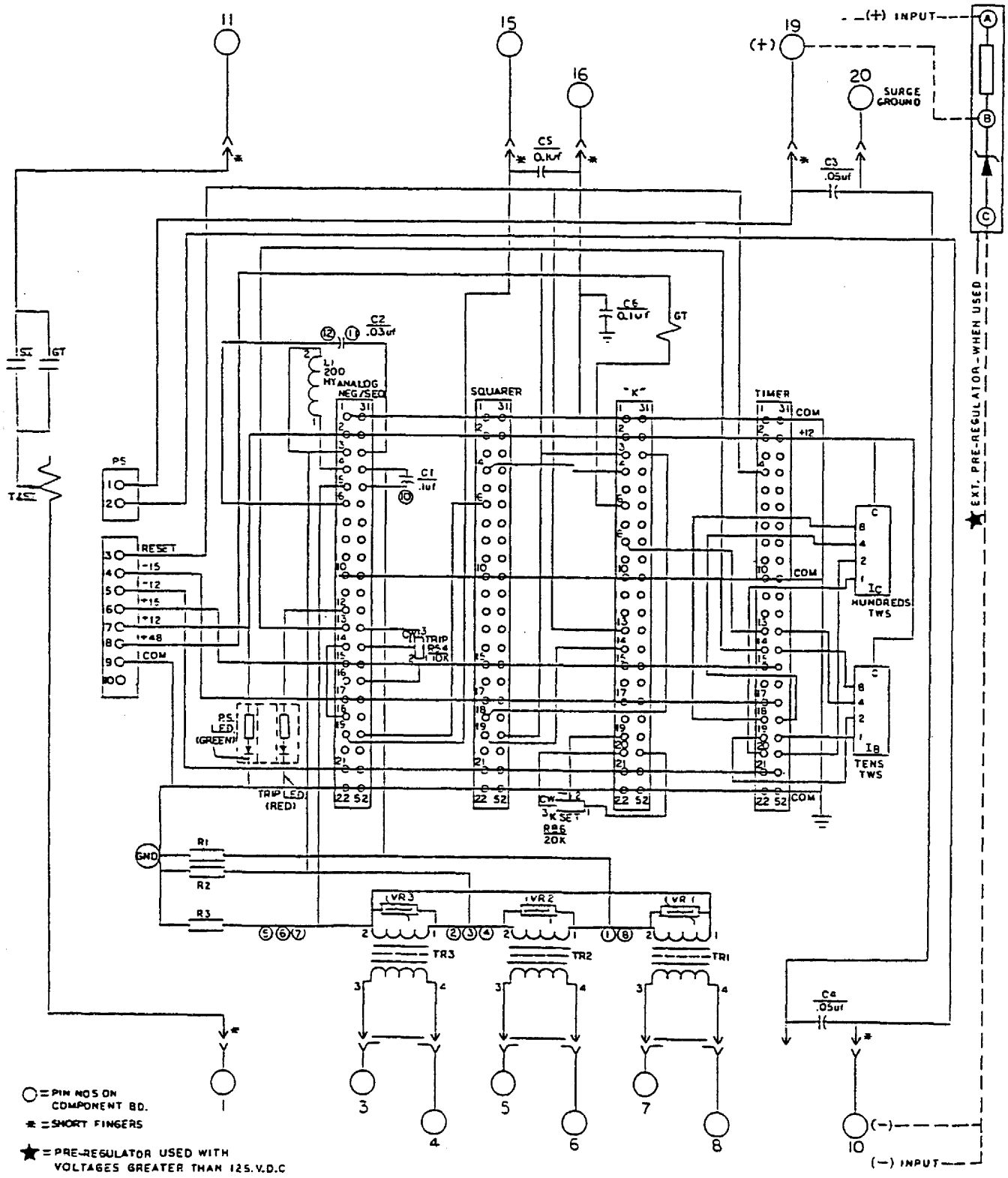



**Figure 12 (0285A5869): INTERNAL CONNECTIONS DIAGRAM FOR SGC21C RELAYS**

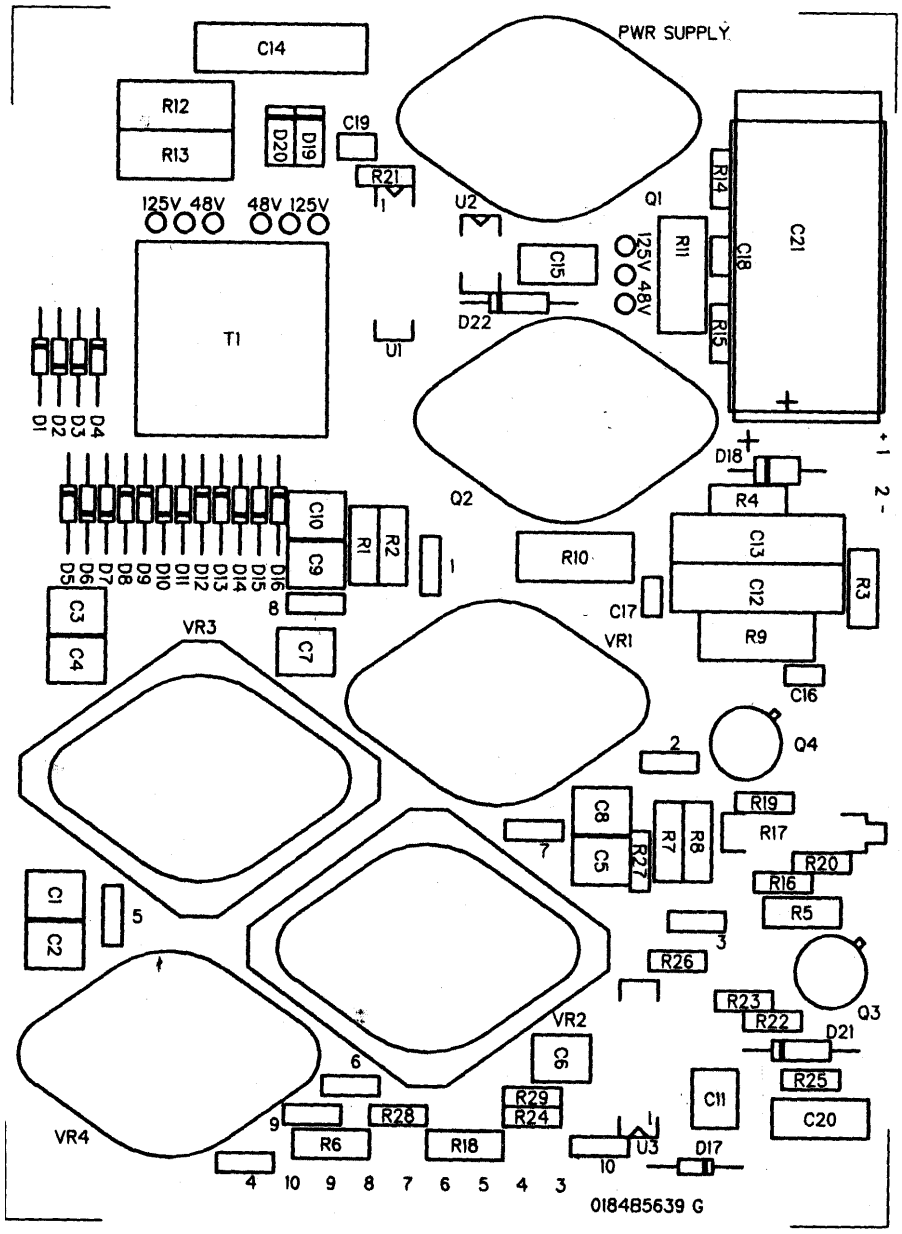
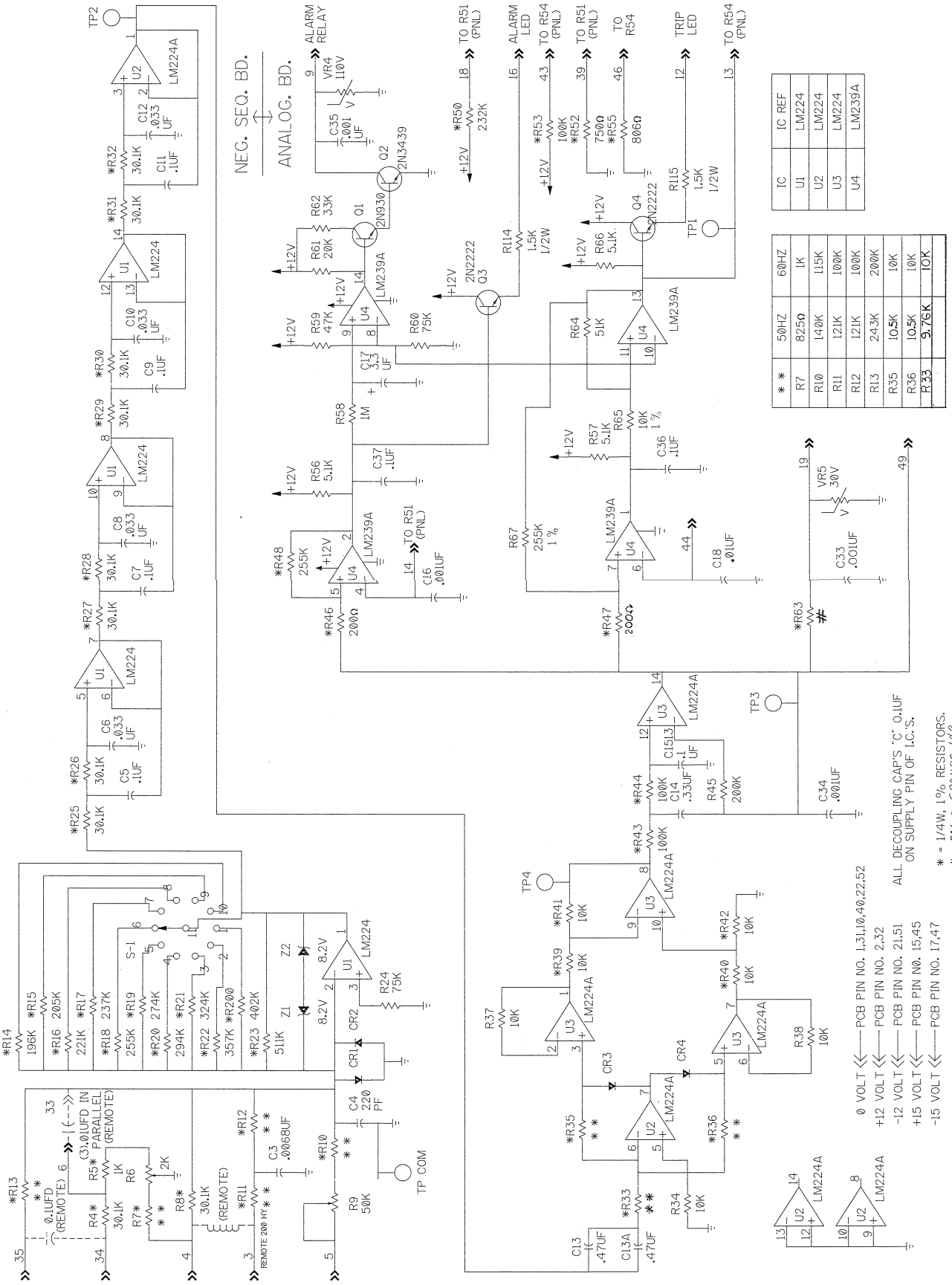



**Figure 13 (0179C7772 Sh.2): POWER SUPPLY ASSEMBLY**




| IC | IC REF |
|---|---|
| U1 | LM224 |
| U2 | LM224 |
| U3 | LM224 |
| U4 | LM239A |

| * * | 50HZ | 60HZ |
|---|---|---|
| R7 | 825Ω | 1K |
| R10 | 140K | 115K |
| R11 | 121K | 100K |
| R12 | 121K | 100K |
| R13 | 243K | 200K |
| R35 | 10.5K | 10K |
| R36 | 10.5K | 10K |
| R33 | 9.76K | 10K |

**Figure 14 (0179C6307): NEGATIVE-SEQUENCE / ANALOG BOARD INTERNAL CONNECTIONS DIAGRAM**

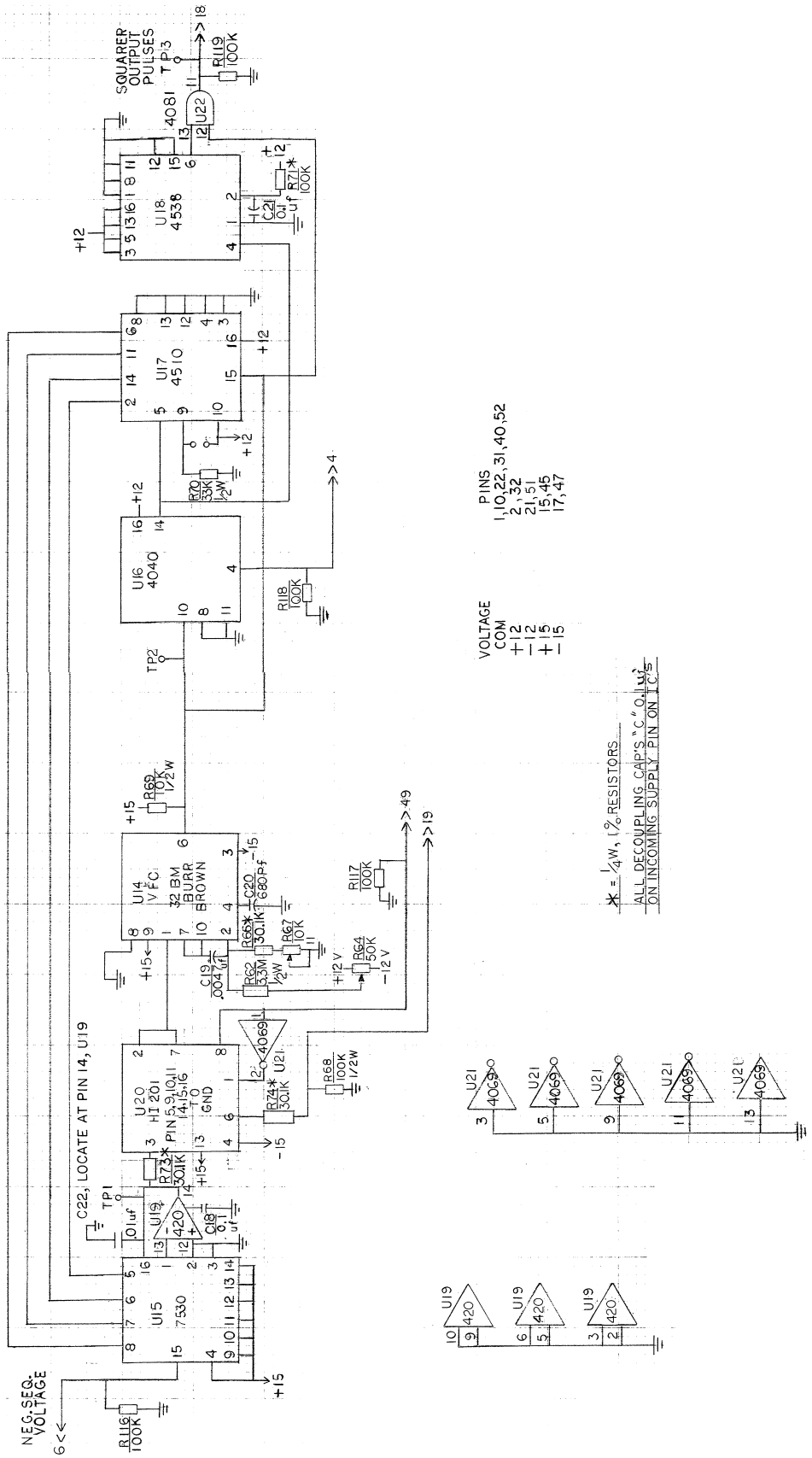



**Figure 15 (0179C6308): SQUARER BOARD INTERNAL CONNECTIONS DIAGRAM**

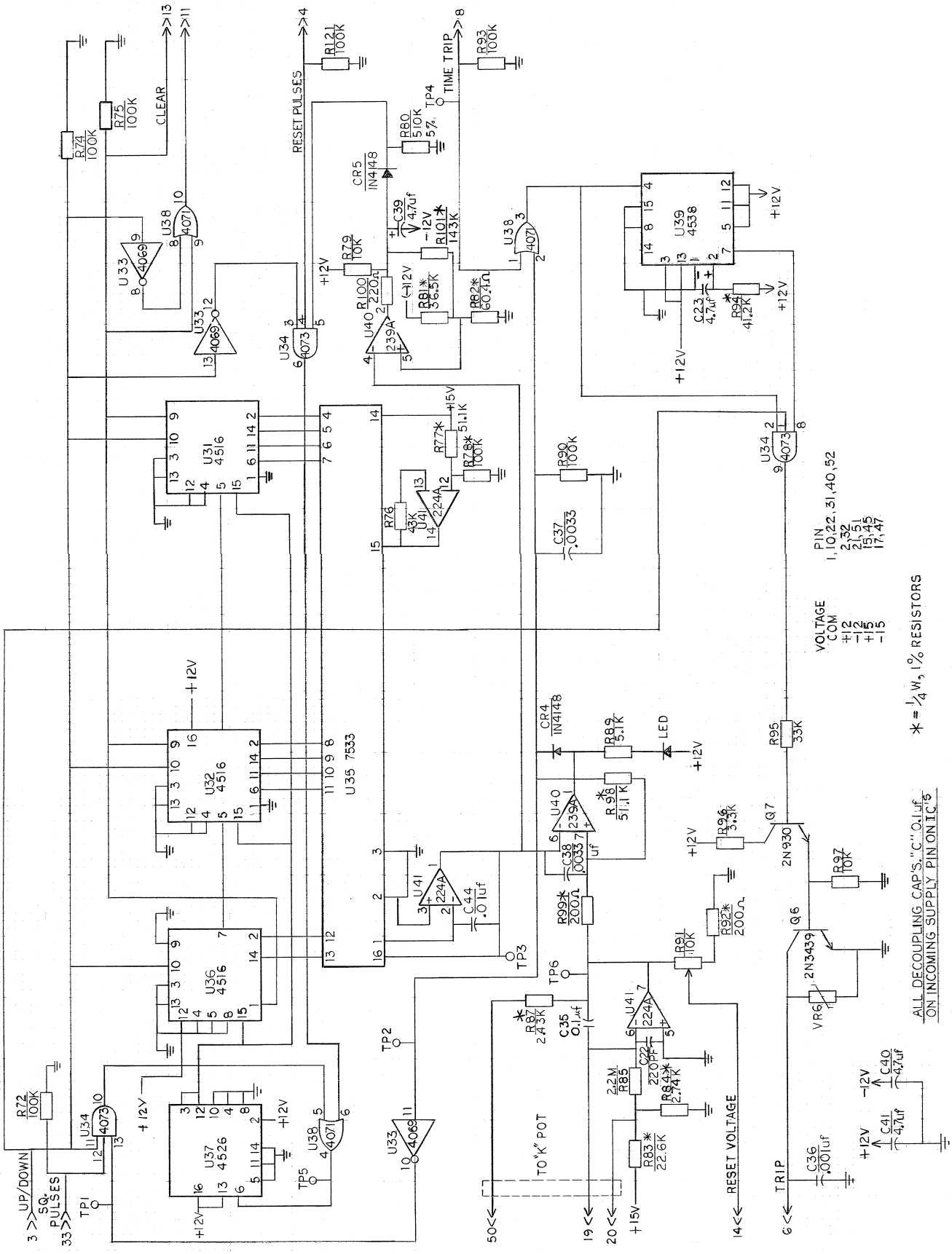



**Figure 16 (0179C6309): K BOARD INTERNAL CONNECTIONS DIAGRAM**

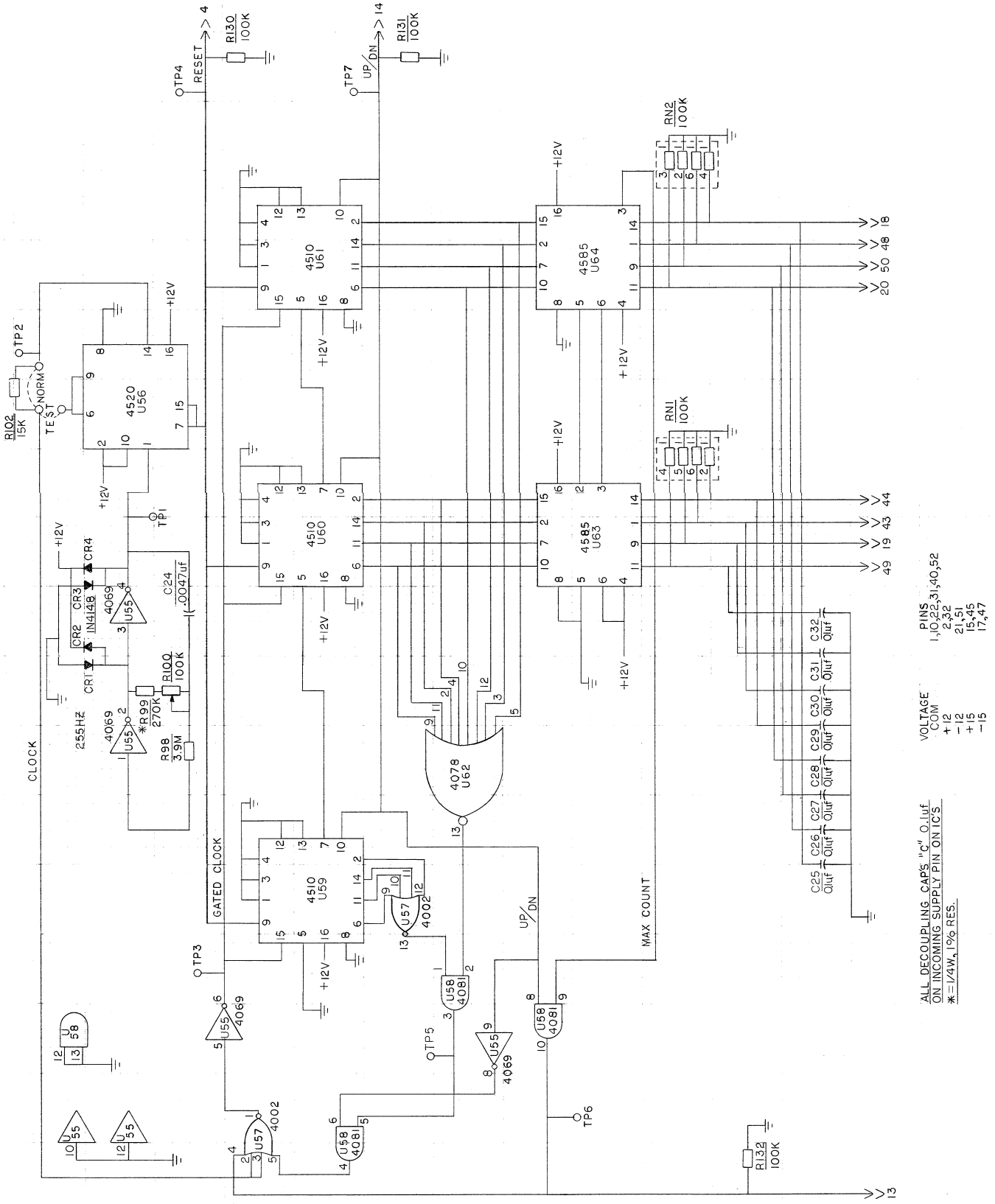



**Figure 17 (0179C6310): TIMER BOARD INTERNAL CONNECTIONS DIAGRAM**

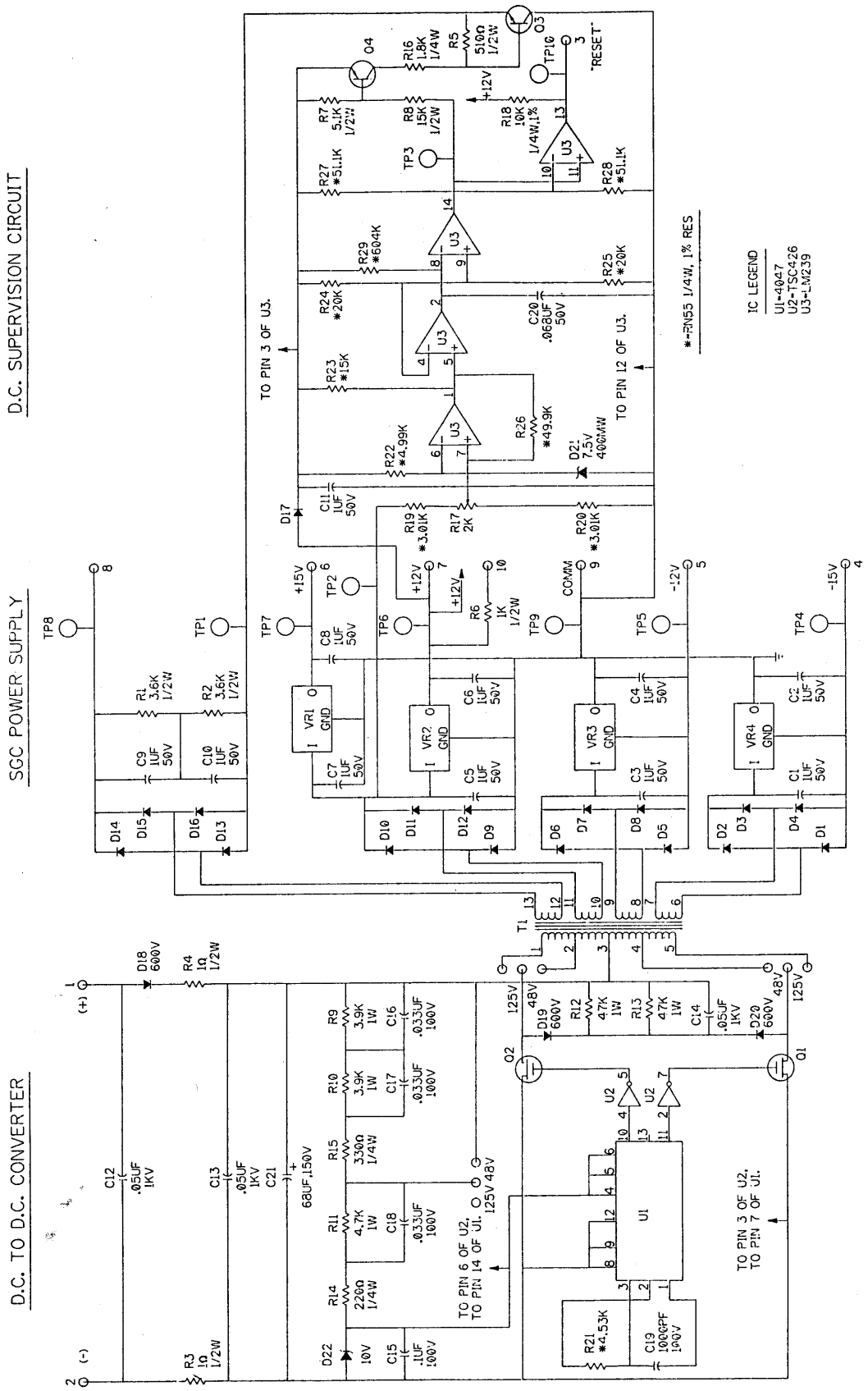



**Figure 18 (0172C5374): POWER SUPPLY INTERNAL CONNECTIONS DIAGRAM**

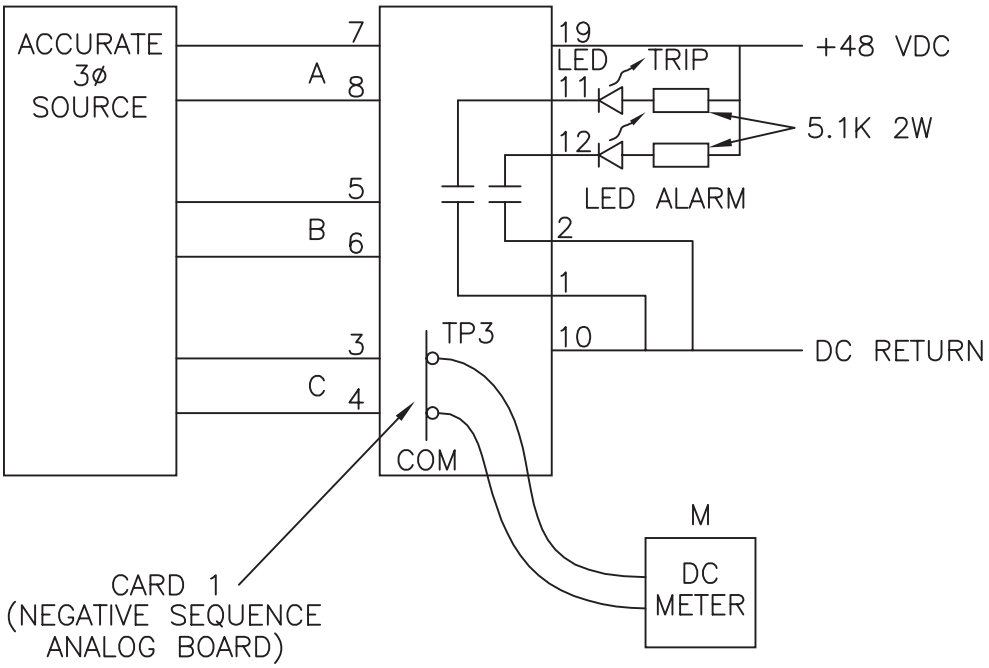



**Figure 19 (0285A7035): RELAY TEST SET-UP**

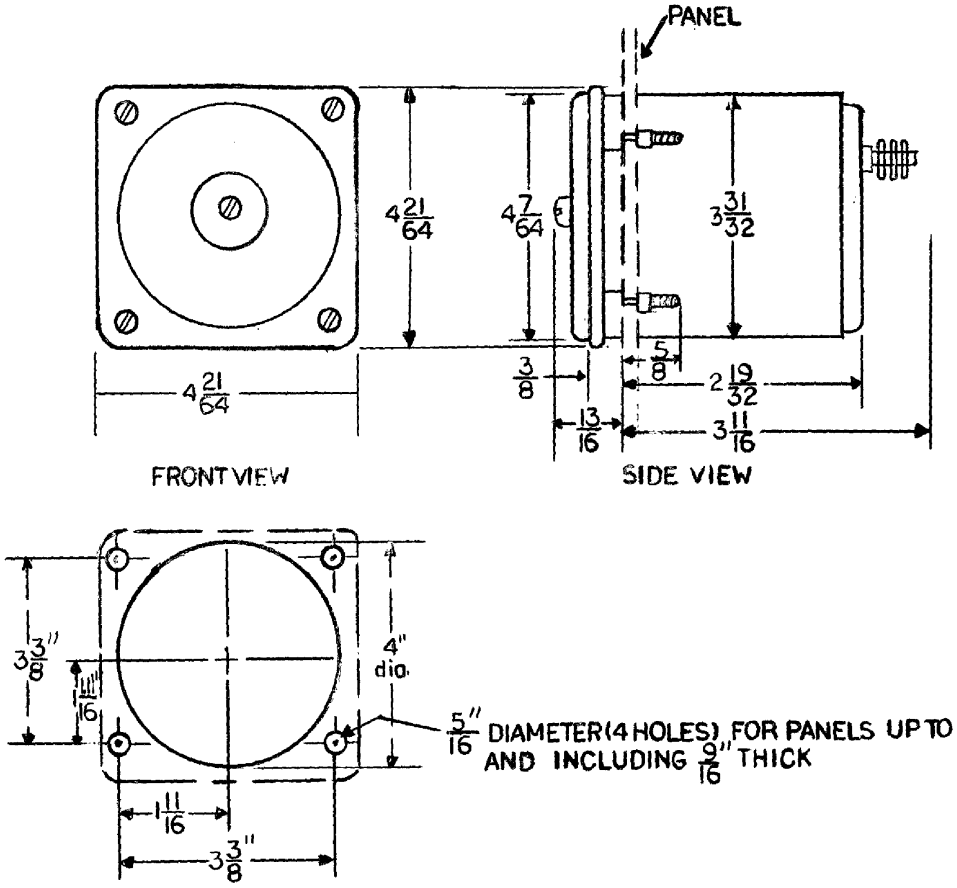



**Figure 20 (0285A7039): METER OUTLINE DRAWING**

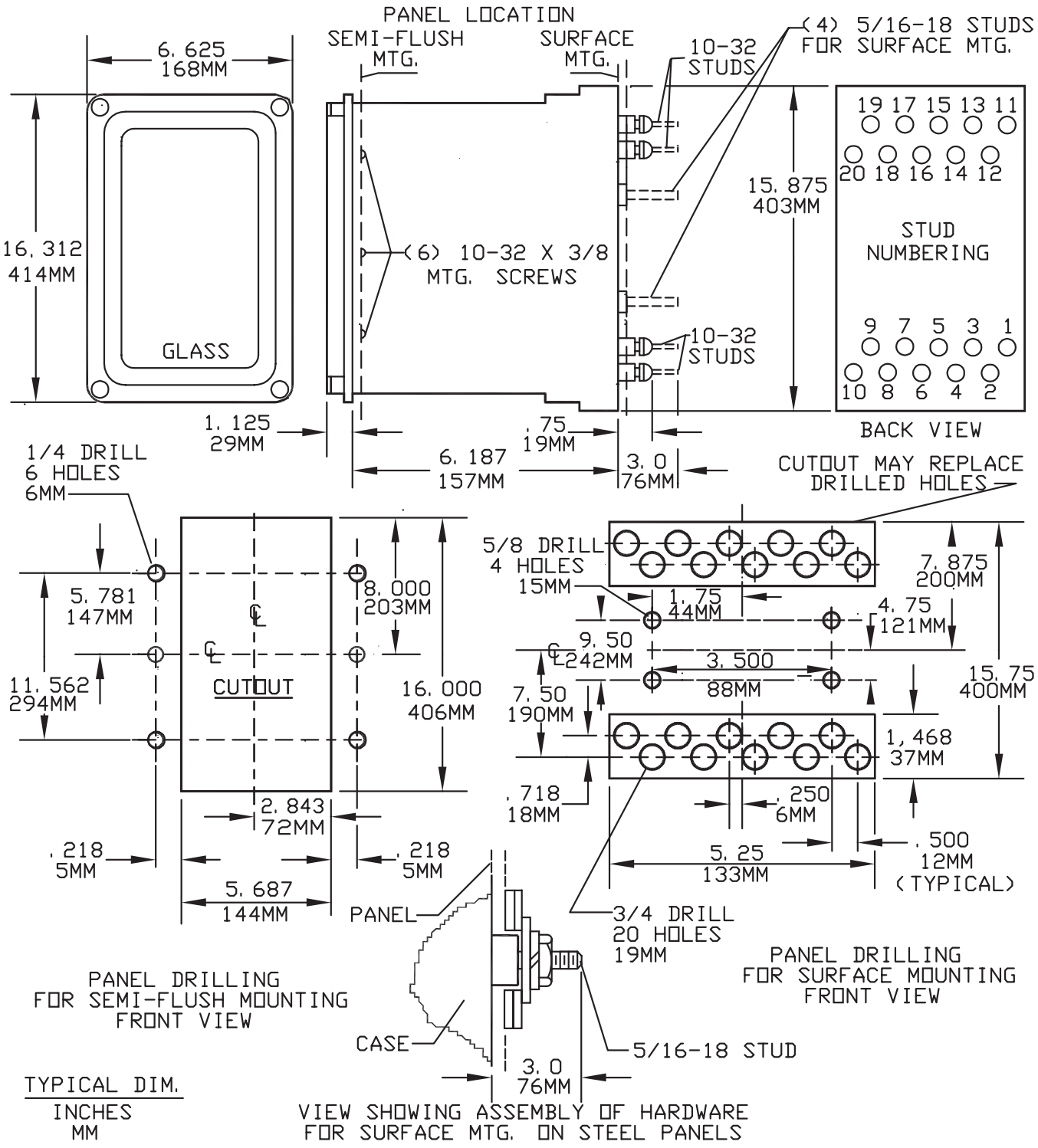



**Figure 21 (K-6209274-6): OUTLINE AND PANEL DRILLING DIMENSIONS**

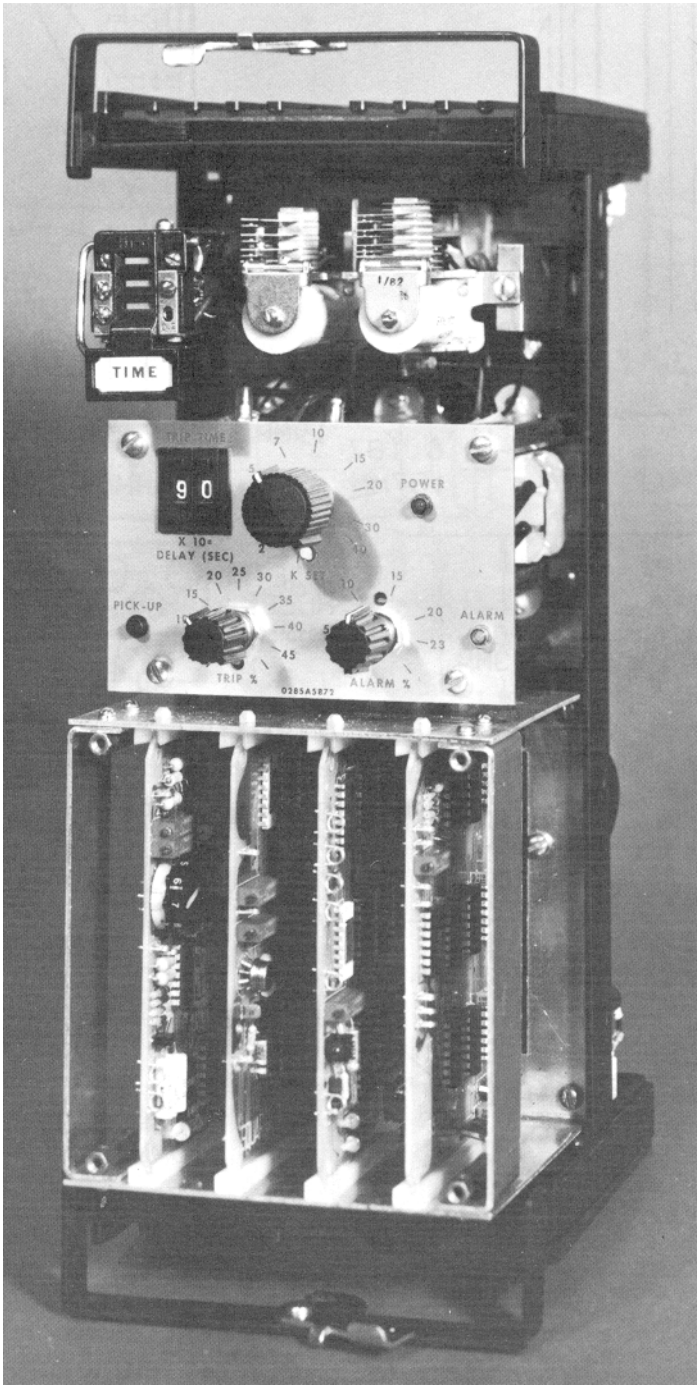



**Figure 22 (WAM7128302): FRONT VIEW WITHOUT CARD COVER**

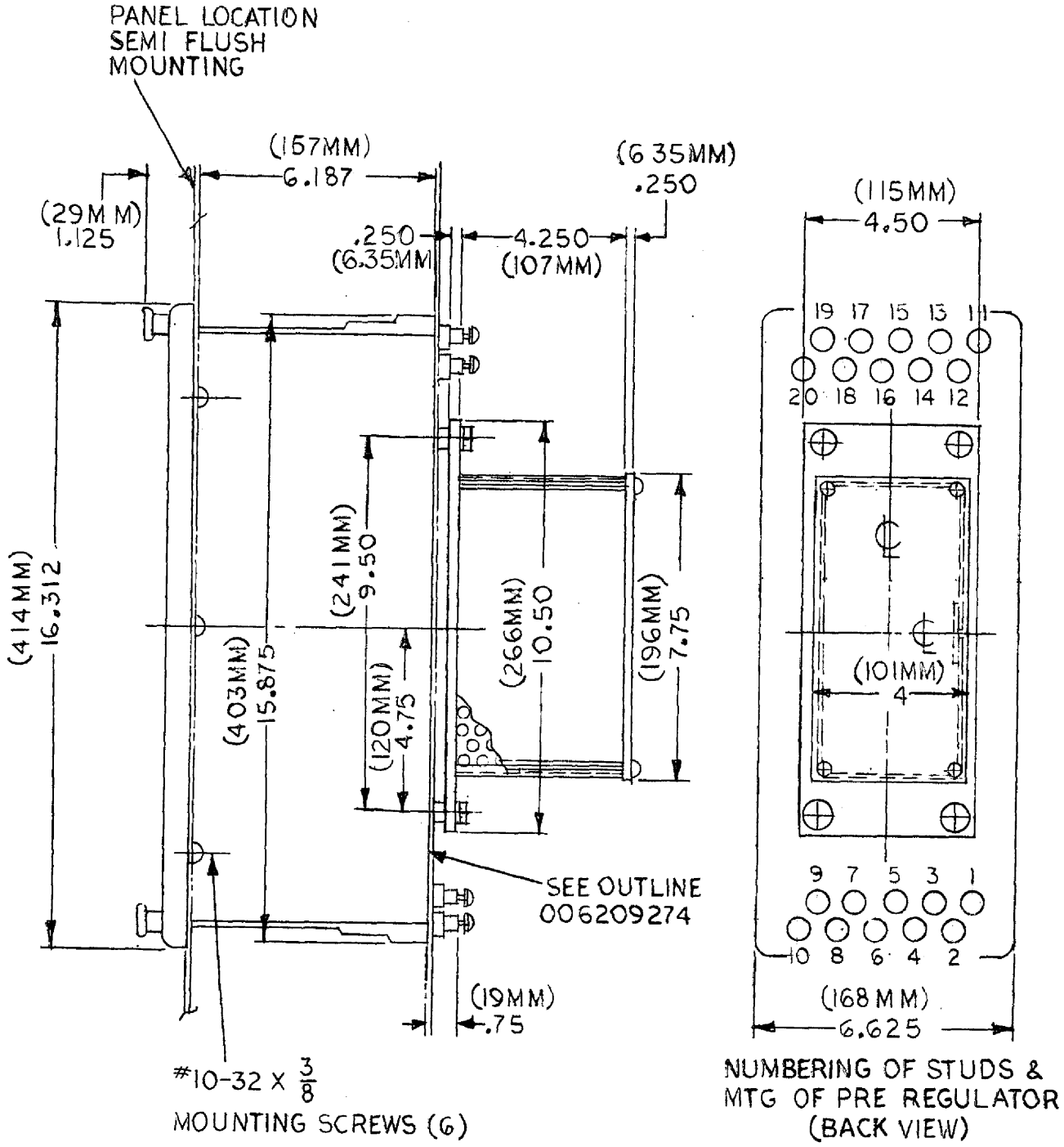
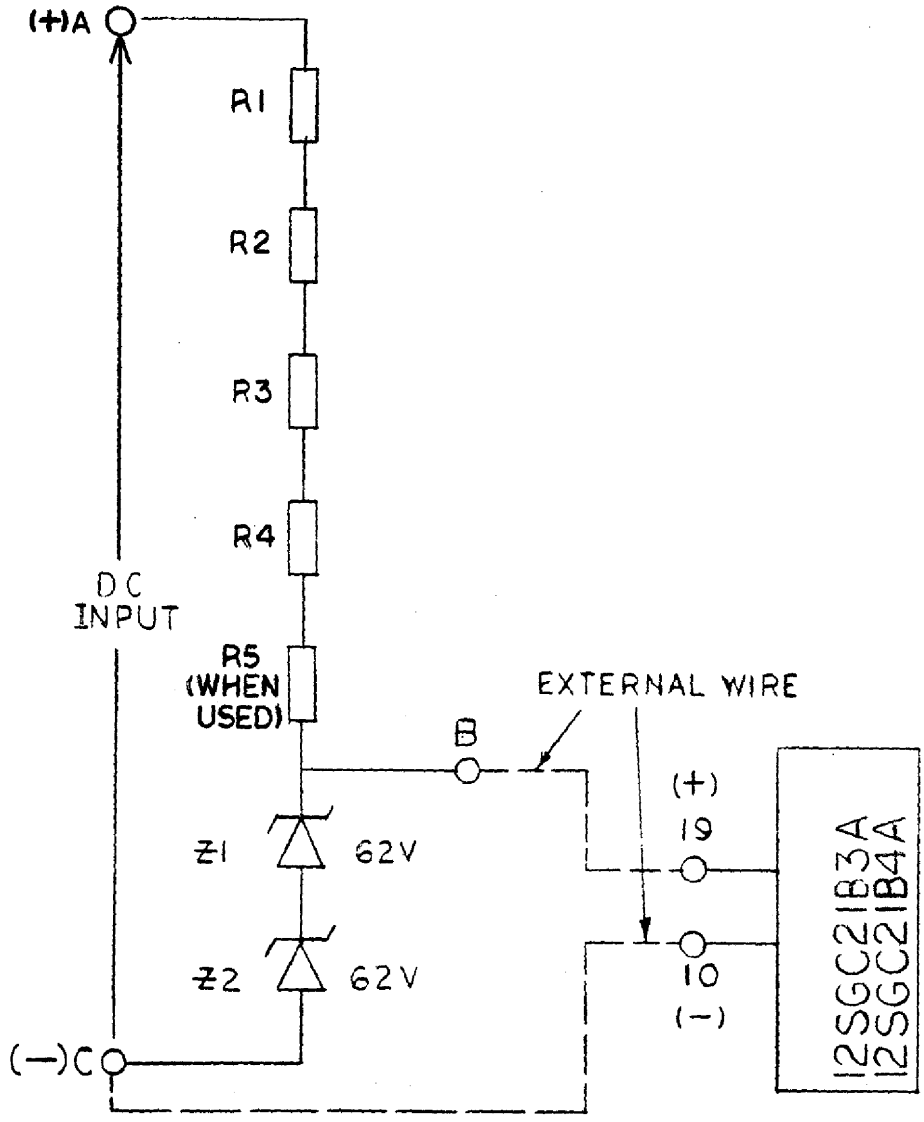



**Figure 23 (0285A5830): MOUNTING EXTERNAL PRE-REGULATOR TO RELAY CASE**




| DC INPUT | R1 | R2 | R3 | R4 | R5 |
|---|---|---|---|---|---|
| 220 VOLTS | 100Ω | 100Ω | 100Ω | 100Ω | — |
| 250 VOLTS | 100Ω | 100Ω | 100Ω | 75Ω | 75Ω |

**Figure 24 (0285A8224): ELECTRICAL CONNECTIONS OF PRE-REGULATOR TO THE RELAY**

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