SEL-2BFR, -2/BFR

BREAKER FAILURE RELAY AND MONITOR

INSTRUCTION MANUAL

20030207

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PM2BFR-01

Warning

This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.

ATTENTION!

Cet équipement est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement pourrait être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.

20001120

MANUAL CHANGE INFORMATION

The date code at the bottom of each page of this manual reflects the creation or revision date. Date codes are changed only on pages that have been revised and any following pages affected by the revisions (i.e., pagination). If significant revisions are made to a section, the date code on all pages of the section will be changed to reflect the revision date.

Each time revisions are made, both the main table of contents and the affected individual section table of contents are regenerated and the date code is changed to reflect the revision date.

Changes in this manual to date are summarized below (most recent revisions listed at top).

Revision Date	Summary of Revisions
20030207	Updated ***Appendix A: Firmware Versions in this Manual***.
20010515	Added information on the effect of 50FT pickup on IRIG-B operation in ***Section 2: Specifications*** and ***Section 5: Applications***.
990714	Changed footers on entire manual to reflect SEL-2BFR, -2/BFR. Added ***Model Variation Information*** to ***Section 1: Introduction***. Incorporated SEL-2BFR-2 ***Time Delayed Retrip*** Logic into ***Section 2: Specifications***. Modified AND and OR gate numbering in ***Section 2: Specifications***. Reformatted ***Settings Sheets*** at end of ***Section 5: Event Reporting***. Added ***Appendix C: SEL-BFR*** to explain SEL-BFR Relay differences.
990512	Clarified Figure 2.12 in ***Section 2: Specifications***. Updated ***Appendix A: Firmware Versions in this Manual***.
981019	Incorporated the following addenda into ***Section 1: Introduction***: "ACB Phase Rotation Option" and "50 Hz Options." Incorporated the following addenda into ***Section 2: Specifications***: "New SEL-200 Series Optical Isolator Logic Input Rating" and "SEL-2BFR/BFR Instruction Manual Addendum for 1 Amp Version and 50/60 Hz Relays." Incorporated the following addendum into ***Section 6: Installation***: "Jumper Installation Instructions." Updated Figures 6.3, 6.4, and 6.5.
970423	2BFR Specifications Addendum - Addition

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SECTION 1: INTRODUCTION

GETTING STARTED

This instruction manual applies to SEL-2BFR and SEL-2BFR-2 relays**.** ***Appendix C: SEL-BFR Specifications*** outlines the differences between the SEL-2BFR and legacy SEL-BFR relays. The hardware is identical for all SEL-2BFR relays.

If you are unfamiliar with the SEL-2BFR or SEL-2BFR-2 relays, we suggest that you read this section, then perform the Initial Checkout Procedure in ***Section 7: Maintenance & Testing***. For a more detailed understanding of the relay, we suggest that you read the following sections in the outlined order:

Section 2: Specifications for a description of the logic and how it works with logic inputs, the Relay Word, and relay outputs

Section 5: Applications for a description of breaker failure timing, an application outline that guides settings selection, and Settings Sheets.

Section 3: Communications for a description of the commands used to set the relay for protection, set the relay for control, obtain target information, obtain metering information, etc.

Section 4: Event Reporting for a description of event report generation, summary event reports, long event reports, and their interpretation.

OVERVIEW

Relay Features

The SEL-2BFR Breaker Failure Relay and Monitor performs many circuit breaker protective relaying, diagnostic, and data recording functions. The relay detects the following line circuit breaker failure modes:

- Failure to clear a fault (six available schemes).
- Failure to trip under load.
- Failure of the breaker auxiliary contact to indicate that the breaker tripped.
- Failure to complete trip sequence due to trip resistor(s) remaining inserted.
- Failure to complete close sequence due to close resistor(s) remaining inserted.
- Failure to close.
- Failure while open: breaker pole flashover detected.

Other features and capabilities include:

- Recording of summaries for the last 100 breaker operations.
- Fifteen-cycle event recording of the last nine operations.
- Alarm event history including slow trip, slow close, blown potential fuse, etc.
- Motor-Operated Disconnect (MOD) trip and power circuit breaker isolation security logic.
- Instantaneous or time-delayed retripping capability.
- User-selectable targets for operations and testing.
- Programmable Mask Logic for flexible application and testing.
- Metering.
- Communications ports for local and remote access.
- Automatic self-tests.
- Demodulated IRIG-B time code input port.
- Compact size.

Unique protection features and economy make the SEL-2BFR Relay an ideal breaker failure relay.

MODEL VARIATIONS

SEL-BFR

This manual is written for SEL-2BFR relays. For SEL-BFR relays, substitute SEL-BFR for each reference to SEL-2BFR. Refer to **.** ***Appendix C: SEL-BFR Specifications*** for SEL-BFR general specifications and drawings

SEL-2BFR Relay

The basic SEL-2BFR relay has all the features outlined in the preceding Overview.

2BFR-2 Relay

This variation adds a timer, RTSD (Retrip Seal-In Delay), to delay the seal-in of the trip input in the time-delayed retrip logic. This timer has a settable pickup time and instantaneous dropout time. You can set the pickup time to filter out undesirable transients, see ***Section 2: Specifications***.

Conventional Terminal Block

This model includes hardware that supports three current inputs, three voltage inputs, six optoisolated inputs, eight output contacts, two EIA-232 ports, and IRIG-B time code in a 3.5” (2U) rack mount package. It uses terminal blocks that support #6 ring terminals. This robust package meets or exceeds numerous industry standard type tests.

Plug-In Connector

This model includes hardware that supports all of the features of the conventional terminal block model. It differs in its use of plug-in connectors instead of terminal blocks. In addition, it provides

- High current interrupting output contacts.
- Quick connect/release hardware for rear-panel terminals.
- Time code input access on all rear communications ports.

This robust package meets or exceeds numerous industry standard type tests.

Phase Rotation

This manual is written for standard ABC phase rotation applications. If your SEL relay is ordered with the ACB phase rotation option, references made in the instruction manual to voltage and current phase angle should be noted accordingly. The firmware identification number (FID) may be used to verify whether your relay was ordered with ABC ("B") or ACB ("C") rotation.

All current and voltage inputs are connected to the SEL relay rear panel as shown in the instruction manual.

System Frequency

This manual is written for relays operating at a nominal system frequency of 60 Hz. For relays which specify a nominal frequency of 50 Hz, substitute 50 Hz for each reference to 60 Hz.

References made to a sampling time of 1/240 seconds should be replaced with a time of 1/200 seconds.

General Description

The SEL-2BFR Relay is a single- or three-pole breaker failure protection and monitoring package. The relay provides classical overcurrent-based breaker failure protection for a wide variety of breaker arrangements. Additional features include metering, event reporting, remote setting capabilities, breaker operating time monitors, energy interruption monitors, and breaker resistor thermal protection. Simple hardware design and efficient digital signal processing ensure reliability. Extensive self-testing and communication capabilities enhance availability.

The SEL-2BFR Relay has six fault current-driven breaker protection schemes, including one specially designed for ring-bus or breaker-and-a-half applications. Tailor the relay to your circuit breaker protection requirements by selecting the most appropriate scheme.

The relay detects failures to interrupt fault, load, or line-charging current. It also detects failures of breaker poles to complete a close sequence. When potential transformers are used, the relay can detect open breaker pole flashover failures.

Independent phase current detectors, protection logic, and timers make the relay easy to apply on both simple systems and more complicated breaker arrangements such as single-pole trip installations.

The SEL-2BFR Relay stores summaries of the 100 latest events in nonvolatile memory. These summaries include event type, mechanical and electrical operating times, breaker energy, and date and time of operation. Using this breaker history, you can monitor breaker wear and effectively schedule routine breaker maintenance.

A breaker can occasionally operate incompletely, leaving trip or close resistors in service. The energy dissipated in a breaker resistor due to current flow can exceed the resistor thermal rating within seconds, resulting in dangerous and expensive resistor failure.

When potential transformer inputs are used, the SEL-2BFR Relay uses six thermal models to monitor energy dissipated in breaker trip and close resistors. When a resistor temperature estimate reaches preset limits, the relay can alarm, generate an event report, or trip the lockout relay. Resistor thermal models have pending failure and failure temperature levels.

The thermal protection function does not require an initiating input; it monitors the breaker continuously. Thermal protection can be disabled when trip and close resistors are not used.

When you use a single motor-operated disconnect switch (MOD) with the protected breaker, the SEL-2BFR Relay can trip the MOD to isolate the failed breaker when phase current drops below a settable value. When an MOD is not installed, the MOD logic may be used to indicate a 'Safe to Disconnect' condition to personnel.

The relay also includes Programmable Mask Logic, which allows you to configure the 86BF TRIP and five auxiliary outputs to operate when any of 40 protective elements or logic outputs pick up. You can implement complete application-specific protective schemes with a minimum of wiring and panel space. Programmable Mask Logic also simplifies relay testing.

Communications functions provide remote and local examination of a wide range of data, including the voltages and currents presented to the instrument, relay settings, and a history of the last 100 events. You can enter and modify relay settings remotely; you can also control all outputs via the communications channel. A two-level password scheme protects settings and circuit breaker control. The SEL-2BFR Relay monitors password execution and closes the ALARM contact output to indicate possible unauthorized access. The relay requires no special communication software. Access the relay with a dumb terminal, printing terminal, or computer with serial port and terminal emulation software.

A wide range of user-selectable events, including any input or output assertion (except ALARM), triggers the event record function. Assertion of the 86BF TRIP output automatically generates an event report. You can also set the relay to trigger an event report for CLOSE or TRIP input assertions. This ensures a record of every normal circuit breaker operation, as well as every circuit breaker failure (***Section 4: Event Reporting*** includes more details on triggering event reports).

The event report contains all information needed to determine the cause of relay and breaker operations. These 15-cycle reports contain current, voltage, input, output, and relay element data presented on a quarter-cycle basis. Parameters such as event type, relay response time, circuit breaker operation time, currents, voltages, and breaker power dissipation appear directly in the event report or can be calculated from the data stored. All event reports are time-tagged by a self-contained clock/calendar.

The SEL-2BFR Relay is available in either a conventional terminal block or plug-in connector model. The conventional terminal block relay has #6-32 screw terminals for ring lugs. The plug-in connector model offers easy and fast connector installation and replacement through the use of plug-in connectors. Inputs and outputs use Euro-style plugs. CT, PT, and power connectors come with factory-crimped custom wiring harnesses. Shorting mechanisms within CT plugs automatically short CT secondaries upon removal of the plugs from the relay.

High current interrupting contacts are standard on the SEL-2BFR plug-in connector model. These contacts use an electromechanical relay with solid state circuitry to interrupt dc currents far greater than that of a typical contact output. This circuitry employs no silicon-controlled rectifiers (SCRs). The circuit is designed to make 30 Adc, carry 6 Adc, and interrupt 10 Adc. The circuit can interrupt 10 Adc four times in one second. The circuit then must cool for two minutes to prevent thermal damage.

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SECTION 2: SPECIFICATIONS

General Specifications

General

Tightening Torque: Terminal Block:
Minimum: 7-in-lb (0.8 Nm)
Maximum: 12-in-lb (1.4 Nm)

Connectorized®:
Minimum: 4.4-in-lb (0.5 Nm)
Maximum: 8.8-in-lb (1.0 Nm)

Terminal Connections: Terminals or stranded copper wire. Ring terminals are recommended. Minimum temperature rating of 105°C.

AC Current Inputs: 5 A nominal: 15 A continuous, 500 A for 1 s, linear to 155 A symmetrical.
1250 A for 1 cycle.
Burden: 0.27 VA at 5 A, 2.51 VA at 15 A.

1 A nominal: 3 A continuous, 100 A for 1 s, linear to 31 A symmetrical.
250 A for 1 cycle.
Burden: 0.06 VA at 1 A, 0.5 VA at 3 A.

AC Voltage Inputs: 150 V_{L-N}, three-phase, four-wire connection.
150 V continuous (connect any voltage from 0 to 150 Vac).
365 V for 10 s.
Burden: 0.07 VA @ 67 V; 0.42 VA @ 150 V.

Power Supply: Rated: 125/250 Vdc:
Range: 85–350 Vdc or 85–264 Vac
Burden: <15 W
Interruption: 30 ms @125 Vdc
Ripple: 100%

Rated: 24/48 Vdc:
Range: 20–60 Vdc
Burden: <15 W
Interruption: 30 ms @ 48 Vdc
Ripple: 5%

Note: Interruption and Ripple per IEC 255-11: 1979.

Output Contacts: Standard (Terminal Block Option):

Make: 30 A; Carry: 6 A continuous carry at 70°C; 1 s Rating: 50 A; MOV protected: 270 Vac, 360 Vdc, 40 J;
Pickup time: Less than 5 ms. Dropout time: Less than 5 ms, typical.

Breaking Capacity (10000 operations):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

Cyclic Capacity (2.5 cycles/second):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

High Current Interrupting (Connectorized Option):

Make: 30 A; Carry: 6 A continuous carry at 70°C; 1 s Rating: 50 A;
MOV protected: 330 Vdc, 40 J;
Pickup time: Less than 5 ms; Dropout time: Less than 8 ms, typical.

Breaking Capacity (10000 operations):

24 V	10 A	L/R = 40 ms
48 V	10 A	L/R = 40 ms
125 V	10 A	L/R = 40 ms
250 V	10 A	L/R = 20 ms

Cyclic Capacity (4 cycles in 1 second, followed by 2 minutes idle for thermal dissipation):

24 V	10 A	L/R = 40 ms
48 V	10 A	L/R = 40 ms
125 V	10 A	L/R = 40 ms
250 V	10 A	L/R = 20 ms

Note: Do not use high current interrupting output contacts to switch ac control signals. These outputs are polarity dependent.

Note: Make per IEEE C37.90: 1989; Breaking and Cyclic Capacity per IEC 255-23: 1994.

Optoisolated Inputs:

250 Vdc:	Pickup 150–300 Vdc.		
125 Vdc:	Pickup 100–150 Vdc;	Dropout 75 Vdc (Connectorized Option).
48 Vdc:	Pickup 30–60 Vdc;	(Terminal Block Option).
48 Vdc:	Pickup 38.4–60 Vdc;	Dropout 28.8 Vdc (Connectorized Option).
24 Vdc:	Pickup 15.0–30 Vdc.	

Note: Terminal Block Option: 24, 48, and 250 Vdc optoisolated inputs draw approximately 4 mA of current, and 125 Vdc inputs draw approximately 6 mA of current. Connectorized Option: 24 and 250 Vdc optoisolated inputs draw approximately 4 mA of current, 48 Vdc inputs draw approximately 5 mA of current, and 125 Vdc inputs draw approximately 6 mA of current. All current ratings are at nominal input voltage.

Routine Dielectric Strength: AC current inputs, AC voltage inputs: 2500 Vac for 10 s; power supply, optoisolated inputs, and output contacts: 3100 Vdc for 10 s.

Frequency and Rotation System Frequency: 50 or 60 Hz are ordering options;
Phase Rotation: ABC or ACB are ordering options.

Communications Ports: EIA-232: Baud rate: 300–9600 baud; includes front and rear connector for Port 2.

Time-Code Input: Relay accepts demodulated IRIG-B time-code input at AUX INPUT.

Operating Temp.: –40° to +70°C (–40° to +158°F).

Weight: 12 lbs (5.5 kg).

Dimensions: Refer to Figure 6.3 and Figure 6.5.

Type Tests:

*Cold:	IEC 68-2-1: 1990, EN 60068-2-1: 1993, Test Ad, 16 hours at –40ºC
*Dry Heat:	IEC 68-2-2: 1974, EN 60068-2-2: 1993, Test Bd, 16 hours at +85ºC
Damp Heat, Cyclic:	IEC 68-2-30: 1980, Test Db, 25° to 55ºC, 6 cycles, 95% humidity
Dielectric Strength:	IEC 255-5: 1977; IEEE C37.90: 1989, 2500 Vac on analog inputs, 3100 Vdc on contact inputs, contact outputs, and power supply
Impulse:	IEC 255-5: 1977, 0.5 J, 5000 V
Vibration:	IEC 255-21-1: 1988, Class 1
Shock and Bump:	IEC 255-21-2: 1988, Class 1
1 MHz Burst Disturbance:	IEC 255-22-1: 1988, 2.5 kV Peak, Common Mode, 1.0 kV Peak, Differential Mode
Electrostatic Discharge:	IEC 801-2: 1991, Level 4
Radiated Radio Frequency:	IEC 255-22-3: 1989, (Connectorized) IEEE C37.90.2: 199x (draft), (Terminal Block) 10 V/m

Fast Transient Disturbance:	IEC 801-4: 1988
Surge Withstand Capability:	IEEE C37.90.1: 1989, 3000 V oscillatory, 5000 V fast transient

Note: * = Connectorized option only.

Processing Specifications: 4 samples per power system cycle.

Fault Current Element (50FT)

Pickup Range	
5 A Model:	0.5–45.0 A
1 A Model:	0.1–9.0 A
Pickup Accuracy	
Steady State:	±0.025 A ±5%
Transient (Scheme 6):	±5%
Pickup Time:	Less than 0.84 cycle at 2 multiples of pickup
Dropout Time:	Less than 1.1 cycles

MOD Current Element (50MD)

Pickup Range	
5 A Model:	0.1–45.0 A
1 A Model:	0.02–9.00 A
Pickup Accuracy	
Steady State:	±0.025 A ±5%
Pickup Time:	Less than 1.1 cycles at 2 multiples of pickup
Dropout Time:	Less than 1.55 cycles

Load/Line-Charging Current Element (50LD)

Pickup Range	
5 A Model:	0.10–45.00 A
1 A Model:	0.02–9.00 A
Pickup Accuracy	
Steady State:	±0.025 A ±5%
Pickup Time:	Less than 1.1 cycles at 2 multiples of pickup
Dropout Time:	Less than 1.55 cycles

Flashover Voltage Element (59FO)

Pickup Range:	1.0–67.0 V
Pickup Accuracy	
Steady State:	±0.09 V ±5%
Pickup Time:	Less than 1.35 cycle
Dropout Time:	Less than 1.55 cycles

Negative-Sequence Overvoltage Element (47Q)

Pickup Range:	2.0–170.0 V
Pickup Accuracy:	±0.27 V ±15%
Pickup Time:	Less than 1.35 cycles
Dropout Time:	Less than 1.55 cycles

Flashover Voltage Element (59H)

Pickup:	Fixed at 67.0 V
Pickup Accuracy:	±3.5 V
Pickup Time:	Less than 1.35 cycles
Dropout Time:	Less than 1.55 cycles

Voltage Across Closed Breaker Element (Vwarn)

Pickup Range:	0.5–7.5 V
Pickup Accuracy:	±0.09 V ±5%
Pickup Time:	Less than 3 seconds

Current Unbalance Element (87UB)

87UB Phase Current Unbalance Element

87UB detects phase discordance when the protected breaker closes. For example, A-phase is unbalanced if phase current is above the 50LD setting in one or more phases and:

$$\frac{|IA| < \left(|IA| + |IB| + |IC|\right)}{87\text{ UB setting}}$$

Stabilization Time: Less than 1.35 cycle

Overpower Elements (37OP)

Pickup Range	
5 A Model:	0.1–3400.0 Watts
1 A Model:	0.02–680.00 Watts
Pickup Time:	Less than 2.10 cycles
Dropout Time:	Less than 3.00 cycles
Maximum Element Error:	±2.25 mW ±10.25% (measured input power) ±2.63% (measured voltage) ±9.45% (measured current)

Section 5: Applications discusses use of this error figure.

Breaker Resistor Thermal Elements (26CF, 26CP, 26TF, 26TP)

Pickup Range	
5 A Model:	0.01–1000.00 Joules
1 A Model:	0.002–200.000 Joules

Settable Timers

62TT	Failure to Trip Fault Current Trip Input Timer
62FC	Failure to Trip Fault Current Failure Timer
62LD	Failure to Trip Load Current Failure Timer
62LP	Failure to Trip Load Current Pending Failure Timer
62AF	Failure of Breaker 52A Contact to Indicate Operation Failure Timer
62AP	Failure of Breaker 52A Contact to Indicate Operation Pending Failure Timer
62FF	Flashover Failure Timer
62FP	Flashover Pending Failure Timer
62UC	Phase Discordance Close Input Pickup Timer
62OP	Trip and Close Resistor Heating Pickup Timer
RTSD	Retrip Seal-In Delay Timer (SEL-2BFR-2 ONLY) setting ranges: 0.25–63.75 cycles in quarter-cycle steps
RTTD	Retrip Time Delay Timer setting ranges: 0.25–63.75 cycles in quarter-cycle steps
62UF	Phase Discordance Failure Timer
62UP	Phase Discordance Pending Failure Timer
62M1	Maximum Bus Clearing Time
62M2	Maximum MOD Operate Time setting ranges: 0.25–16383.75 cycles in quarter-cycle steps

Fixed Timers

62F1	Flashover Voltage Time Delayed Dropout Timer	5 cycles
62F2	Load Current Pickup Timer (Flashover Logic)	5 cycles
62F3	Trip or Close Dropout Timer (Flashover Logic)	6 cycles
62M3	86BF Reset Signal Duration Timer	60 cycles
62M4	86BF Reset Time Delay, MOD Logic Enabled	300 cycles

Note: All timers are crystal controlled. Any significant ambiguities in timing are due to pickup/dropout times of measuring elements, inputs, and outputs. All timers, except the 620P timer, have an accuracy of ±0.25 cycle. The 62OP timer has an accuracy of ±0.5 cycle.

LOGIC INPUTS

Six input circuits are provided. To assert an input, apply nominal control voltage to the appropriate terminal pair. Table 2.1 lists the inputs and their functions.

Table 2.1: Logic Input Functions

Input	Function
TRIP A	A-Phase Trip Signal Input
TRIP B	B-Phase Trip Signal Input
TRIP C	C-Phase Trip Signal Input
52A STATUS	Breaker Auxiliary Contact Input
MOD STATUS	MOD Auxiliary Contact Input
CLOSE	Breaker CLOSE Signal Input

For three-pole trip breakers, connect the trip inputs such that any time the breaker trip coil is energized, all three trip inputs are asserted. For single-pole trip breakers, connect the trip inputs such that only the corresponding trip input is asserted when a single-pole trip coil is energized.

The CLOSE input is three pole. In single-pole trip installations, connect the close input so that it is asserted each time any single-pole close coil is energized.

Connect the 52A STATUS and MOD STATUS inputs such that when the corresponding equipment is in a closed position, the input is asserted.

Relay Outputs

The SEL-2BFR Relay has seven programmable output relays. All outputs, except the ALARM output, are programmed with the **LOGIC** command. All can be tested with the **OUT n** command.

All conventional terminal block model relay contacts are rated for circuit breaker tripping duty. Any of the programmable outputs or the ALARM contacts may be configured as "a" or "b" when you order the relay. The 86BF TRIP output contacts are always "a."

All plug-in connector model relay control outputs are dry relay contacts rated for 30 A make, 6 A carry, and 10 A interrupt with an L/R = 40 ms at 125 Vdc. The contacts can interrupt 10 A, L/R = 40 ms, 125 Vdc four times in one second after which the contact must be allowed to cool for two minutes. Each contact is protected by a metal oxide varistor. Note that the contacts are polarity sensitive.

86BF TRIP Output

Use this output to assert the bus lockout relay when a breaker failure occurs.

Programmable Outputs (A1, A2, A3, A4, A5)

Use these five outputs to trip motor-operated disconnect switches, retrip the protected breaker following a trip input assertion, or indicate a number of conditions detected by the relay.

ALARM Output

The ALARM output closes for the following conditions:

- Three unsuccessful Level 1 access attempts: one-second pulse
- Any Level 2 access attempt: one-second pulse
- Self-test failures: permanent contact closure or one-second pulse depending on which self-test fails (see ***Self-Testing*** at the end of this section).

The standard relay has the ALARM contact configured as "b." In this case, it is held open during normal relay operation and closes if control power is lost or any other alarm condition occurs.

RELAY WORD

The Relay Word consists of five eight-bit rows containing relay elements, timer outputs, and logic outputs. Each bit in the Relay Word is either a logical 1 or logical 0:

- 1 indicates that the element is picked up or logic condition is true
- 0 indicates that the element is dropped out or logic condition is false

The logic description defines the logic conditions in the Relay Word.

The relay updates the Relay Word each quarter-cycle.

Table 2.2: SEL-2BFR Relay Word

Row	Relay Word Bits							
1	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF
2	FOBF	FOPF	59FO	59H	ALRM	TC	TB	TA
3	PDBF	PDPF	87UA	87UB	87UC	86RS	MDT	CTF
4	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB
5	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q

Table 2.3 explains each bit in the Relay Word.

Table 2.3: Relay Word Bit Definitions

Row	Bit	Explanation
1	FBF	Fault Current Breaker Failure
1	LBF	Load Current Breaker Failure
1	LPF	Load Current Pending Failure
1	50FT	Fault Current Overcurrent Element
1	50LD	Load Current Overcurrent Element
1	50MD	MOD Overcurrent Element
1	52BV	Current-Verified 52BV
1	TTF	Trip Resistor Thermal Failure
2	FOBF	Flashover Breaker Failure
2	FOPF	Flashover Pending Failure
2	59FO	Overvoltage Element
2	59H	Flashover Overvoltage Element
2	ALRM	Breaker Operation Alarms
2	TC	C-Phase Retrip Output
2	TB	B-Phase Retrip Output
2	TA	A-Phase Retrip Output
3	PDBF	Phase Discordance Breaker Failure
3	PDPF	Phase Discordance Pending Failure
3	87UA	A-Phase Discordance
3	87UB	B-Phase Discordance
3	87UC	C-Phase Discordance
3	86RS	86BF Reset
3	MDT	MOD Trip
3	CTF	Close Resistor Thermal Failure
4	CRFA	A-Phase Close Resistor Failure
4	CRPA	A-Phase Close Resistor Pending Failure
4	TRFA	A-Phase Trip Resistor Failure
4	TRPA	A-Phase Trip Resistor Pending Failure
4	CRFB	B-Phase Close Resistor Failure
4	CRPB	B-Phase Close Resistor Pending Failure
4	TRFB	B-Phase Trip Resistor Failure
4	TRPB	B-Phase Trip Resistor Pending Failure

Row	Bit	Explanation
5	CRFC	C-Phase Close Resistor Failure
5	CRPC	C-Phase Close Resistor Pending Failure
5	TRFC	C-Phase Trip Resistor Failure
5	TRPC	C-Phase Trip Resistor Pending Failure
5	DOPA	A-Phase Delayed Overpower
5	DOPB	B-Phase Delayed Overpower
5	DOPC	C-Phase Delayed Overpower
5	47Q	Negative-Sequence Overvoltage Element

Programmable Output Logic

The relay uses programmable logic masks to control the 86BF TRIP and programmable output relays. Logic masks are saved in nonvolatile memory with the other settings. They are set with the **LOGIC** command and retained through losses of control power.

To program each logic mask, select elements of the Relay Word. If any element in the Relay Word asserts and the same element is selected in a logic mask, the output contact associated with the logic mask operates.

The output equations follow (the "*" indicates a logical "and," while the "+" indicates a logical "or").

Let R = Relay Word

Close 86BF Trip = R * M86T

Open 86BF Trip conditions are defined in the logic description.

A1 = R * MA1
A2 = R * MA2
A3 = R * MA3
A4 = R * MA4
A5 = R * MA5

ALARM = (Self-Test Failure or Warning)
+ (Level 1 Password Violation)
+ (Setting or Logic Changes)
+ (Level 2 Access Attempts)

RELAY TARGETS

The relay normally displays the targets identified on the front panel. Under normal operating conditions, the Enable (EN) target lamp is lit. The AL, PF, A, B, and C target LEDs latch.

Front-panel targets illuminate for the conditions shown in Table 2.4.

Table 2.4: Front-Panel Target Illumination Conditions

Target LED	Conditions for Illumination
EN	Normal operation
AL	ALARM condition
PF	PEND FAIL condition
A	Phase A breaker failure
B	Phase B breaker failure
C	Phase C breaker failure
52A	52A STATUS input assertion
MOD	MOD STATUS input assertion

The Enable (EN) LED indicates that the relay is energized and operating.

The Alarm (AL) LED asserts for Level 1 Access failures, Level 2 Access attempts, and self-test warnings or failures. The AL LED does not assert when the Relay Word ALRM bit asserts. The AL LED latches, so the user must press the TARGET RESET button or execute the **TARGET R <ENTER>** command to clear the ALARM LED when it asserts.

The PF LED illuminates if any pending failure bits routed to an output contact assert.

If the relay asserts the 86BF TRIP output, the A, B, or C targets latch to indicate the failed breaker pole.

The 52A and MOD LEDs illuminate if the associated rear-panel input is asserted.

The target LEDs that illuminated during the last trip output remain lit until one of the following occurs:

- Operator presses front-panel TARGET RESET button
- Operator executes **TARGET R** command

When you press the TARGET RESET button, all eight indicators illuminate for a one-second lamp test. The relay targets clear and the Enable target lamp (EN) illuminates to indicate that the relay is operational.

The **TARGET R** command also resets the front-panel target LEDs. Use the **TARGET** command and display to examine the state of the relay inputs, outputs, and Relay Word elements. For more details, see ***Command Descriptions*** in ***Section 3: Communications***.

The relay does not clear the front-panel targets when additional trip outputs occur. The new tripping targets are displayed with the old in a cumulative fashion until an operator clears them as described above.

The front-panel targets indicate breaker failures based on the outputs from each of the basic breaker protection schemes, regardless of whether you have enabled the scheme for protection. This can become important when testing the relay, because targets may assert for conditions not under test if they indicate that a failure has occurred.

SIGNAL PROCESSING

The relay filters the current and voltage channels and samples the signals four times per power system cycle. The relay stores the analog low-pass filtered samples for event reporting. The microprocessor digitally filters each signal using the CAL or FOD digital filters explained below. The relay stores digital filter outputs for magnitude calculations.

The relay uses a simple, effective CAL digital filter with the properties of a double differentiator smoother. Let the latest four samples of one analog signal be X1, X2, X3, and X4. Then the filter is defined:

$$P = X1 - X2 - X3 + X4.$$

This filter eliminates dc offsets. When all samples are set to the same value, the filter output is zero. The filter also eliminates ramps, which you may verify by setting the samples equal to 1, 2, 3, 4. Again, the output is zero.

Every quarter-cycle, the relay computes a new value of P for each input. The current value of P combines with the previous value (renamed Q) to form a Cartesian coordinate pair. This pair represents the input signal as a phasor (P, Q). The relay processes these phasor representations of the input signals.

The digital and analog filter net frequency response is centered on system frequency and completely rejects dc and double-frequency harmonics. The computer determines the magnitude of each voltage and current from the digital filter output.

For a faster pickup and dropout response time, the 50FT element uses a First Order Difference (FOD) filter ($P = X1 - X2$) rather than the CAL filter.

LOGIC DESCRIPTION

The SEL-2BFR Relay provides protection for several circuit breaker (CB) failure modes:

- Failure to clear a fault (six available schemes)
- Failure to trip under load
- Failure of the breaker 52A contact to indicate operation
- Failure to complete trip sequence due to trip resistor(s) remaining inserted
- Failure to complete close sequence due to close resistor(s) remaining inserted
- Failure to close
- Failure while open: breaker pole flashover detected

The relay provides reset logic for applications with and without motor-operated disconnects. The relay also provides logic for a verified 52B output. The following sections describe the logic for each of these protection schemes. ***Section 5: Applications*** discusses scheme and relay setting selection.

Protection While Tripping Fault Current

The SEL-2BFR Relay provides six different protection schemes to safeguard the circuit breaker under fault current conditions. While the schemes share elements and timers, each is independent. You may enable only one protection scheme at a time. The SEL-2BFR Relay applies the single chosen scheme to all three breaker poles. To enable the selected scheme for breaker lockout tripping via the 86BF TRIP output, set the FBF bit in the M86T logic mask equal to one.

Figure 2.1 through Figure 2.6 show logic diagrams for A-phase breaker protection only. In each case, B-phase and C-phase logic is identical in form, using the respective phase trip inputs and 50FT elements.

Scheme 1

The logic shown in Figure 2.1 protects the breaker for failure during a fault. This scheme is applicable to single breaker, ring-bus, and breaker-and-a-half bus configurations.

To understand the operation of the Scheme 1 logic, review two possible scenarios:

- 50FT element asserts before the trip input is asserted.
- Trip input is asserted before the 50FT element asserts.

If the 50FT element picks up before trip input assertion, the 50FT signal disables the 62TT timer. The 62FC timer starts when the trip signal input asserts. The 62FC timer continues to time until 50FT drops out or the timer expires. When the 62FC timer expires, the FBF bit in the Relay Word asserts.

In ring-bus and breaker-and-a-half installations, it is possible for the trip input to assert before the 50FT overcurrent element picks up. If the trip input asserts before the 50FT element picks up, the 62TT timer output asserts and the 62FC timer starts. The 62TT timer output remains asserted for 62TTdo time or until the 50FT element picks up. When the 50FT element asserts, the 62TT timer resets, but the output of OR 2 remains high. The 62FC timer continues to time until the 50FT overcurrent element drops out. If the 50FT element picks up and remains asserted until 62FC expires, the FBF bit in the Relay Word asserts.

In both cases, logic latches in the trip signal when the 62FC pickup timer starts. From that time, trip signal dropout does not affect the breaker protection scheme.

The 62TTdo setting must be at least two cycles lower than the 62FC timer setting. The relay checks this setting on entry. This restriction prevents the FBF output from asserting if the 50FT element does not assert. There are several instances in which trip input assertion occurs without 50FT pickup. This occurs when the:

- Relay receives an inadvertent trip signal;
- Operator manually trips load current;
- Protected breaker is open when trip input is asserted.

The FBF bit in the Relay Word asserts after the 62FC timer expires.

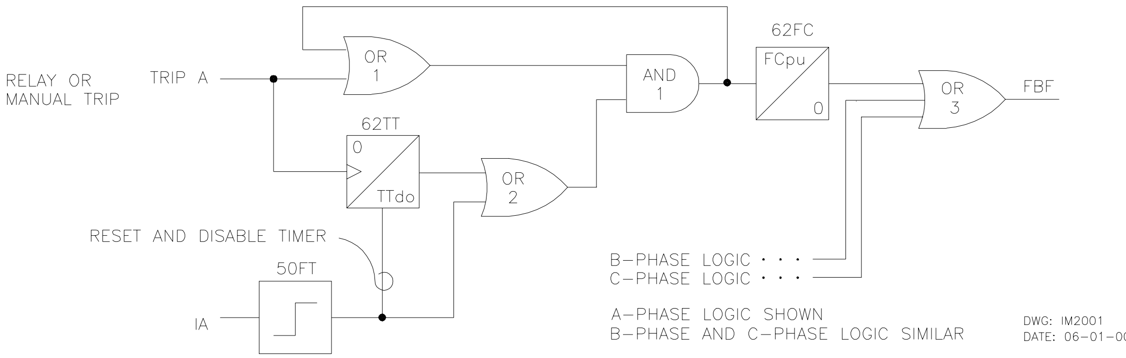

Figure 2.1: A-Phase Failure to Trip for Fault Logic, Scheme 1

Scheme 2

Figure 2.2 shows the logic diagram for Scheme 2, A-phase breaker protection.

In a single breaker arrangement, fault current causes the 50FT element to assert immediately following fault inception and just prior to trip signal arrival. If 50FT is asserted when the SEL-2BFR Relay receives the trip signal, the AND 1 output goes high. The 62FC pickup timer starts and the trip input signal is latched in. At this point, trip signal dropout does not affect the breaker failure scheme. If the 50FT element remains asserted until the 62FC timer expires, the Relay Word FBF bit asserts. If the breaker operates successfully, the 50FT element drops out before the 62FC timer expires and FBF does not assert.

Although it is very simple and effective in single breaker arrangements, Scheme 2 is not recommended when the protected breaker is part of a ring-bus or breaker-and-a-half installation. Consider using Scheme 1, Scheme 4, or Scheme 5 in such breaker arrangements.

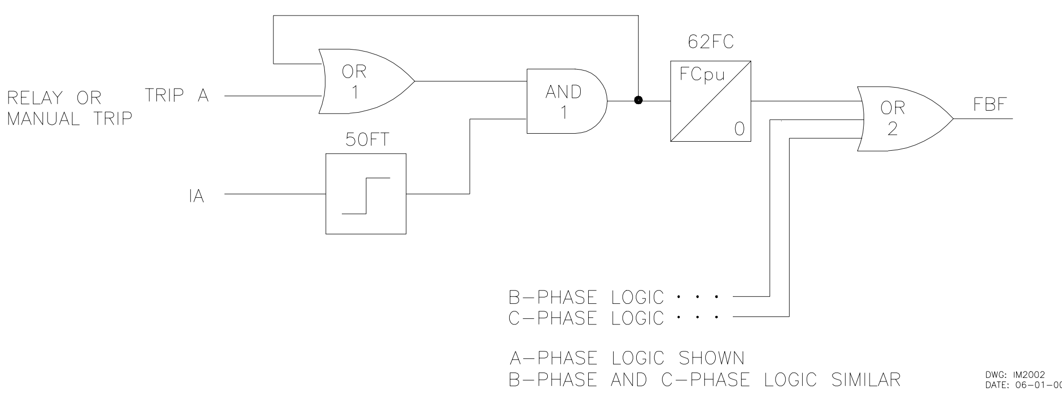

Figure 2.2: A-Phase Failure to Trip for Fault Logic, Scheme 2

Scheme 3

Figure 2.3 shows the logic diagram for Scheme 3, A-phase breaker protection.

Like Scheme 2, Scheme 3 is intended for use in a single breaker arrangement. When a fault occurs, 50FT asserts and the line protective relay asserts the SEL-2BFR Relay trip input. The

AND 1 output goes high and the 62FC timer starts. If the trip input and 50FT element remain asserted until 62FC expires, Relay Word bit FBF asserts.

In Scheme 3, the trip input must remain asserted while current flows in the protected breaker. Scheme 3 resets when either the trip input deasserts or the 50FT element drops out.

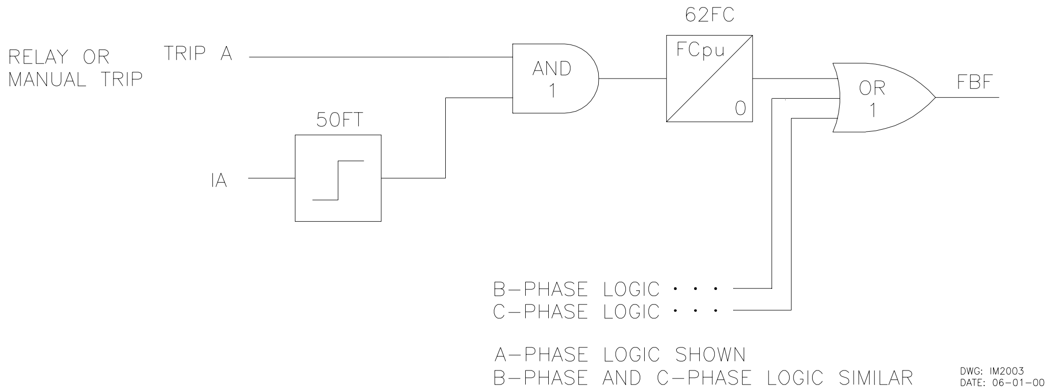

Figure 2.3: A-Phase Failure to Trip for Fault Logic, Scheme 3

Scheme 4

Figure 2.4 illustrates Scheme 4 A-phase breaker protection. Use Scheme 4 breaker protection in single breaker, ring-bus, or breaker-and-a-half installations.

When the SEL-2BFR Relay trip input is asserted, the 62TT pickup timer starts. The trip input is latched and may be deasserted after a single quarter-cycle assertion. 62TT pickup time following trip input assertion, the 62TT timer output asserts. The timer output remains asserted for 62TT dropout time. Relay Word bit FBF asserts if 50FT asserts while the 62TT timer output is asserted.

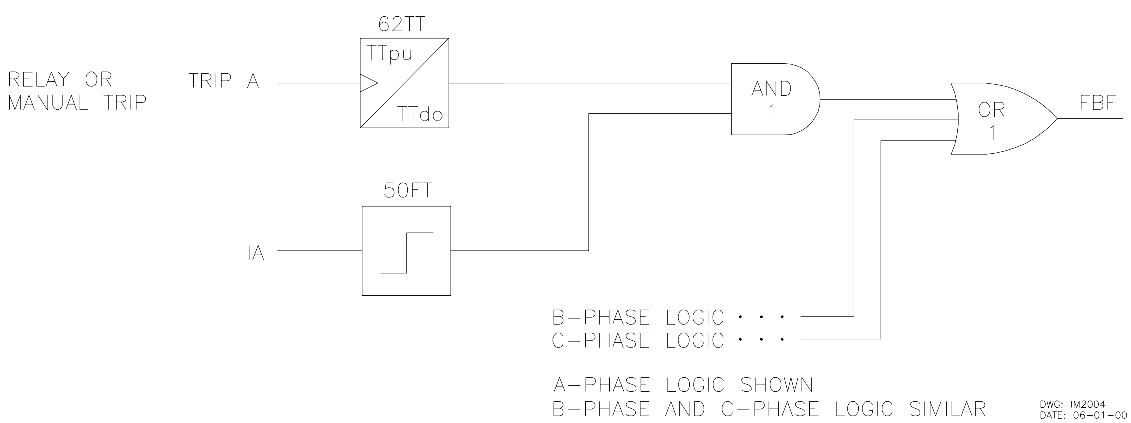

Figure 2.4: A-Phase Failure to Trip for Fault Logic, Scheme 4

Scheme 5

Figure 2.5 shows the A-phase logic for Scheme 5 breaker protection. Scheme 5 is intended for use in single breaker, breaker-and-a-half, and ring-bus arrangements.

When the trip input is asserted, the 62FC pickup timer starts. If 50FT is asserted when the 62FC timer expires, the Relay Word FBF bit asserts. If the trip input is deasserted or the 50FT element drops out before 62FC expires, the logic resets and FBF does not assert.

This scheme is similar to Scheme 3 because the trip input must remain asserted while current still flows in the protected breaker.

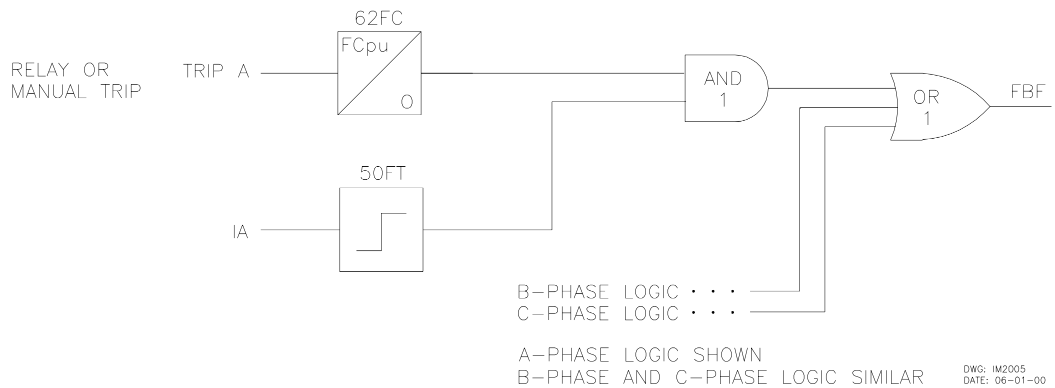

Figure 2.5: A-Phase Failure to Trip for Fault Logic, Scheme 5

Scheme 6

Figure 2.6 illustrates Scheme 6 A-phase and three-phase breaker protection. Use Scheme 6 breaker protection in single breaker, ring-bus, or breaker-and-a-half installations.

When the SEL-2BFR Relay trip input is asserted, the 62TT pickup timer starts. The trip input is latched and may be deasserted after a single quarter-cycle assertion. Following trip input assertion and 62TT pickup time, the 62TT timer output asserts. The timer output remains asserted for one cycle. Relay Word bit FBF asserts if 50FT picks up and asserts during the one-cycle window.

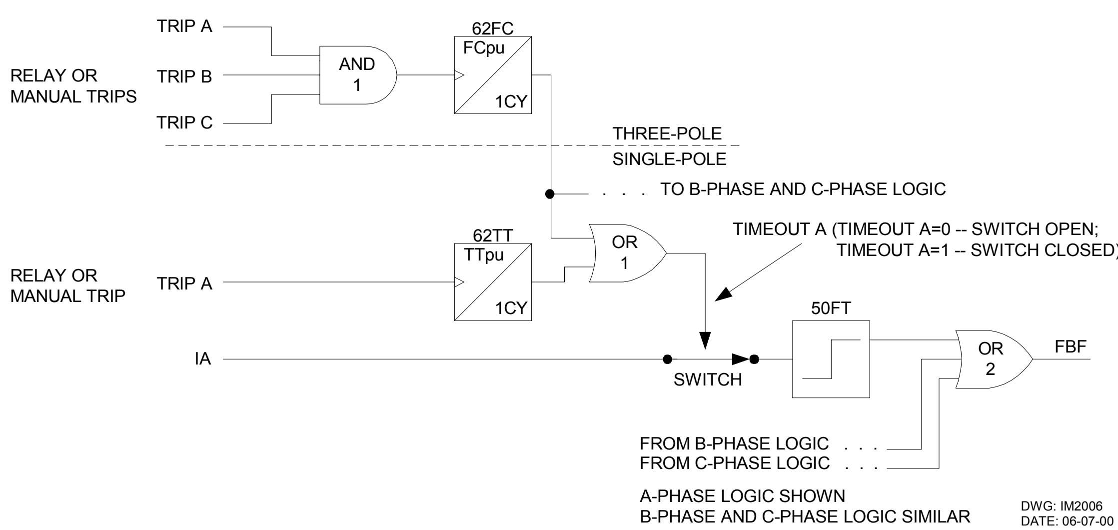

Figure 2.6: A-Phase and Three-Phase Failure to Trip for Fault Logic, Scheme 6

If all three trip inputs assert, the 62FC pickup timer starts. The three-phase trip input is latched and may be deasserted after a single quarter-cycle assertion. Following trip input assertion and 62FC pickup time, the 62FC timer output asserts. The timer output remains asserted for one cycle. Relay word bit FBF asserts if 50FT picks up and asserts during the one-cycle window.

The 62TT pickup timer also times for three-phase faults. Thus, the 62FC pickup timer provides an operational advantage only if it is set such that:

62FC pickup time delay setting < 62TT pickup time delay setting

Otherwise, the 62TT pickup timer will time out first for a three-phase fault.

The 50FT element is disabled while the 62TT or 62FC pickup timers are timing. Thus, the 50FT reset time does not have to be taken into account as part of the safety margin incorporated into the 62TT and 62FC pickup time-delay settings. See ***Section 5: Applications*** for more details.

Note: In a double-breaker arrangement (i.e., ring-bus or breaker-and-a-half) there are two breaker sources to the line, Figure 2.7. In this example, fault current distributes unequally between Breakers 1 and 2. Fault current through Breaker 1 is below breaker failure overcurrent element pickup levels. The majority of the fault current flows through Breaker 2. If Breaker 2 clears before Breaker 1 then the fault current increases dramatically through Breaker 1.

If Breakers 1 and 2 both fail to interrupt fault current and Breaker 1 has Scheme 6 active, breaker failure protection problems can result. The breaker failure protection scheme at Breaker 2 tries to trip the immediate breakers surrounding it, including Breaker 1. Breaker 1 is also failed, so the breaker failure trip from Breaker 2 to Breaker 1 is ineffectual.

Breaker failure timer 62TT (or 62FC) times out in Scheme 6 for Breaker 1 and the one-cycle window becomes active to let the 50FT overcurrent element pickup if sufficient fault current is present. After the one-cycle window, the 50FT element is turned off again. Because of the unequal fault current distribution between the Breakers 1 and 2, and Breaker 2 is failed, no fault current above the 50FT overcurrent element pickup level is detected through Breaker 1. The one-cycle window passes and no breaker failure tripping is initiated for Breaker 1.

The immediate breakers to the right of Breaker 2 eventually clear due to operation of the Breaker 2 breaker failure protection scheme and then fault current levels increase dramatically through Breaker 1. The one-cycle window for Breaker 1 has already passed so Scheme 6 does not initiate breaker failure tripping for Breaker 1 in this scenario.

The failure to trip load or line-charging current scheme (see Figure 2.8 and accompanying discussion) should be enabled to provide breaker failure protection for this scenario if it is a concern for Scheme 6 applied to such breaker arrangements.

Figure 2.1 and accompanying discussion (Scheme 1) address operating concerns similar to this scenario. Scheme 1 may be better suited to operate in such a scenario.

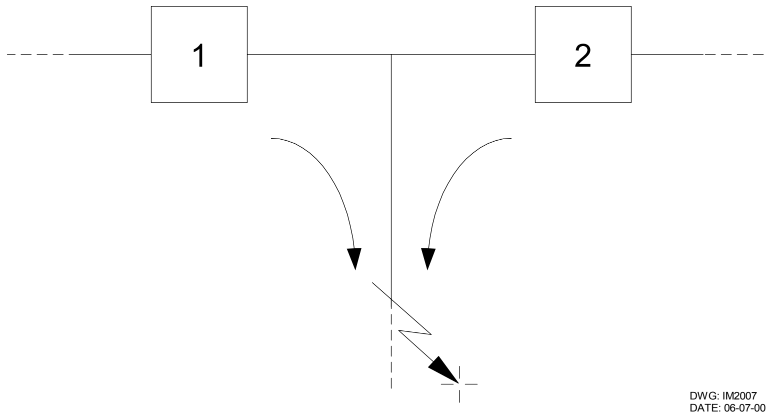

Figure 2.7: Double-Breaker Arrangement Provides Two Fault Current Sources

Protection While Tripping Load or Line-Charging Current

Figure 2.8 illustrates the logic that protects against breaker failure while tripping load current. This logic contains two sections. The first section detects breaker operation by dropout of sensitive phase overcurrent elements. The second section detects breaker operation by dropout of the 52A input. Both sections of logic operate the Relay Word LPF bit for pending failure operations and the Relay Word LBF bit for failure operations.

To use the overcurrent section of the logic, set the 50LD overcurrent element to pickup for load or line-charging current. With this sensitive setting, the 50LD element is picked up whenever the protected breaker is closed. When the trip input is asserted for two consecutive quarter-cycles, the 62LP and 62LD timers start. If the 50LD overcurrent element does not drop out before 62LP expires, the LPF (Load Current Pending Failure) bit asserts in the Relay Word. If the current remains above the 50LD threshold for the duration of 62LD, the LBF bit in the Relay Word asserts. When the phase current drops below the 50LD threshold, both timers reset.

Because this logic is very sensitive, the trip input must be asserted for two consecutive quarter-cycles before this logic acknowledges the input. This feature provides security against incidental trip input assertions.

In some applications, current through the closed breaker may be below the minimum setting of the 50LD element. In these instances, enable the relay to provide breaker failure protection based upon the 52A input state. When you set the E62A setting equal to Y or 1, the relay starts the 62AF and 62AP timers each time any TRIP input is asserted for two consecutive quarter-cycles while the protected breaker is closed (52A input asserted). The timers run until one of the following occurs:

- The 52A input deasserts, indicating that the breaker opened, or
- Some breaker failure detection mode operates the relay 86BF TRIP outputs, or
- The 62AF timer expires.

If the 52A input deasserts before either timer expires, both timers stop then are reset the next time the breaker closes. If the breaker fails in some manner detected by other logic in the relay and the 86BF TRIP output asserts, the 62A timers are disabled. When the 62AF timer expires, the Relay

Word LBF bit asserts. When the 62AP timer expires, the Relay Word bit LPF asserts to indicate the pending failure.

Set E62A equal to 1 or 2 to inhibit, or set E62A equal to Y or N to enable seal-in for manual or relay trip inputs to the 62LP and 62LD timer logic.

E62A Setting =	Enable Breaker Aux. Failure Logic	Enable Seal-In
Y	Yes	Yes
1	Yes	No
N	No	Yes
2	No	No

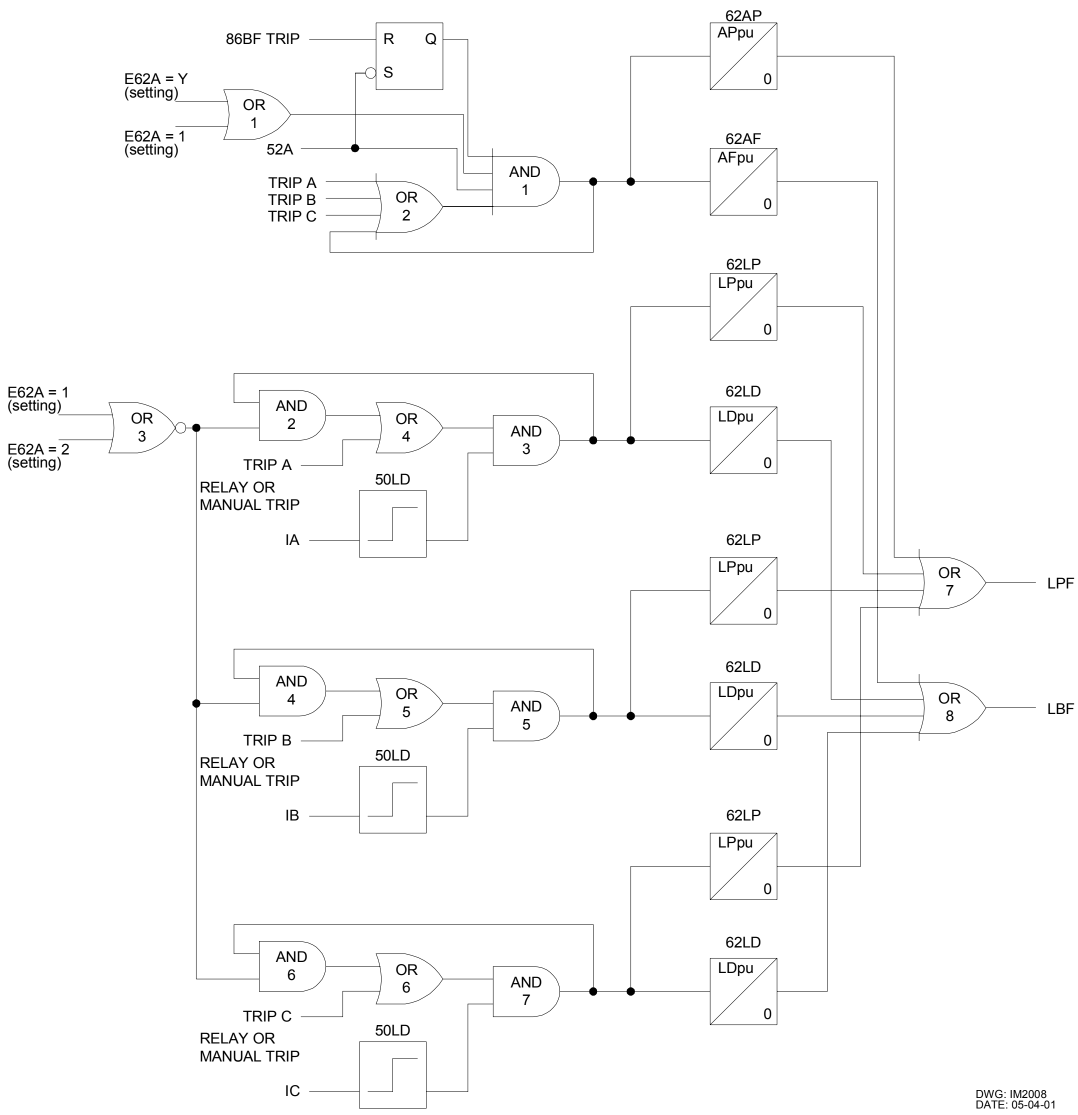

Figure 2.8: Failure to Trip Load or Line-Charging Current Logic

Thermal Protection of Close and Trip Resistors

The logic shown in Figure 2.9 is designed to protect the trip and close resistors in the A-phase of the circuit breaker. B- and C-phase logic is similar. The relay calculates the energy dissipated in each of the six resistors using independent thermal models.

The relay determines which model to heat based on the trip and close inputs. When a trip input is asserted, the relay closes switch T and opens switch C. When the close input is asserted, the relay closes switch C and opens switch T.

The 47Q negative-sequence overvoltage element supervises heating of the close resistor thermal model. If the breaker is closed and the 47Q element picks up, the relay inhibits heating of the close resistor thermal model. Pickup of the 47Q element indicates a blown potential fuse.

The thermal models and 37OP overpower element use current through the breaker and voltage across it. When power dissipated in the breaker exceeds the 37OP setting value, the 62OP pickup timer starts. If 37OP remains asserted for 62OP time, the H1 and H2 switches close. The close or trip resistor thermal model (CRTM or TRTM) heats, depending on the state of the switches T and C. If the energy accumulated by the thermal model reaches the 26CP (or 26TP) level before the 37OP element drops out, the CRP_ (or TRP_) (close or trip resistor pending failure) bit asserts in the Relay Word. If 37OP remains asserted until the resistor energy reaches the 26CF (or 26TF) value, the CRF_ or TRF_ (close or trip resistor failure) bit asserts in the Relay Word.

The Relay Word bits CTF (Close resistor Thermal Failure) and TTF (Trip resistor Thermal Failure) assert when any Close or Trip resistor thermal model has reached the failure energy level and at least 0.1 amp secondary of current is flowing in the hot resistor phase. If you set the CTF and TTF bits in the M86T logic mask, the relay asserts the 86BF TRIP outputs when a resistor thermal failure occurs.

The relay models cooling of the breaker resistors using a settable time constant. The thermal failure and pending failure elements do not drop out until the resistor thermal models have cooled below the element thresholds. The cooling function helps prevent hot resistors from being put back in service.

Thermal model cooling is performed at discrete time intervals. Tests reflect this interval as a uniformly distributed measurement error with bounds of ±T minutes where RTC equals the resistor cooling time constant and:

$$T = RTC \text{ (minutes)} / 383$$

No initiating input is required with this protection scheme. If the protected breaker is not equipped with trip or close resistors, do not enable this function for 86BF tripping. Three-phase potential inputs from both sides of the protected breaker are required when you use the thermal protection logic, see ***Section 5: Applications***.

Use the **HEAT** command to track or reset thermal model resistor energy.

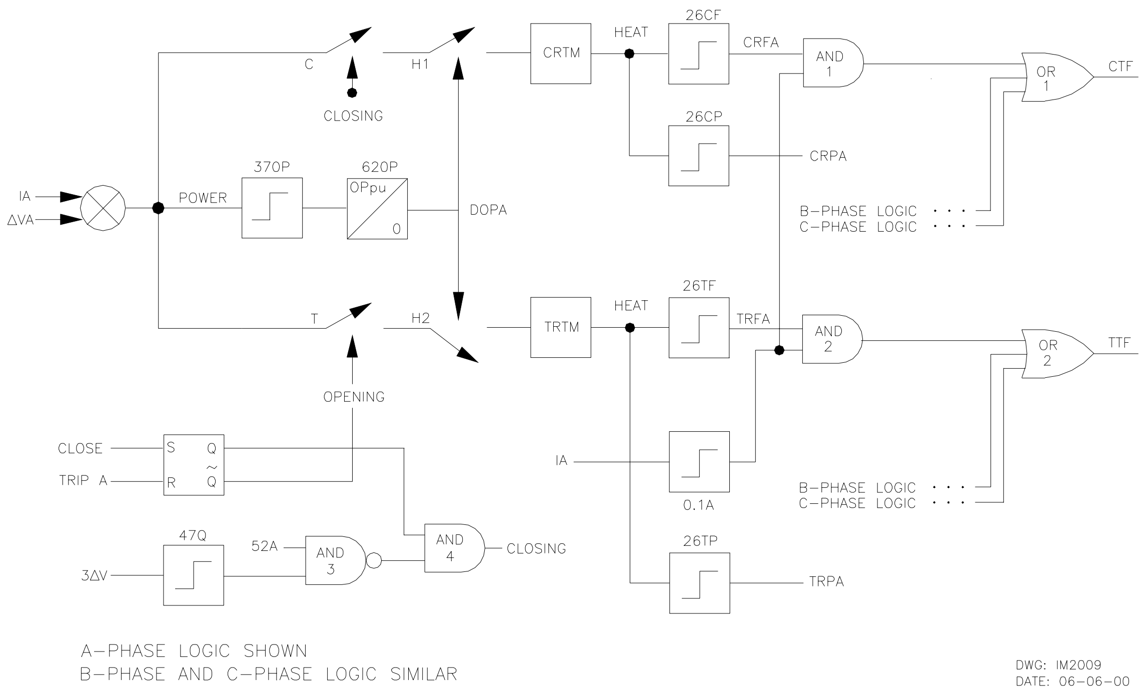

Figure 2.9: Trip and Close Resistor Thermal Protection Logic

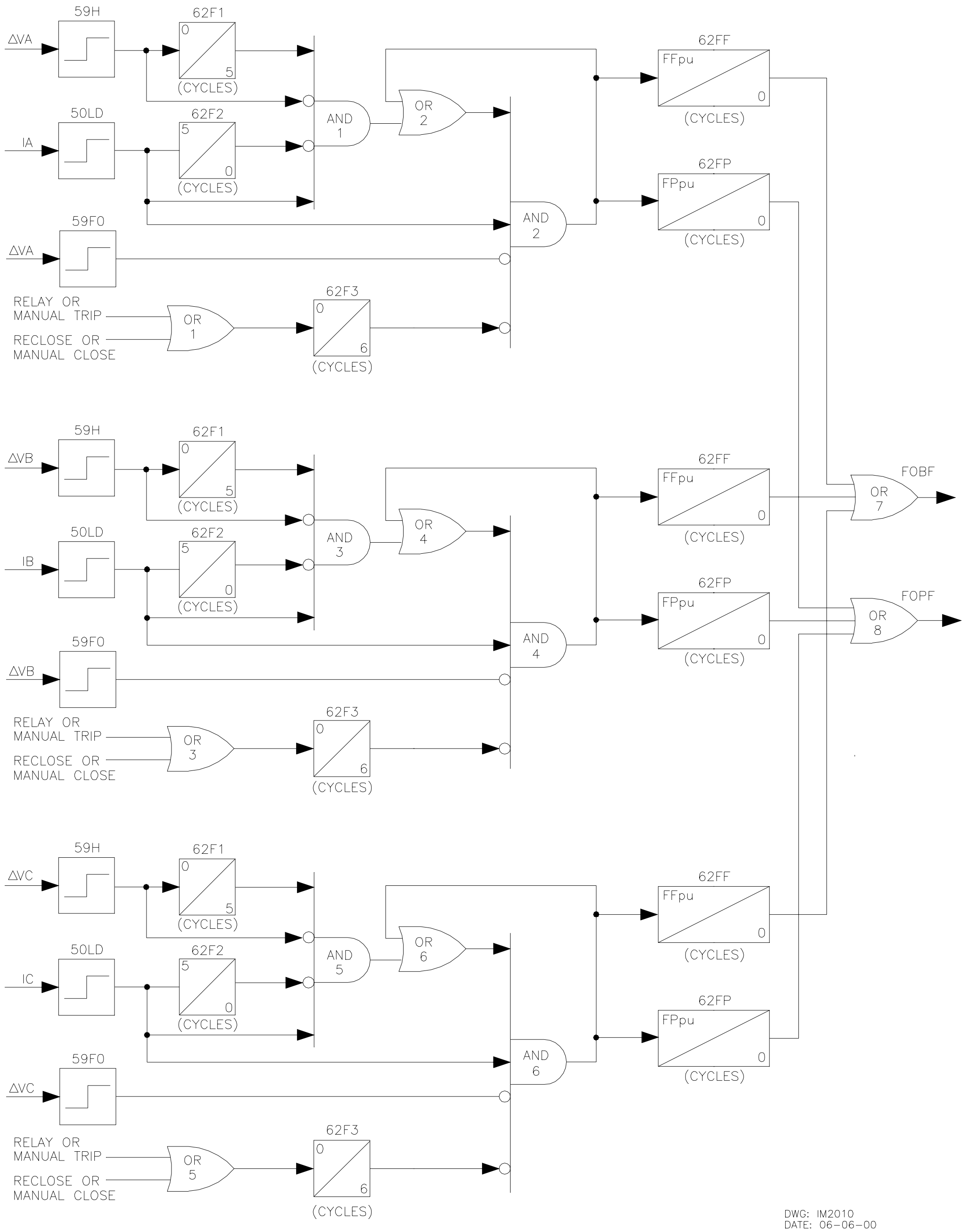

Figure 2.10: Protection for Current Through an Open Breaker Logic

Protection for Current Through an Open Breaker (Flashover)

When an open breaker pole flashes over, the following conditions can be used to detect the failure:

- One per-unit system voltage can be measured across the breaker pole before the flashover occurs.
- Once the flashover starts, voltage drops and current flows.

Because these two criteria may also describe breaker close operations, the flashover protection scheme is disabled for six cycles after assertion of the trip or close input.

The logic shown in Figure 2.10 detects breaker pole flashover failure.

The output of AND 2 asserts if voltage across the breaker pole has dropped below the 59FO element setting, current flowing in the breaker is above the 50LD setting, no trip or close input has asserted for six cycles, and the output of AND 1 is true.

For the output of AND 1 to be true, the following conditions must be met:

- 59H is not asserted, but was no more than five cycles ago (62F1 dropout timer).
- 50LD is asserted, but was not in the last five cycles (62F2 pickup timer).

Voltage of 67 volts secondary must be measured across the breaker for the 59H element to pick up.

If the AND 2 output asserts, the 62FF and 62FP timers start and the AND 1 condition is latched in via OR 2.

The timers will assert their outputs: if current remains above the 50LD threshold, and the trip and close inputs remain deasserted, and breaker voltage stays below the 59FO pickup threshold until the 62FP and 62FF timers expire. This causes the FOPF (Flashover Pending Failure) bit, then the FOBF (Flashover Breaker Failure) bit, to assert in the Relay Word.

Protection for Failure to Close

Figure 2.11 shows logic which detects a failure of one or two breaker poles to close. When the SEL-2BFR Relay receives a close signal, the 62UC timer begins timing. After the 62UC pickup time (UCpu) expires, if any phase has current greater than the 50LD setting and the sum of the currents divided by 87UB is greater than the phase current, the 62UF and 62UP timers start. If the unbalance condition persists for the 62UP time period, the PDPF (Phase Discordance Pending Failure) bit asserts in the Relay Word. If the condition continues until 62UF expires, the PDBF (Phase Discordance Breaker Failure) bit asserts in the Relay Word. The value of 87UB is setting selectable: 8, 16, 32, or 64.

This logic has an advantage over typical pole disagreement schemes based on contact operation. Because the logic operates based on current flowing in the breaker poles, protection is not dependent upon the operation of auxiliary contacts. Thus, this logic is not subject to misoperation due to mechanical failures in the breaker or contacts.

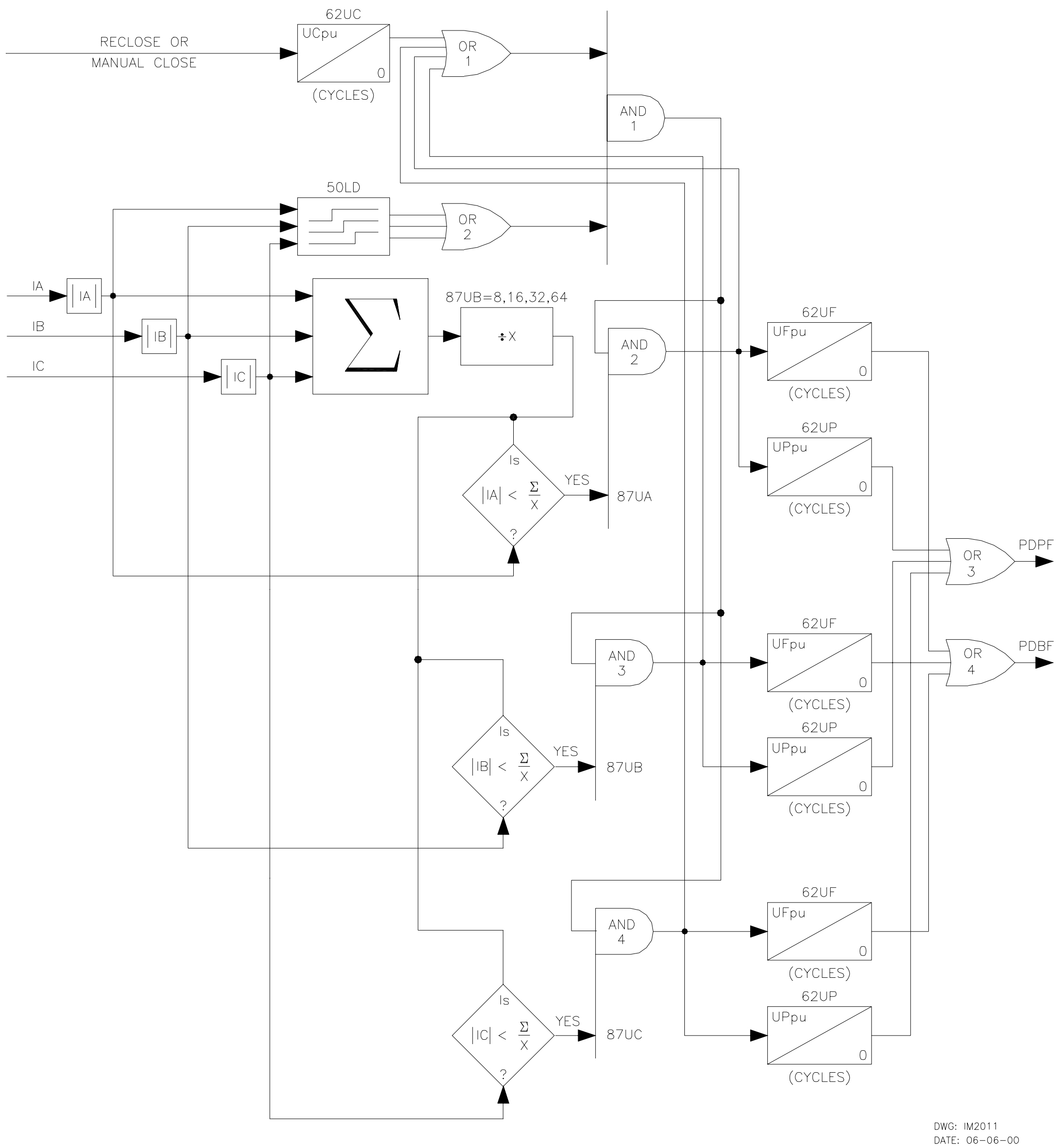

Figure 2.11: Phase Discordance While Closing Logic

Time-Delayed Breaker Retrip (SEL-2BFR Relay)

Figure 2.12 shows one phase of the logic used to provide a current supervised, time-delayed retrip of the protected breaker. To enable this function, set the DRTE setting equal to Y. With this setting, the relay starts the RTTD time-delayed pickup timer when the A-phase trip input is asserted if A-phase current is above the 50LD relay element setting. The timer runs as long as current is above the 50LD setting. When the RTTD timer expires, the relay sets the Relay Word TA bit. The TA bit remains asserted for three cycles following dropout of the 50LD element. You may use the TA bit to retrip the protected breaker by setting it in a programmable output mask, as described in ***Section 5: Applications***.

When you set DRTE equal to N, Relay Word bit TA asserts immediately when the TRIP A input is asserted, regardless of the A-phase current measured.

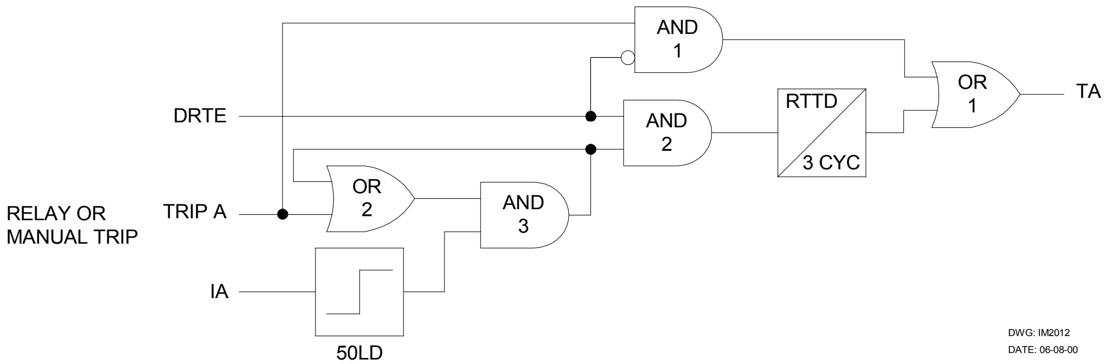

Figure 2.12: Time-Delayed Retrip Logic (SEL-2BFR Relay)

Time-Delayed Breaker Retrip (SEL-2BFR-2 Relay)

Figure 2.13 shows one phase of the current supervised, time-delayed retrip logic. This logic provides the ability to energize a redundant trip coil of the protected breaker after a fixed time delay. The RTTD (Retrip Time Delay) timer provides the retrip time delay. The RTSD (Retrip Seal-In Delay) timer provides a retrip seal-in delay to prevent seal-in during noisy conditions in the TRIP A input.

Enable the time-delayed retrip by setting DRTE (Delayed Retrip Enable) equal to Y. The RTSD timer has a default setting of 0.25 to provide a quarter-cycle seal-in delay. To increase the seal-in delay of the trip input, enter the desired delay in the RTSD setting (Note: This setting should be less than the RTTD setting). Timers RTTD and RTSD will start timing when the A-phase trip input is asserted and the A-phase current is above the 50LD relay element setting. When the RTSD time expires, the TRIP A input will seal in. The RTTD timer will run as long as A-phase current is above the 50LD setting and the TRIP A input is asserted or sealed in. Relay word bit TA will be set when the RTTD timer expires and will remain asserted for three cycles after the 50LD element drops out. Use the TA bit in a programmable output mask to utilize the retrip logic. See ***Section 5: Applications***.

Set the DRTE equal to N to bypass the current-supervised, time-delayed retrip logic. The TA Relay Word bit will immediately assert or deassert after the TRIP A input asserts or deasserts, respectively.

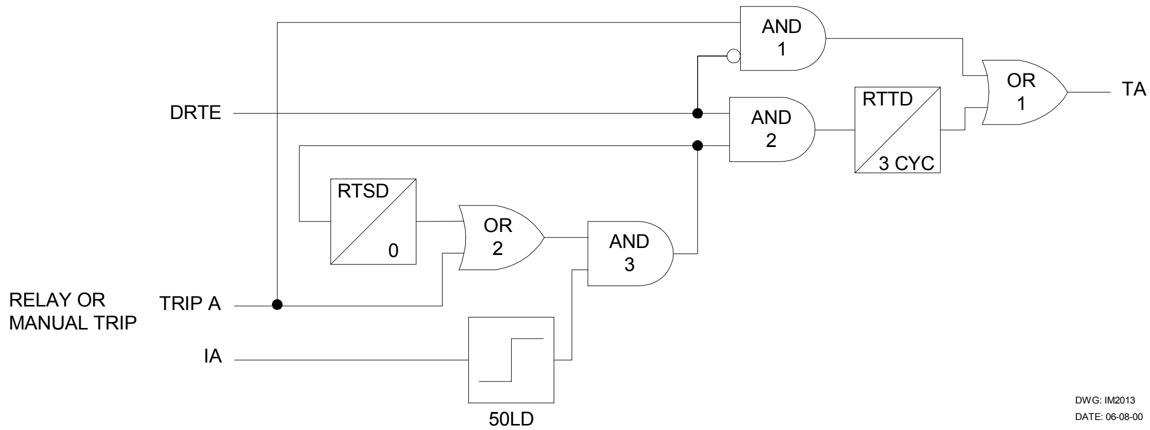

Figure 2.13: Time-Delayed Retrip Logic (SEL-2BFR-2 Relay)

86BF Trip and Reset Logic

MOD Trip Disabled

Figure 2.14 shows the logic used to assert the 86BF trip output and the 86RS reset bit in the Relay Word when MOD Trip logic is disabled (setting ModTrip = N). Figure 2.15 shows the MOD Trip Disabled logic timing.

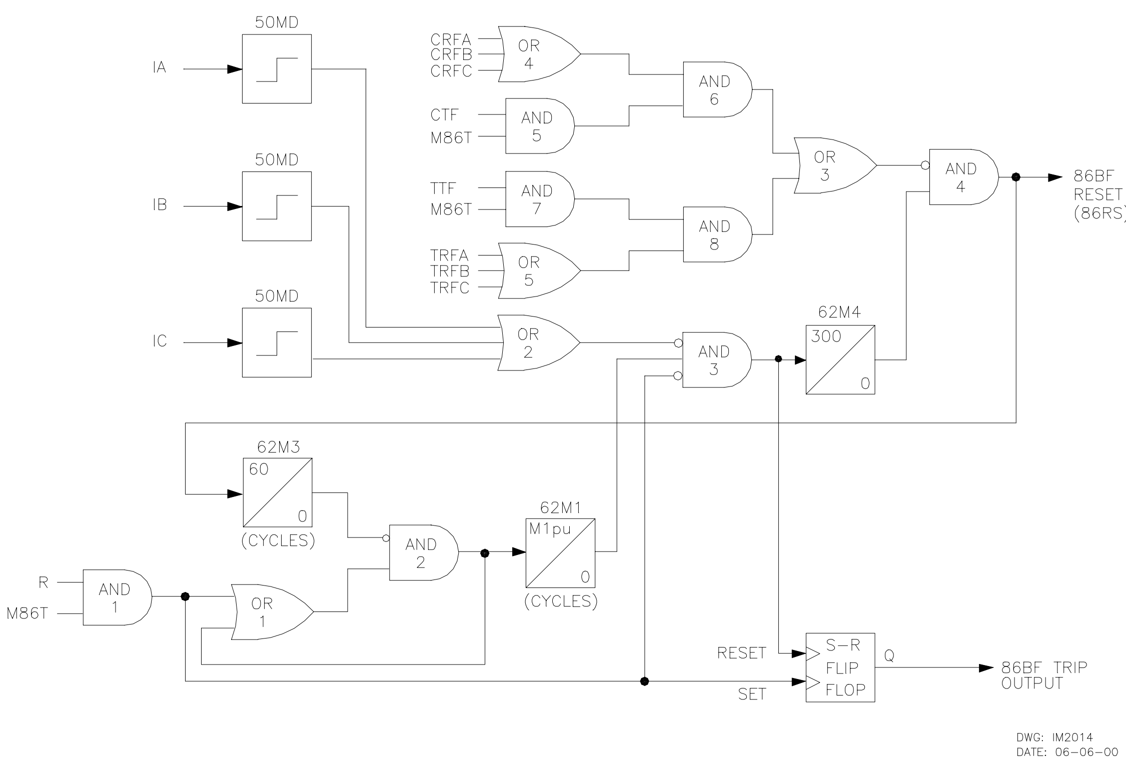

Figure 2.14: 86BF TRIP and Reset Logic (MOD Trip Disabled)

When AND 1 output asserts, the 62M1 timer starts and the 86BF Trip output asserts. After the 62M1 timer expires, if AND 1 output is zero and the 50MD elements are deasserted, the 62M4 timer starts and the 86BF Trip output deasserts. The 62M4 timer has a fixed value of 300 cycles. When the 62M4 timer expires, the 86RS bit asserts for 60 cycles if no protected trip or close resistor has failed.

If the 50MD overcurrent elements have not dropped out when 62M1 times out, the relay postpones 86BF TRIP deassertion and asserts the ALRM bit. As soon as the 50MD overcurrent elements drop out, the 86BF Trip output deasserts and the 62M4 timer starts, as described above.

In two situations, the relay delays assertion of the 86BF Reset bit 86RS. These situations are (1) a Close resistor thermal failure element is asserted and CTF is set in the M86T logic mask, or (2) a trip resistor failure element is asserted and TTF is set in the M86T logic mask. When the thermal failure condition drops out, the 86BF Reset bit asserts for 60 cycles.

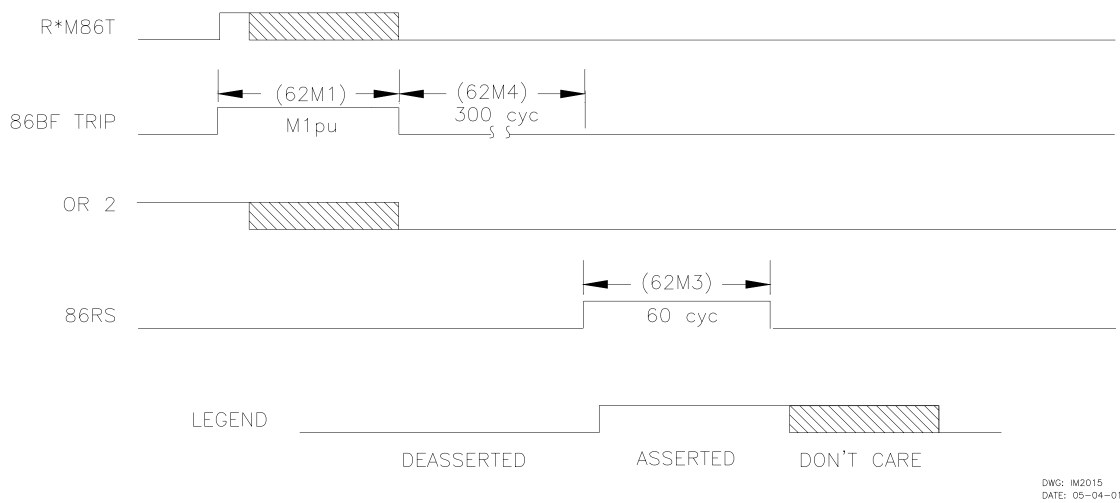

Figure 2.15: MOD Trip Disabled Logic Timing Diagram

MOD Trip Enabled

Figure 2.16 shows the logic used to assert the 86BF trip output and the 86RS reset bit in the Relay Word when MOD Trip logic is enabled. Figure 2.17 shows the timing of the MOD Trip Enabled logic.

The 86BF Trip output asserts and the 62M1 timer starts when the Relay Word logically ANDed with the M86T mask is not zero. If the 50MD elements have dropped out when the 62M1 timer expires, the MDT (MOD Trip) bit asserts and the 62M2 timer starts. When the 62M2 timer expires, if no 50LD overcurrent element is picked up, the MOD status input is deasserted, and the 86BF Trip condition has cleared, the 86BF Trip output deasserts and the 62M4 timer starts. Five seconds (62M4 time) after the 86BF Trip output deasserts, the 86RS bit asserts, and one second later both MDT and 86RS deassert.

If the 50MD overcurrent elements have not dropped out when 62M1 expires, MDT assertion is delayed until all three 50MD elements drop out.

If any 50LD overcurrent element is picked up when the 62M2 timer expires, the Relay Word ALRM bit asserts for one second and the message: “Current after ModTrip” is stored in the ALRM buffer. When the 50LD elements drop out, the timing sequence continues as described above.

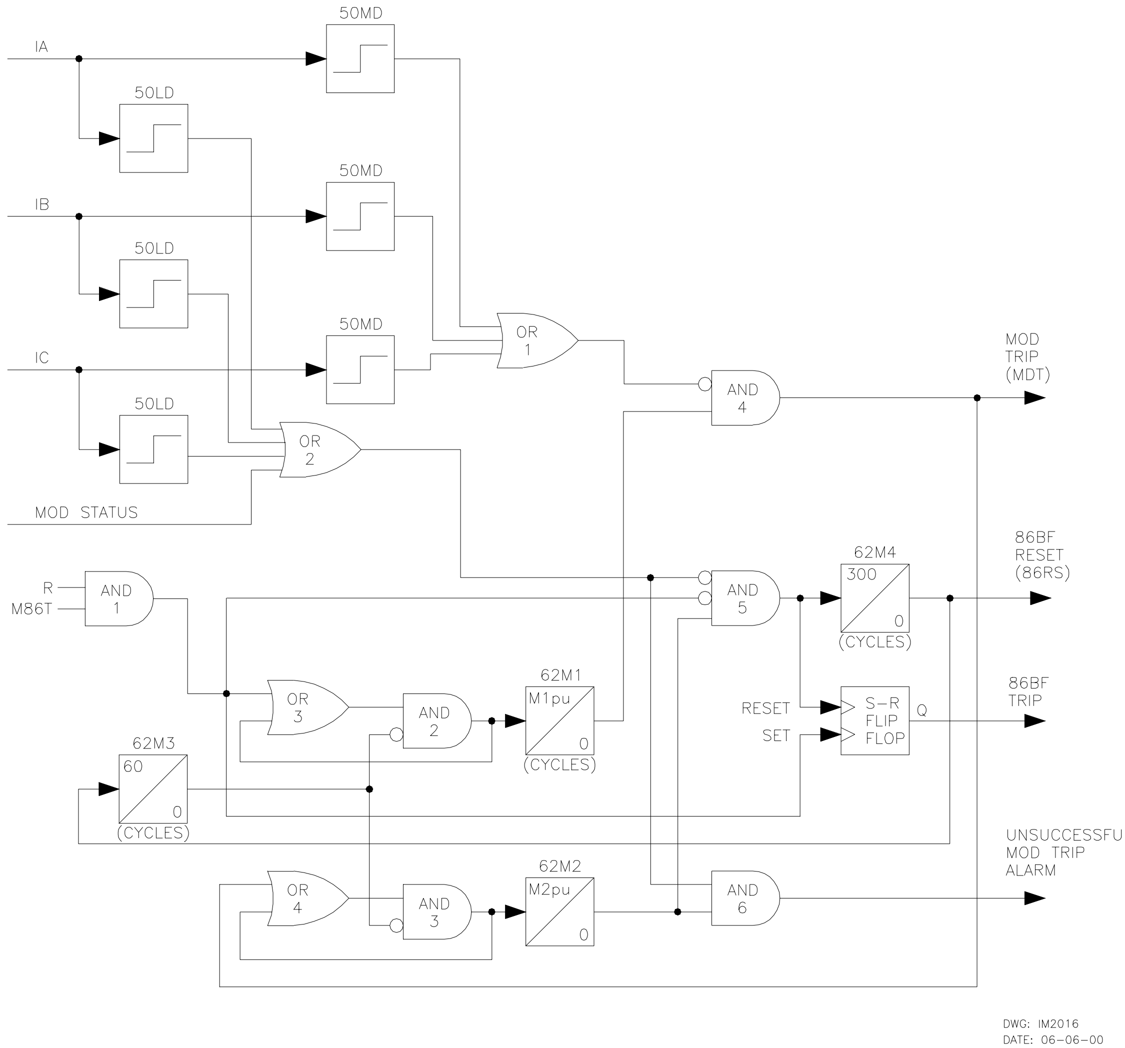

Figure 2.16: 86BF TRIP, Reset, and MOD Trip Logic (MOD Trip Enabled)

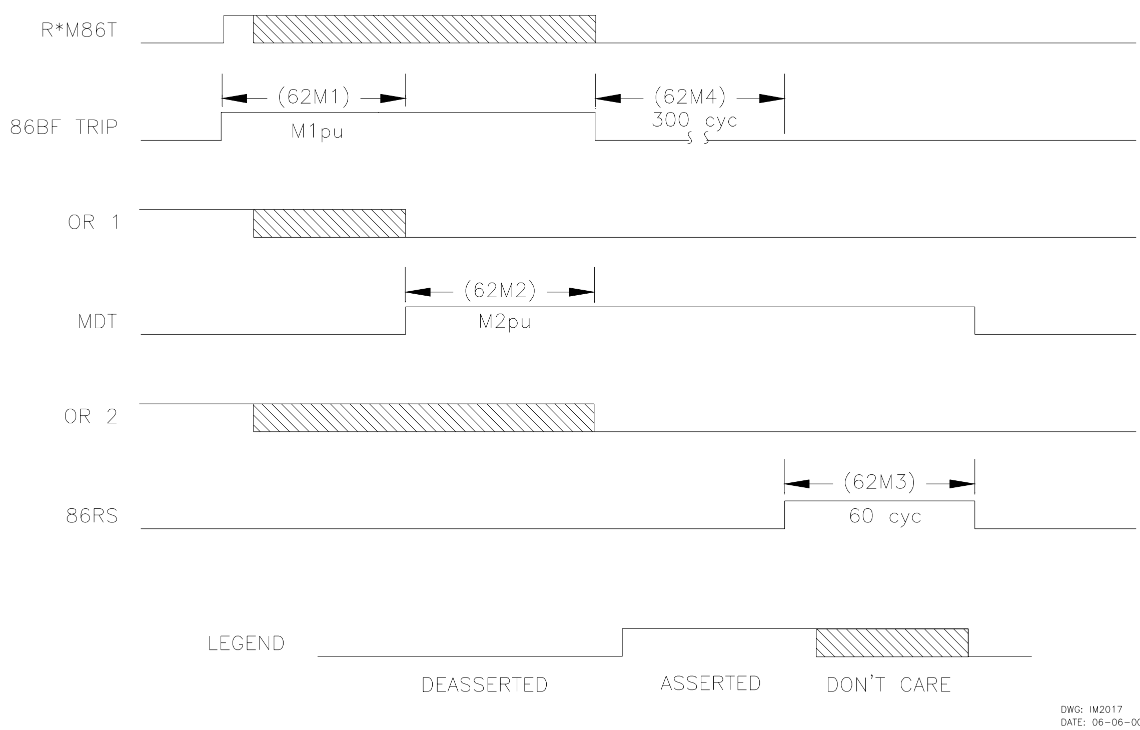

Figure 2.17: MOD Trip Enabled Logic Timing Diagram

52BV Logic

Figure 2.18 shows the logic used to determine the state of 52BV in the Relay Word. The 52BV bit asserts if the 52A input is deasserted while no phase current is above the 50LD setting. The 52BV bit deasserts when the 52A input asserts, or when any phase current exceeds the 50LD setting.

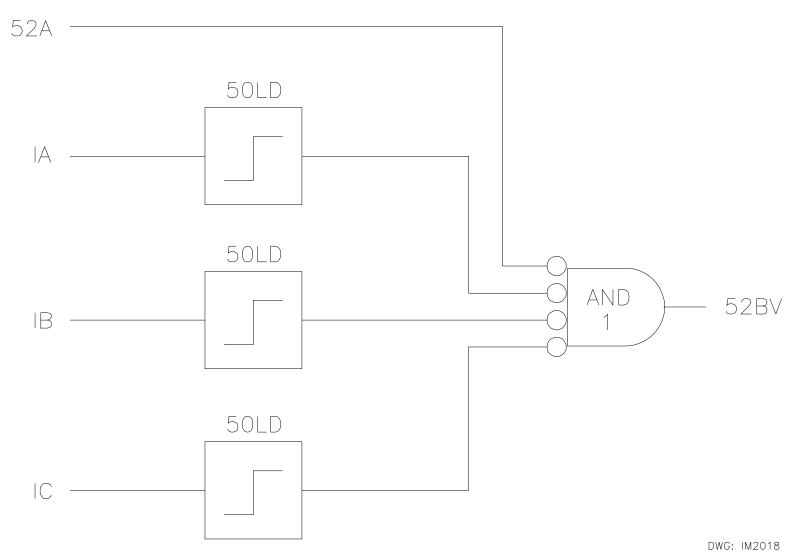

Figure 2.18: 52BV Logic

Alarm Logic

In addition to the relay ALARM output described above, the ALRM bit is available in the Relay Word. The ALRM bit indicates dangerous or abnormal conditions related to operation of the protected circuit breaker.

You can set a programmable output contact to close and indicate when the relay detects an alarm condition. When the ALRM bit is set in a programmable output contact logic mask, operation of the contact follows ALRM bit assertion by one quarter-cycle.

The relay sets the ALRM bit for one second and stores a message in the alarm message buffer when any of the following conditions are detected:

Failed CB trip resistors put in service
Failed CB close resistors put in service
52A contradicts voltage
Current while open
Trip while open
CB did not close
Blown pot fuse
Current after MOD Trip
MOD contradicts current
MOD Trip failed
Volts across closed CB
Slow trip
Slow close

To view the ALRM message buffer, execute the **STATUS** command.

The following items explain conditions that cause ALRM assertion.

Failed CB Trip Resistors Put in Service

ALRM asserts if any trip resistor thermal failure bit is asserted and 86RS bit or close input assertion occurs.

Failed CB Close Resistors Put in Service

ALRM asserts if any close resistor thermal failure bit is asserted and 86RS bit or close input assertion occurs.

52A Contradicts Voltage

ALRM asserts if the 59FO overvoltage element picks up when 52A is asserted.

Current While Open

ALRM asserts if any 50LD element picks up when 52A is not asserted.

Trip While Open

ALRM asserts if a trip input asserts while the 59FO element for that phase is picked up.

CB Did Not Close

ALRM asserts if all three 50LD elements have not picked up three seconds after close input assertion. Three-phase current resets the three-second timer to prevent possible ALRM assertion during reclosing sequences.

Blown Pot Fuse

ALRM asserts if the 52A input is asserted, no trip or close input is asserted, and the 47Q negative-sequence overvoltage element picks up.

Current After MOD Trip

ALRM asserts if any phase 50LD element is picked up when the 62M2 timer expires following an 86BF Trip when MOD Trip logic is enabled.

MOD Contradicts Current

ALRM asserts if MOD Trip is enabled, the 50MD element is picked up, and the MOD STATUS input is not asserted, indicating that the MOD is open.

MOD Trip Failed

ALRM asserts if MOD Trip (MDT) asserts, but the trip is unsuccessful. See “Unsuccessful MOD Trip Alarm” output shown in Figure 2.16.

Volts Across Closed CB

ALRM asserts if the voltage across a breaker pole exceeds the Vwarn setting while that phase 50LD element is picked up.

Slow Trip

ALRM asserts if the phase 50LD element is picked up Topen time following phase trip input assertion.

Slow Close

ALRM asserts if the phase 50LD element is not picked up Tclose time following close input assertion.

Serial Interfaces

The SEL-2BFR Relay is equipped with two EIA-232 serial communications ports. PORT 2 has 9-pin connectors on both the front and rear panels, designated PORT 2F and PORT 2R, respectively.

PORT 2R, located on the relay rear panel, typically is used with an SEL-2020 or an SEL-2030 Communications Processor or local printer. PORT 2F is always available for short-term local communications with a portable computer or printing terminal. Simply plug the device into the front-panel port. The relay automatically discontinues communications with PORT 2R and addresses PORT 2F. When testing or data retrieval is complete, unplug the temporary device from PORT 2F. The relay automatically resumes communication with the device connected to PORT 2R.

The baud rate for each port is set by jumpers near the front of the main board. You can access these jumpers by removing either the top cover or front panel. Available baud rates are 300, 600, 1200, 2400, 4800, and 9600.

The serial data format is:

Eight data bits

Two stop bits

No parity

The serial communications protocol appears in ***Section 3: Communications***.

IRIG-B Input Description

The port labeled J201/AUX INPUT accepts demodulated IRIG-B time code input. The IRIG-B input circuit is a 56-ohm resistor in series with an optocoupler input diode. The input diode has a forward drop of about 1.5 volts. Driver circuits should put approximately 10 mA through the diode when "on."

On the Plug-in Connector Model, Ports 1 and 2R may be configured to accept demodulated IRIG-B input. When JMP 13 and JMP 14 are bridged, Pins 6 and 4 will accept –IRIG-B and +IRIG-B, respectively. See Table 3.2 for part pinouts.

The IRIG-B serial data format consists of a one-second frame containing 100 pulses and divided into fields. The relay decodes second, minute, hour, and day fields and sets the relay clock accordingly.

When IRIG-B data acquisition is activated either manually (with the **IRIG** command) or automatically, the relay reads two consecutive frames. It updates the older frame by one second and compares the frames. If they do not agree, the relay considers the data erroneous and discards it.

The relay reads the time code automatically about once every five minutes. The relay stops IRIG-B data acquisition 10 minutes before midnight on New Year's Eve so the relay clock may implement the year change without interference from the IRIG-B clock. Ten minutes after midnight, the relay restarts IRIG-B data acquisition.

Please note that all six breaker fail schemes use the 50FT current element. This element is defined as a protection element and takes precedence over other tasks during the period of element assertion. In particular, the IRIG-B time synchronizing function will not be processed during this period. For 50FT element settings below load current (50FT element asserted during normal operating conditions), consider one of the load breaker fail schemes. Load current breaker fail schemes use the 50LD elements and the IRIG-B time synchronizing function is unaffected.

EVENT REPORTING

The relay retains a 15-cycle data record for each of the last nine events. The record includes input currents and voltages, Relay Word elements, input contacts, and output contacts. The relay saves a report when any of the following occur:

- The relay trips
- User-selected Relay Word bits, inputs, or outputs assert
- User executes the **TRIGGER** command

The relay stores the last nine event reports in a buffer. You can examine any full-length report stored in the relay using the **EVENT** command. The relay clears the event buffer when relay power is interrupted or when you make a setting or logic change.

The relay stores 100 event summaries in nonvolatile memory. The event summaries are retained through setting changes and losses of control power. Summaries contain breaker operation data such as event type, mechanical and electrical breaker operating times, and the event date and time. You can use this data to monitor breaker wear and more effectively schedule routine breaker maintenance.

Section 4: Event Reporting has further information regarding the generation, content, and analysis of event reports and summaries saved by the relay.

METERING

The meter function shows the values of ac current through the breaker, voltage across it, and real and reactive power dissipated in it (see ***Section 3: Communications***, **METER** command). You can execute the **METER** command locally or remotely to check breaker conditions.

SELF-TESTING

The relay runs a variety of self-tests. Some tests have warning and failure states; others only have failure states. The relay generates a status report after any self-test warning or failure.

The relay closes the ALARM contacts after any self-test fails. When the relay detects certain failures, it disables the breaker control functions and places the output relay driver port in an input mode. No outputs may be asserted when the relay is in this configuration. The relay continuously runs all self-tests.

Offset

The relay measures dc offset voltage of each analog input channel and compares the value against fixed limits. If an offset measurement is outside the fixed limits, the relay declares a warning or failure.

Power Supply

The relay measures the internal power supply voltages and compares the values against fixed limits. If a voltage measurement is outside the limits, the relay declares a warning or failure.

Table 2.5: Power Supply Self-Test Limits

Supply	Warning Thresholds		Failure Thresholds	
+5 V	5.3 V	4.7 V	5.4 V	4.6 V
+15 V	15.8 V	14.2 V	16.2 V	13.8 V
–15 V	–15.8 V	–14.2 V	–16.2 V	–13.8 V

Random-Access Memory

The relay continuously checks the random-access memory (RAM). If a byte cannot be written to or read from, the relay declares a RAM failure. There is no warning state for this test.

Read-Only Memory

The relay checks the read-only memory (ROM) by computing a checksum. If the computed value does not agree with the stored value, the relay declares a ROM failure. There is no warning state for this test.

Analog-to-Digital Converter

The relay verifies A/D converter function by checking the A/D conversion time. The test fails if conversion time is excessive or a conversion starts and never finishes. There is no warning state for this test.

Master Offset

The master offset (MOF) test checks the dc offset in the multiplexer/analog to digital converter circuit. The relay selects a grounded input to sample for dc offset.

Settings

Every time you set the relay, it calculates a checksum for the settings. The checksum is stored in nonvolatile memory with the settings. The relay recalculates and compares the checksum at least every five minutes. If the checksums disagree, the setting test fails and the relay disables all protective and control functions.

The following table shows relay actions for any self-test condition: warning (W) or failure (F).

Table 2.6: Self-Test Summary

Self-Test	Limits	Status Message	Protection Disabled	Control Disabled	Alarm Output
RAM	----	F	YES	YES	permanent closure
ROM	----	F	YES	YES	permanent closure
Settings	----	F	YES	YES	permanent closure
A/D	----	F	YES	no	permanent closure
+5 V	±0.3 V	W	no	no	no ALARM closure
	±0.4 V	F	YES	YES	permanent closure
±15 V	±0.8 V	W	no	no	no ALARM closure
	±1.2 V	F	YES	no	permanent closure
Channel	±50 mV	W	no	no	no ALARM closure
Offsets	±75 mV	F	no	no	one-second pulse
Master	±50 mV	W	no	no	no ALARM closure
Offset	±75 mV	F	no	no	one-second pulse

PROGRAMMABLE LOGIC MASK CONCEPT

Figure 2.19 illustrates the programmable logic mask concept by comparing it to discrete relay element connections. At the top, the figure shows relay element contacts X, Y, and Z connected to a common reference, such as the positive pole of the battery. The ends of these contacts are connected to knife switches, while the other side of the switches is connected to drive an auxiliary relay labeled A1. The knife switch positions select which relay elements can pick up the auxiliary relay. In the figure, switches SX and SY are closed, so closure of contact X or Y causes A1 to pick up. This is expressed in Boolean terms next to the A1 output contact by the notation X + Y, where "+" indicates the logical "OR" operation.

This logic scheme may be modified by setting switches SX, SY, and SZ to other positions. If an application requires combinations of contacts X, Y, and Z to control other auxiliary relays, diodes must be used in each contact path. These diodes ensure that the logic settings for this scheme do not affect other auxiliary relays.

In programmable mask logic, the states of all relay elements are collected into a single group of binary digits called the Relay Word. Each bit reports the state of one relay element. A zero indicates that the element is not picked up; one indicates that the element is picked up.

Figure 2.19 shows a three-bit Relay Word with elements X, Y, and Z. Each bit corresponds to one relay element contact in the contact-logic equivalent. The operator sets or clears bits in the mask for the A1 output rather than using switches to select which elements control the A1 output (see ***Section 3: Communications***, **LOGIC** command). In the figure, the operator selected the X and Y elements and deselected the Z element by setting the mask bits to (1,1,0). The computer ANDs each bit in the Relay Word with the corresponding bit the operator set in the mask. Next, it ORs all three outputs together, forming the condition which drives the output relay A1. A convenient shorthand way of expressing this bitwise AND followed by an OR operation is:

A1 = R * MA1

where R is the Relay Word (X,Y,Z), MA1 is the mask (1,1,0), and "*" indicates the operation of bitwise ANDing followed by the OR operation.

While the mask elements are fixed, the Relay Word is updated each quarter-cycle. In this example, if the X or Y element is set to (1) in the Relay Word, the A1 contact closes. The state of the A1 contact is independent of the Z element in the Relay Word because the corresponding Z element in the mask equals zero.

The relay has user programmable logic masks which control tripping, programmable output contacts, and event report generation. Logic masks are saved in nonvolatile memory with the other settings and retained through losses of control power.

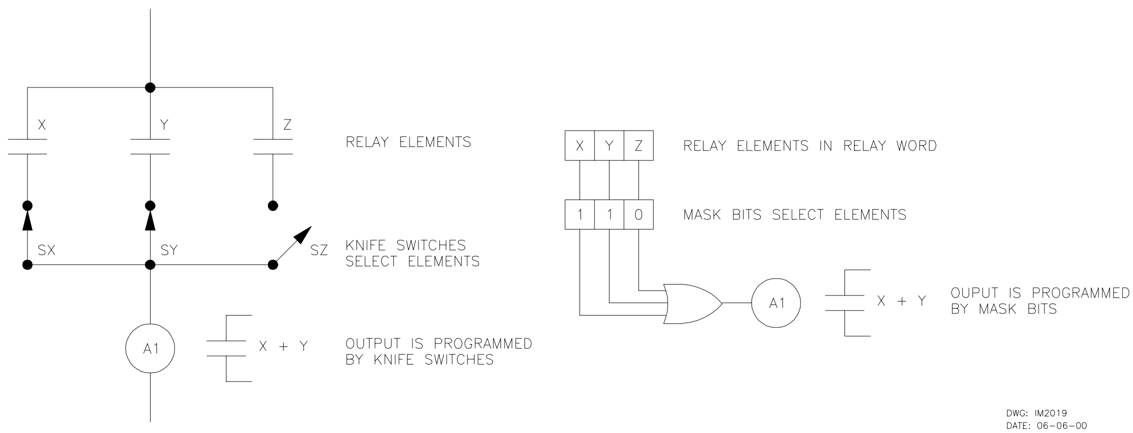

Figure 2.19: Programmable Logic Mask Analogy

OVERCURRENT ELEMENT OPERATING TIME CURVES

The following figures illustrate the pickup and dropout times of the 50FT, 50MD, and 50LD phase overcurrent elements. Ten tests were performed at each multiple of element setting. Pickup and dropout times were measured and operating times were logged, then maximum, mean, and minimum times were plotted. The operating times do not include output contact operating time delay, thus they are accurate for determining element operating times for use with SEL-2BFR Relay internal logic.

You may verify these operating times using relay output contact closure to indicate element assertion. Due to contact operating times, your measured operating times will be approximately three milliseconds longer than shown on element pickup and eight milliseconds longer than shown on element dropout.

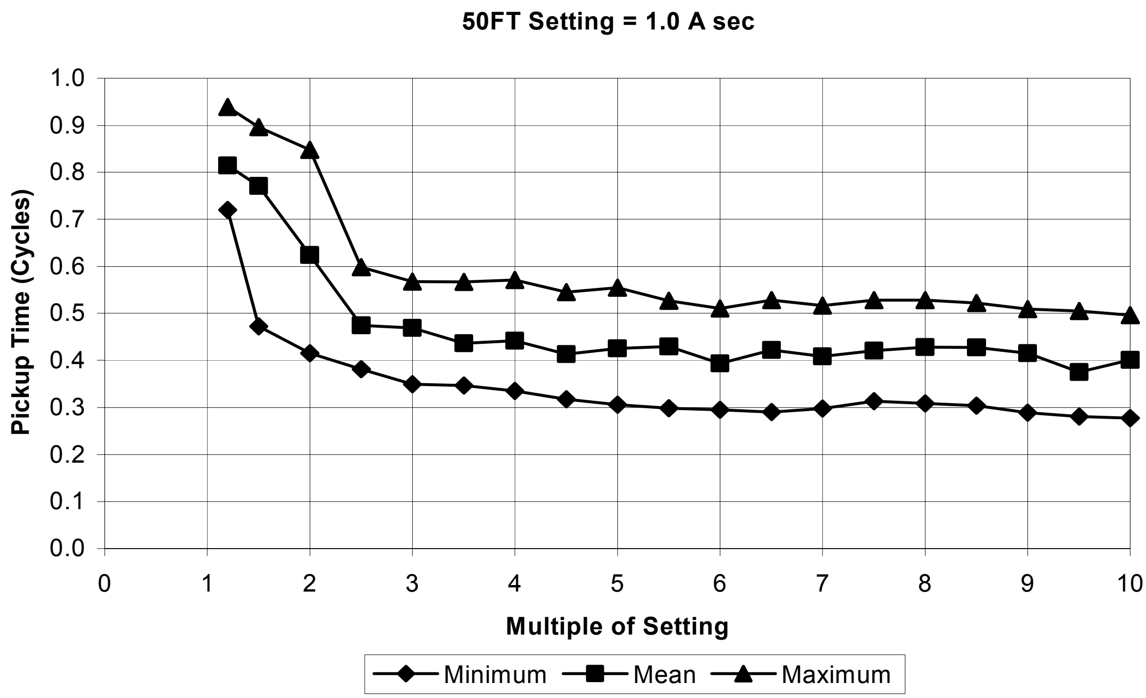

Figure 2.20: 50FT Pickup Time Curves

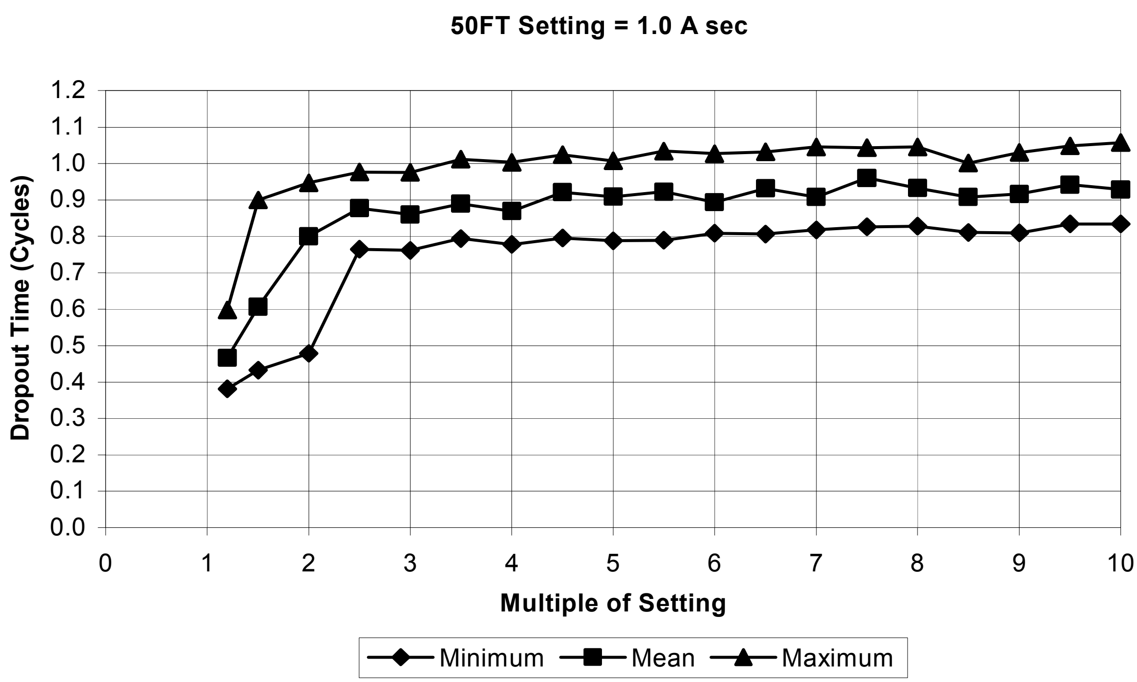

Figure 2.21: 50FT Dropout Time Curves

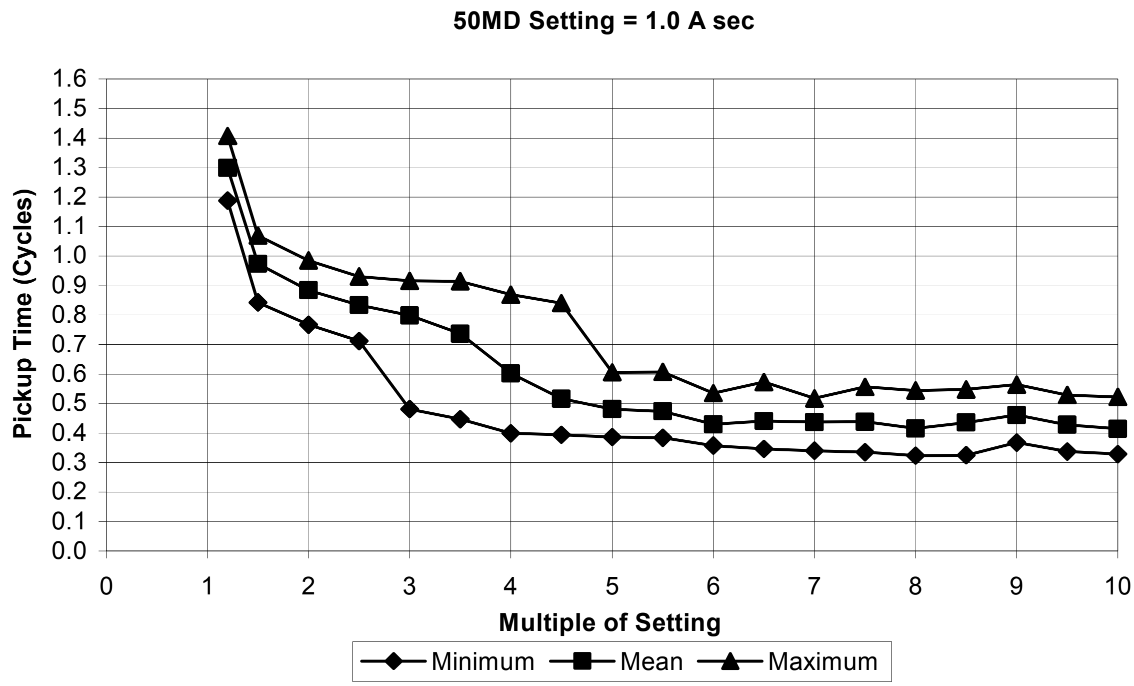

Figure 2.22: 50MD Pickup Time Curves

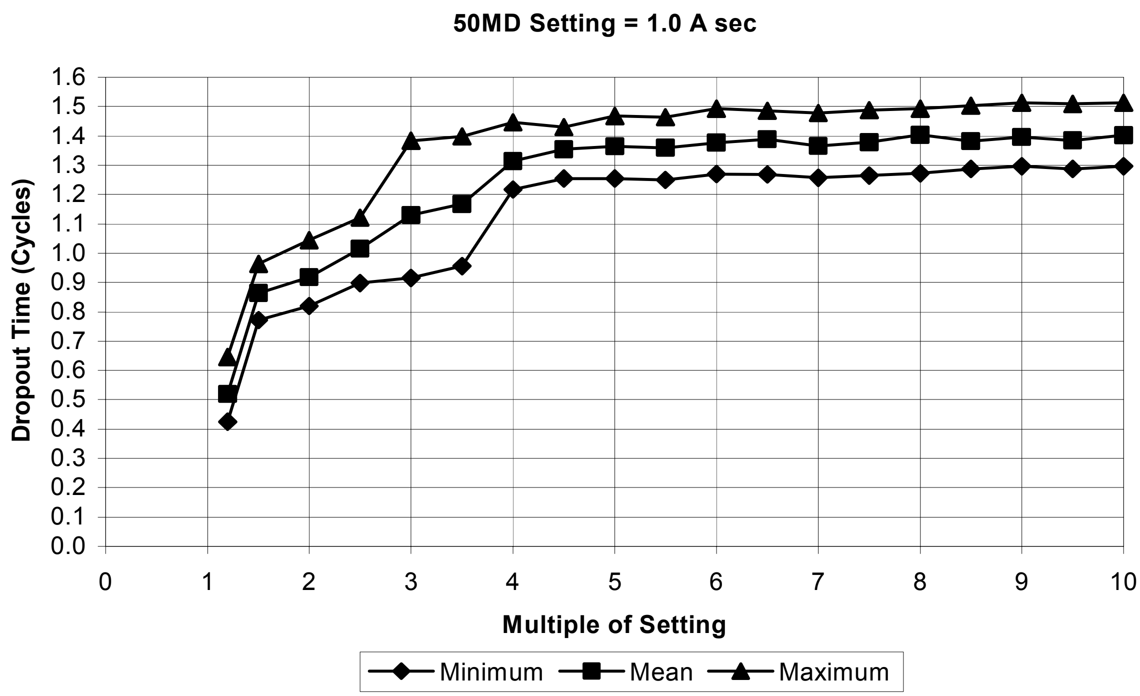

Figure 2.23: 50MD Dropout Time Curves

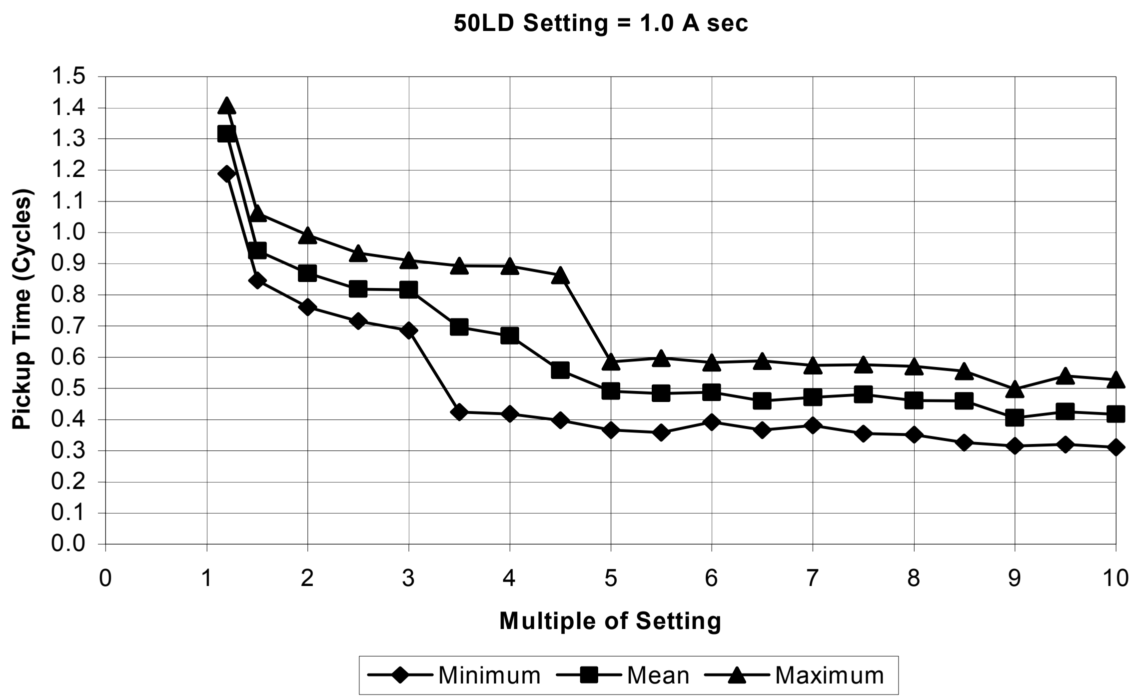

Figure 2.24: 50LD Pickup Time Curves

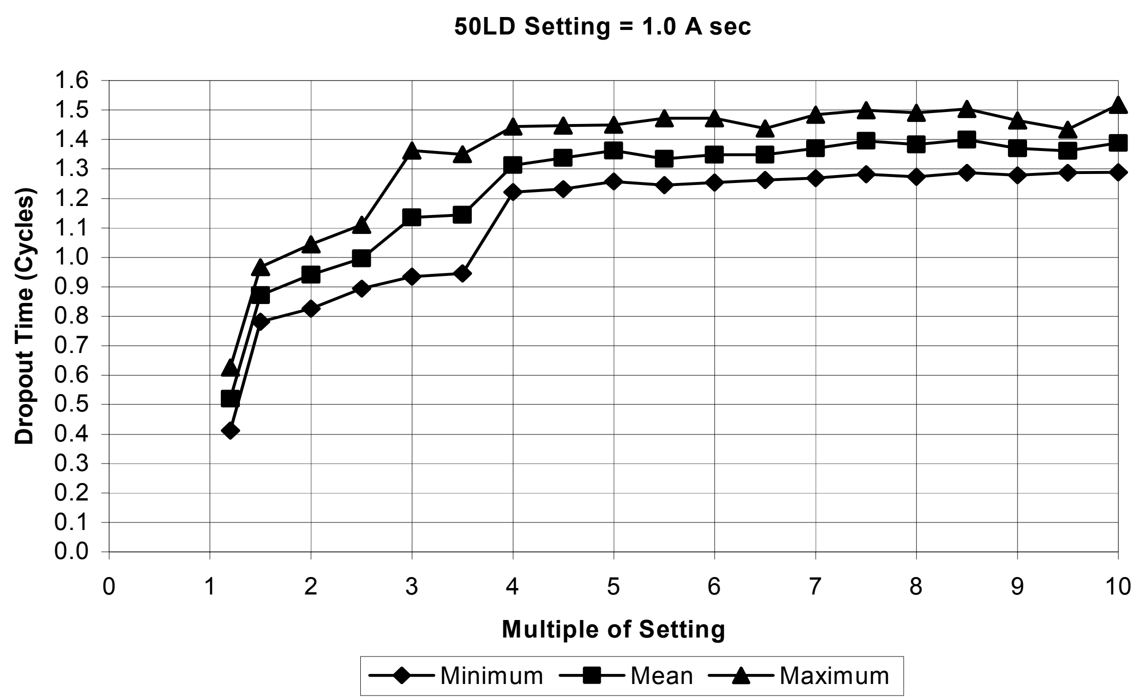

Figure 2.25: 50LD Dropout Time Curves

COMMUNICATIONS
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COMMUNICATIONS

INTRODUCTION

The relay is set and operated via serial communications interfaces connected to a computer terminal and/or modem, the SEL-PRTU (Protective Relay Terminal Unit), or an SEL-2020 Communications Processor. Communication serves these purposes:

1. The relay responds to commands spanning all functions, e.g., setting, metering, and control operations.

2. The relay generates an event record for assertions of the TRIP output, for an event triggering command, or for pickup of any relay element that triggers an event record.

3. The relay transmits messages in response to changes in system status, e.g., self-test warning.

It is impossible to disable any relaying or control functions via communications, unless a user enters erroneous or improper settings with the SET or LOGIC commands.

Note: In this manual, commands to type appear in bold and upper case: **OTTER**. Keys to press appear in bold, upper case, and brackets: **<ENTER>**.

Relay output appears boxed and in the following format:

```
Example 500 kV Line                         Date: 6/1/92            Time: 01:01:01
```

SERIAL PORT CONNECTIONS AND CONFIGURATIONS

The SEL-2BFR Relay is equipped with two EIA-232 serial communications ports. PORT 2 has 9-pin connectors on both the front and rear panels, designated PORT 2F and PORT 2R, respectively.

PORT 2R, located on the relay rear panel, is typically used with an SEL-2020 Communications Processor or local printer. PORT 2F is always available for short term local communications with a portable computer or printing terminal. Simply plug the device into the front panel port. The relay automatically discontinues communications with PORT 2R and addresses PORT 2F. When testing or data retrieval is complete, unplug the temporary device from PORT 2F. The relay automatically resumes communication with the device connected to PORT 2R.

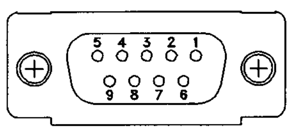
Serial communications PORT 1 and the Auxiliary Input for demodulated IRIG-B time code input are located on the relay rear panel.

Communications port baud rate jumpers are located along the front edge of the circuit board. To select a baud rate for PORT 1 or PORTs 2, remove the relay front panel. The jumpers are visible near the center of the relay drawout assembly, to the right of the target LEDs. Carefully move the jumpers using needle-nosed pliers. Available rates are 300, 600, 1200, 2400, 4800, and 9600 baud.

Caution: Do not select two baud rates for the same port as this can damage the relay baud rate generator. The relay is shipped with PORT 1 set to 300 baud and PORT 2F/2R set to 2400 baud.

The serial data format is:

Eight data bits
Two stop bits
No parity bit



(female chassis connector, as viewed from outside panel)

Figure 3.1: SEL-2BFR Relay Nine-Pin Connector Pin Number Convention

On the Plug-in connector model, Ports 1 and 2R may be configured to accept demodulated IRIG-B input. When JMP13 and JMP14 are bridged, pins 6 and 4 will accept -IRIG-B and +IRIG-B, respectively. See Table 3.2 for port pinouts.

Table 3.1 lists port pin assignments and signal definitions for the Conventional Terminal Block model.

Table 3.1: SEL-2BFR Conventional Terminal Block Model Relay Serial Port Connector Pin Assignments

Pin	PORT 1, PORT 2R	PORT 2F	Description
1	+5 Vdc	N/C	+5 Vdc available if JMP12 installed.
2	RXD	RXD	Receive data input.
3	TXD	TXD	Transmit data output.
4	+12 Vdc	N/C	+12 Vdc available if JMP13 installed.
5	GND	GND	
6	-12 Vdc	N/C	-12 Vdc available if JMP14 installed.
7	RTS	RTS	The SEL-2BFR Relay asserts this line under normal conditions. When its received-data buffer is full, the line is deasserted, and asserts again when the buffer has sufficient room to receive more data. Connected devices should monitor RTS (usually with their CTS input) and stop transmission whenever the line deasserts. If transmission continues, data may be lost.
8	CTS	CTS	The SEL-2BFR Relay monitors CTS, and transmits characters only if CTS is asserted.
9	GND	GND	Ground for ground wires and shields.

Table 3.2 lists port pin assignments and signal definitions for the Plug-in Connector model.

Table 3.2: SEL-2BFR Plug-in Connector Model Relay Serial Port Connector Pin Assignments

Pin	PORT 1, PORT 2R	PORT 2F	Description
1	+5 Vdc	N/C	+5 Vdc available if JMP12 installed.
2	RXD	RXD	Receive data input.
3	TXD	TXD	Transmit data output.
4	+IRIG-B	N/C	+IRIG-B available if JMP14 installed.
5	GND	GND	
6	-IRIG-B	N/C	-IRIG-B available if JMP13 installed.
7	RTS	RTS	The SEL-2BFR Relay asserts this line under normal conditions. When its received-data buffer is full, the line is deasserted, and asserts again when the buffer has sufficient room to receive more data. Connected devices should monitor RTS (usually with their CTS input) and stop transmission whenever the line deasserts. If transmission continues, data may be lost.
8	CTS	CTS	The SEL-2BFR Relay monitors CTS, and transmits characters only if CTS is asserted.
9	GND	GND	Ground for ground wires and shields.

COMMUNICATIONS PROTOCOL

Communications protocol consists of hardware and software features. Hardware protocol includes the control line functions described above. The following software protocol is designed for manual and automatic communications.

1. All commands received by the relay must be of the form:

   <command><CR> or <command><CRLF>

   Thus, a command transmitted to the relay should consist of the command followed by either a carriage return or a carriage return and a line feed. You may truncate commands to the first three characters. Thus, **EVENT 1 1 <ENTER>** would become **EVE 1 1 <ENTER>**. You can use upper and lower case characters without distinction, except in passwords.

Note: The ENTER key on most keyboards is configured to send the ASCII character 13 (^M) for a carriage return. This manual instructs you to press the ENTER key after commands, which should send the proper ASCII code to the relay.

2. The relay transmits all messages in the following format:

   <STX> <MESSAGE LINE 1> <CRLF>
   <MESSAGE LINE 2> <CRLF>
   .
   .
   <LAST MESSAGE LINE> <CRLF> <PROMPT> <ETX>

   Each message begins with the start-of-transmission character (ASCII 02) and ends with the end-of-transmission character (ASCII 03). Each line of the message ends with a carriage return and line feed.

3. The relay indicates the volume of data in its received-data buffer using an XON/XOFF protocol.

   The relay transmits XON (ASCII hex 11) and asserts the RTS output when the buffer drops below ¼ full.

   The relay transmits XOFF (ASCII hex 13) when the buffer fills above ¾ full. It deasserts the RTS output when the buffer is approximately 95% full. Automatic transmission sources should monitor for the XOFF character so they do not overwrite the buffer. Transmission should terminate at the end of the message in progress when XOFF is received and may resume when the relay sends XON.

4. You can use an XON/XOFF procedure to control the relay during data transmission. When the relay receives XOFF during transmission, it pauses until it receives an XON character. If there is no message in progress when the relay receives XOFF, it blocks transmission of any message presented to its buffer. The relay transmits the message after it receives XON.

   The CAN character (ASCII hex 18) aborts a pending transmission. This is useful in terminating an unwanted transmission.

5. Control characters can be sent from most keyboards with the following keystrokes:

   XON: **<CTRL>Q** (hold down the Control key and press Q)
   XOFF: **<CTRL>S** (hold down the Control key and press S)
   CAN: **<CTRL>X** (hold down the Control key and press X)

COMMAND CHARACTERISTICS

The relay responds to commands sent to either serial communications port. A two level password system provides security against unauthorized access.

When the relay is first turned on, the instrument is in Access Level 0 and honors only the ACCESS command. It responds "Invalid command" to any other entry.

You may enter Access Level 1 with the ACCESS command and first password. The Level 1 password is factory set to OTTER and may be changed with the PASSWORD command in Access Level 2. Most commands can be used in Access Level 1.

Critical commands such as SET operate only in Access Level 2. You may enter Access Level 2 with the 2ACCESS command and second password. The Level 2 password is factory set to TAIL and may be changed with the PASSWORD command.

Startup

Immediately after power is applied, the relay transmits the following message to the port(s) designated automatic:

```
Example 500 kV Breaker                 Date: 6/1/92            Time: 01:01:01

SEL-BFR
=
```

The ALARM relay should pull in.

The = represents the Access Level 0 prompt.

The relays are shipped with PORT 2 designated automatic; you may use the SET command to change this designation (see SET command, AUTO setting). This allows you to select PORT 1, PORT 2, or both ports to transmit automatic responses from the relay.

To enter Level 1, type the following on a terminal connected to PORT 2:

```
=ACCESS <ENTER>
```

The response is:

```
Password: ? @@@@@@
```

Enter the Level 1 password **OTTER** and press **<ENTER>**. The response is:

```
Example 500 kV Breaker                         Date: 6/1/92            Time: 01:01:44

Level 1

=>
```

The Access Level 1 prompt is =>. Now you can execute any Level 1 command.

Use a similar procedure to enter Access Level 2:

Type **2ACCESS <ENTER>**. The relay pulses the ALARM relay contact closed for approximately one second, indicating an attempt to enter Access Level 2. Enter the proper password, **TAIL**, when prompted. After you enter the second password, the relay opens access to Level 2, as indicated by the following message and Level 2 prompt (=>>):

```
=>2ACCESS <ENTER>
Password:   TAIL <ENTER>

Example 500 kV Breaker                         Date: 6/1/92            Time: 01:03:32

Level 2

=>>
```

You can enter any command at this prompt.

Command Format

Commands consist of three or more characters; only the first three characters of any command are required. You may use upper or lower case characters without distinction, except in passwords.

You must separate arguments from the command by spaces, commas, semicolons, colons, or slashes.

You can enter commands any time after the terminal displays an appropriate prompt.

In this manual, commands to type appear in bold and upper case: **OTTER**. Keys to press appear in bold, upper case, and brackets: **<ENTER>**.

COMMAND DESCRIPTIONS

Access Level 0 Command

ACCESS

ACCESS allows you to enter Access Level 1. The password is required unless you install JMP103 on the main board. The first password is set to OTTER at the factory; use the Level 2 command PASSWORD to change passwords.

The following display indicates successful access.

```
=ACCESS <ENTER>
Password: ? OTTER <ENTER>

Example 500 kV Breaker                    Date: 6/1/92            Time: 05:19:05

Level 1

=>
```

The => prompt indicates Access Level 1.

If you enter incorrect passwords during three consecutive attempts, the relay pulses the ALARM contact closed for one second. This feature can alert personnel to an unauthorized access attempt if the ALARM contact is connected to a monitoring system.

Access Level 1 Commands

2ACCESS

2ACCESS allows you to enter Access Level 2. The password is required unless you install JPM103. The second password is set to TAIL at the factory; use the Level 2 command PASSWORD to change passwords.

The following display indicates successful access:

```
=>2ACCESS <ENTER>
Password: ? TAIL <ENTER>

Example 500 kV Breaker                    Date: 6/1/92            Time: 05:21:05

Level 2

=>>
```

You can use any command at the =>> prompt. The relay pulses the ALARM contact closed for one second after any Level 2 access attempt (unless an alarm condition exists).

DATE m/d/y

DATE displays the date stored by the internal calendar/clock. To set the date, type **DATE mm/dd/yy <ENTER>**. Separate month, day, and year with colons, semicolons, spaces, commas or slashes.

To set the date to June 1, 1992, enter:

```
=>DATE 6/1/92 <ENTER>
6/1/92

=>
```

The relay sets the date, and displays the new date. When the power is first turned on, the relay date is set to match that of the last recorded event.

EVENT n l

EVENT displays an event report. Type **EVENT n <ENTER>** to display a summary report for the Nth event. The parameter n ranges from 1 for the newest event through 100 for the oldest event. To review a complete report for the Nth event, type **EVENT n l <ENTER>**. For complete reports, n ranges from 1 for the newest event through 9 for the oldest event stored in relay memory.

To inspect the newest report in full, type **EVENT 1 l <ENTER>**.

To review a summary of the newest report, type **EVENT 1 <ENTER>**. The summary includes the relay identifier string, event type, 52A-time, IV-time, total energy, date, and time of the event.

As discussed in Communications Protocol, you can control transmissions from the relay with the following keystrokes:

- **<CTRL>S** Pause transmission
- **<CTRL>Q** Continue transmission
- **<CTRL>X** Terminate command

The relay retains event summaries indefinitely; you can always review the last one hundred with the EVENT n command. ***Section 4: Event Reporting*** explains the generation and analysis of event reports.

SET and LOGIC command execution and control power interruptions clear the long event buffers. If an event buffer is empty when you request an event, the relay returns an error message:

```
=>EVENT 1 L <ENTER>
Invalid event

=>
```

HEAT n

The SEL-2BFR Relay tracks heat of the CLOSE and OPEN resistor for each of three phases. The HEAT command allows you to examine resistor status, presenting the heat content of each resistor (with respect to ambient) normalized to the resistor failure threshold, 26CF or 26TF.

For example, if the B-phase OPEN (ORB) resistor contains 1.0 J of internal heat and the failure threshold (26TF) setting is 2.0 J, the HEAT command displays the ORB resistor heat as 0.50.

HEAT command output headings use a simple format. **ORA** heads the A-phase opening resistor column, **CRA** the A-phase closing resistor column, and so on, for the B and C phases.

You can automatically repeat the HEAT command by adding a repeat count upon entry. To repeat the command one thousand times, type **HEAT 1000 <ENTER>**. **<CTRL>X** cancels the listing at any time. Repetition is especially useful when testing thermal elements.

```
=>HEAT 4 <ENTER>

RESISTOR HEAT IN PER UNIT TRIP VALUE

Example 500 kV Breaker                       Date: 6/1/92          Time: 10:16:04

ORA   CRA   ORB   CRB   ORC   CRC

0.00  0.00  0.31  0.11  0.00  0.00
0.00  0.00  0.31  0.11  0.00  0.00
0.00  0.00  0.30  0.11  0.00  0.00
0.00  0.00  0.30  0.11  0.00  0.00

=>
```

You can also reset resistor thermal models with this command. Type **HEAT R <ENTER>** to activate this feature. The relay responds by displaying:

```
RESET THERMAL MODELS (Y/N)?
```

Y <ENTER> resets the heat content of all resistor thermal models to zero. This feature is useful when testing the thermal elements.

HISTORY

HISTORY shows the type, 52A-time, IV-time, total energy, date, and time for each of the last one hundred events.

```
=>HISTORY <ENTER>

Example 500 kV Breaker                          Date: 6/1/92                 Time: 01:16:24

EVENT TYPE    52A    IV-TIME    ENERGY  DATE        TIME
              (cyc)  (cyc)      (MJ)

1     CLOSE   1.50    1.50      0.11  01/06/90  00:18:10.333
2     INT                       0.00  01/04/90  09:08:20.058
3     TRIP3   1.00    2.75      1.53  01/04/90  08:53:55.429
4     CLOSE   1.50    1.50      0.07  01/01/90  00:18:10.258
5     TRIPA   1.00    1.50      0.13  01/01/90  00:18:08.095
6     CLOSE   1.50    1.50      0.04  12/09/89  22:41:33.108
7     TRIP3   1.25    1.50      0.31  12/09/89  22:27:47.870

              (etc. for last 100 events)
=>
```

Data shown in each column of the HISTORY display is derived from the short form event summaries the relay generates when an event report is triggered. ***Section 4: Event Reporting*** includes explanations of data in the event summaries.

IRIG

IRIG directs the relay to read the demodulated IRIG-B time code input at J201 on the rear panel if a time code signal is input.

If the relay reads the time code successfully, it updates the internal clock/calendar time and date to the new reading and transmits a message with the ID string, date, and time.

If no signal is present or the time code cannot be read successfully, the relay sends the following error message:

```
=>IRIG
ERROR in IRIGB datacq.

=>
```

Note: Normally, it is not necessary to synchronize using this command because the relay automatically synchronizes every few minutes. The command is provided to prevent delays during testing and installation.

METER n

METER displays voltages across the circuit breaker, currents through it, and real and reactive power dissipated in it using primary quantities of amperes, kilovolts, megawatts, and megavars.

METER output example:

```
=>METER

Example 500 kV Breaker                        Date: 6/1/92                 Time: 00:16:10

                              Primary Values
              A       B       C       AB      BC      CA
I (A)         994     995     994     1723    1724    1724
V (kV)        0.0     0.0     0.0     0.0     0.0     0.0

P (MW)        0.00
Q (MVAR)      0.00

=>
```

The optional parameter n selects the number of times the relay displays meter data. To display a series of eight meter readings, type **METER 8 <ENTER>**.

QUIT

QUIT returns control to Access Level 0 from Level 1 or 2 and displays the date and time of QUIT execution.

Use this command when you finish communicating with the relay to prevent unauthorized access. Control returns to Access Level 0 automatically after a specified interval of no activity (see the TIME1 and TIME2 settings of the SET command).

SHOWSET

SHOWSET displays current relay settings but does not allow setting modification. The SET command description provides complete information about changing settings.

```
=>SHOWSET

Settings for: Example 500 kV Breaker

Schm = 2        50FT  = 8.60     TTpu  = 6.00     TTdo    = 2.00    62FC = 4.00
50LD = 0.52     62LD  = 5.50     62LP  = 3.25
62AP = 5.25     62AF  = 7.50     E62A  = N        DRTE    = N       RTTD = 2.00
37OP = 2.25     26CF  = 1.45     26CP  = 1.09     26TF    = 4.56    26TP = 3.42
47Q  = 18.70    62OP  = 3.00     CRTC  = 80       TRTC    = 80
59FO = 4.01     62FF  = 30.00    62FP  = 25.00
87UB = 16       62UC  = 12.00    62UF  = 60.00    62UP    = 50.00
50MD = 0.10     62M1  = 600.00   62M2  = 600.00   ModTrip= Y
CTR  = 600      PTR   = 4300
Topen= 2.25     Tclose= 10.25    Vwarn = 0.47
TIME1= 5        TIME2 = 0        AUTO  = 2        RINGS   = 3

Logic settings:

M86T  MA1  MA2  MA3  MA4  MA5  MER
  C1   00   02   00   20   00   20
  80   08   00   00   40   00   48
  81   00   00   02   40   04   42
  00   00   00   00   55   00   55
  00   00   00   00   50   00   5F
  --   --   --   --   --   --   00
  --   --   --   --   --   --   07

=>
```

Note: The SEL-2BFR-2 Relay includes the RTSD setting (not shown).

The LOGIC command description includes a detailed explanation of logic settings. Each column in the logic settings display shows the masks for five rows of the Relay Word. The MER mask includes additional rows for inputs and outputs.

Logic settings appear in hexadecimal format. Table 3.3 provides equivalencies between hexadecimal (hex) and binary numbers. Use the table when you examine logic settings in event reports and the SHOWSET display.

Table 3.3: Hexadecimal/Binary Conversion

Hexadecimal	Binary	Hexadecimal	Binary
0	0000	8	1000
1	0001	9	1001
2	0010	A	1010
3	0011	B	1011
4	0100	C	1100
5	0101	D	1101
6	0110	E	1110
7	0111	F	1111

STATUS

STATUS allows inspection of self-test status. The relay automatically executes the STATUS command whenever a self-test enters a warning or failure state. If this occurs, the relay transmits a STATUS report from the port(s) designated automatic (see SET command, AUTO setting). The STATUS report also includes any breaker operation alarm reports. These are described in *Section 2: Specifications*, and include such conditions as 'Slow Trip,' and 'Current Contradicts 52A Status.'

The STATUS report format appears below:

```
=>STATUS <ENTER>

SELF TEST STATUS Example 500 kV Breaker          Date: 6/1/92          Time: 02:34:43

W=Warning F=Failure

      IA    IB    IC    VA    VB    VC
OS     0     0     0     0     0     0
PS      5.01       +15.05      -14.91
RAM    ROM    A/D   MOF      SET
OK     OK     OK    OK       OK

Alarm History:

WARNING: SLOW CLOSE

Clear ALARM History (Y/N) ? Y <ENTER>

Alarm history cleared.

=>
```

Section 2: Specifications provides full definitions of the self-tests, their warning and failure limits, and the results of test warnings and failures.

The ALARM History is volatile and clears upon power-down. You can also clear it by pressing **Y <ENTER>** at the Clear ALARM History (Y/N) ? prompt. The history contains the latest ALARM events. Use the STATUS command to help determine the cause of breaker alarm conditions. Alarm logic is described in ***Section 2: Specifications***.

TARGET n m

TARGET selects the information displayed on target LEDs and communicates the state of the selected LEDs.

When the relay power is on, the LED display indicates the functions marked on the front panel. The default display shows the information for TARGET 0.

Using the TARGET command, you may select any one of eight sets of data in the following table to print and display on the LEDs.

Table 3.4: Target LED Assignment

LED#:		1	2	3	4	5	6	7	8
n									
[0]	EN	AL	PF	A	B	C	52A	MOD	Relay Targets
[1]	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF	Relay Word row 1
[2]	FOBF	FOPF	59FO	59H	ALRM	TC	TB	TA	Relay Word row 2
[3]	PDBF	PDPF	87UA	87UB	87UC	86RS	MTD	CTF	Relay Word row 3
[4]	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB	Relay Word row 4
[5]	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q	Relay Word row 5
[6]	*	86BF	A1	A2	A3	A4	A5	ALARM	Contact Outputs
[7]	*	*	CLOS	MOD	52A	TPC	TPB	TPA	Contact Inputs

These selections are useful in testing, checking contact states, and remotely reading targets. You can repeat the command by including a count. **TAR 1 1000 <ENTER>** reads and displays Relay Word row 1 one thousand times. This command simplifies testing of displayed elements, inputs, or outputs. Press **<CTRL>X** to stop the repeating display. **TAR R <ENTER>** resets the targets and displays information for target 0.

When finished, type **TAR 0 <ENTER>** to display the fault targets so field personnel do not misinterpret displayed data.

TIME h/m/s

TIME checks the internal clock. To set the clock, type **TIME** and the desired setting, then press **<ENTER>**. Separate hours, minutes, and seconds with colons, semicolons, spaces, commas, or slashes. To set the clock to 23:30:00, enter:

```
=>TIME 23:30:00 <ENTER>
23:30:00
=>
```

A quartz crystal oscillator provides the time base for the internal clock. You can set the time clock automatically with the relay time code input and a source of demodulated IRIG-B time code.

TRACE n

The TRACE command permits examination of all current, voltage, relay element, output, and input contact data in a format similar to an event report. This function is especially useful for testing and verification, since you can examine all relevant data as the test proceeds by adding a repeat count to the command. The differences between the TRACE data and that presented in the event reports are as follows:

(1) No record is saved in memory. The relay simply formats and sends data to the serial port about once every second. For permanent test records, capture data with a computer or serial printer connected to the serial port.

(2) Voltage and current samples are magnitude only, unlike those in event reports, which also retain phase information. Voltage and current values appear in primary units.

(3) Voltage and current samples are processed to remove dc offsets. Event reports show samples which have not been filtered to remove dc offsets.

(4) The time relationship between consecutive rows of the TRACE output is approximately one second, but is not precise. There is an approximate one second lag between TRACE data acquisition and presentation as well as a fraction of a second between analog and non-analog data acquisition.

```
=>TRACE 6 <ENTER>

Example 500 kV Breaker                          Date: 6/1/92                Time: 14:16:08

                Amps and Kvolts Prim

          Currents              Voltages            Relay Word      Outs     Ins
                                                                    8AAAAAA  TTT5MC
                                                                    612345L  PPP2OL
     IA      IB      IC      VA      VB      VC     R1 R2 R3 R4 R5  T        ABCAD

      0       0       0     0.0     0.0     0.0     02 00 00 00 00  ..2....  ......
      0       0       0     0.0     0.0     0.0     02 00 00 00 00  ..2....  ......
      0       0       0     0.0     0.0     0.0     02 00 00 00 00  ..2....  ......
      0       0       0     0.0     0.0     0.0     02 00 00 00 00  ..2....  ......
      0       0       0     0.0     0.0     0.0     02 00 00 00 00  ..2....  ......
      0       0       0     0.0     0.0     0.0     02 00 00 00 00  ..2....  ......

=>
```

TRIGGER

TRIGGER generates an event record. After command entry, the relay responds "Triggered," and displays the record summary.

```
=>TRIGGER <ENTER>
Triggered

=>

Example 500 kV Breaker                          Date: 6/1/92                Time: 10:16:04

Type: INT      Energy (MJ):   0.00
```

Use the EVENT command to view event records generated by the TRIGGER command.

Access Level 2 Commands

While all commands are available from Access Level 2, the following commands are available only in Access Level 2. Remember: the ALARM relay pulses closed for one second after any Level 2 access attempt.

LOGIC n

The LOGIC command programs the masks which control outputs and event report triggering.

```
=>>LOGIC n <ENTER>
```

The parameter n specifies a mask to program.

n	Mask
M86T -	Mask for trip
MA1 -	Mask for A1 relay control
MA2 -	Mask for A2 relay control
MA3 -	Mask for A3 relay control
MA4 -	Mask for A4 relay control
MA5 -	Mask for A5 relay control
MER -	Mask for event report triggering

The logic programming procedure requires you to enter changes to the mask or press **<ENTER>** to indicate no change. Each mask listed above is split into sections which correspond to the five rows of the Relay Word as follows:

RELAY WORD

Row 1	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF
Row 2	FOBF	FOPF	59FO	59H	ALRM	TC	TB	TA
Row 3	PDBF	PDPF	87UA	87UB	87UC	86RS	MDT	CTF
Row 4	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB
Row 5	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q

The MER mask has two additional rows, one for input contacts and one for output contacts, as follows:

Row 6	*	86BF	A1	A2	A3	A4	A5	ALARM
Row 7	*	*	CLOS	MOD	52A	TPC	TPB	TPA

Note: Even though ALARM is shown in Row 6, you cannot use ALARM Output Contact Closure to trigger an event report.

The LOGIC command displays a header and settings for each row of the Relay Word. Next it displays a question mark prompt and waits for input. Enter only ones and zeros with no separating spaces as input; one selects and zero deselects a member of the Relay Word. Press **<ENTER>** when a group is satisfactory. If you wish to change any member of a group, you must re-enter all eight members, even if some remain the same. The relay repeats logic settings and the question mark prompt after entry of each row to allow corrections.

When you complete data entry for a row, the relay displays the new settings and prompts for approval to enable the relay with them. **Y <ENTER>** enters the new data, pulses the ALARM contact closed momentarily, and clears the event buffers. **N <ENTER>** retains the old settings.

LOGIC command example for the M86T mask:

```
=>>LOGIC M86T <ENTER>

1 selects, 0 deselects.

FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF

 1    1    0    0    0    0    0    1
?<ENTER>
FOBF FOPF 59FO 59H  ALRM TC   TB   TA

 1    0    0    0    0    0    0    0
?<ENTER>
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF

 0    1    0    0    0    0    0    1
?10000000<ENTER>
 1    0    0    0    0    0    0    0
?<ENTER>
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB

 0    0    0    0    0    0    0    0
?<ENTER>
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q

 0    0    0    0    0    0    0    0
?<ENTER>

New M86T:
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF

 1    1    0    0    0    0    0    1
FOBF FOPF 59FO 59H  ALRM TC   TB   TA

 1    0    0    0    0    0    0    0
PDBF PDPF 87UA 87UB 87UC 86RS MTD  CTF

 1    0    0    0    0    0    0    0
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB

 0    0    0    0    0    0    0    0
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q

 0    0    0    0    0    0    0    0

OK (Y/N) ? Y <ENTER>
Enabled

Example 500 kV Breaker                          Date: 6/1/92              Time: 14:13:36

=>>
```

OUT n

OUT verifies that all output relays are functional. You can close each of the output relays 86BF TRIP, A1 through A5, and ALARM on command. The test also verifies that communications circuits are operating correctly.

To test the 86BF TRIP, type **OUT T <ENTER>**. The relay prompts: Close 86BF TRIP output relay (Y/N)? Reply **Y <ENTER>** to continue, or the test aborts. The relay closes the 86BF TRIP output and prompts: 86BF TRIP output relay now closed. Hit <ENTER> to end test? As soon as you press **<ENTER>**, the test ends and relay outputs revert to normal operating states. Jumper JMP104 protects this test feature; the test aborts unless Jumper JMP104 is in place on the main board.

During command entry, you can abbreviate output relay selections. Shortened versions of the OUT command are:

OUT T for the 86BF TRIP Output
OUT 1 for the A1 Programmable Output
OUT 2 for the A2 Programmable Output
OUT 3 for the A3 Programmable Output
OUT 4 for the A4 Programmable Output
OUT 5 for the A5 Programmable Output
OUT A for the ALARM relay

PASSWORD (1 or 2) password

PASSWORD allows you to inspect or change existing passwords. To inspect passwords, type **PASSWORD <ENTER>** as the following example shows:

```
=>>PASSWORD <ENTER>
1: OTTER
2: TAIL
=>>
```

To change the password for Access Level 1 to BIKE enter the following:

```
=>>PASSWORD 1 BIKE <ENTER>
1:BIKE
2:TAIL
=>>
```

The relay sets the password, pulses the ALARM relay closed, and displays the new passwords.

After entering new passwords, inspect them carefully. Make sure they are what you intended and record them.

Passwords can be any length up to six numbers, letters, or any other printable characters except delimiters (space, comma, semicolon, colon, slash). Upper and lower case letters are considered different characters. Examples of valid, distinct passwords include:

OTTER otter Ot3456 +TAIL+ !@#$%^ 123456 12345. 12345 ab1CDE

If the passwords are lost or you wish to operate the SEL-2BFR Relay without password protection, install JMP103 on the main board. With no password protection, you can gain access without the passwords and view or change existing passwords.

SET n

SET allows entry of relay settings. At the setting procedure prompts, enter new data or press **<ENTER>** to indicate no change. You can jump to a specific setting by entering the setting name as parameter n. If no setting is entered as an argument, the procedure initiates at the first setting, Relay ID.

The relay checks new settings against established limits twice. The first check ensures that settings fall within secondary setting limits shown in *Section 2: Specifications*. The relay also compares certain settings to ensure proper relationships.

The SET command prompts you for each setting. If the setting is within primary setting range, the relay prompts you for the next setting. Press **<ENTER>** to retain an existing setting.

When you finish entering setting changes, it is not necessary to scroll through the remaining settings. Type **END <ENTER>** after your last change to display the new settings and enable prompt. Do not use the END statement at the Relay ID setting; use **<CTRL>X** to abort the SET procedure from this point.

After you enter all data, the relay displays the new settings and prompts for approval to enable them. Answer **Y <ENTER>** to approve the new settings. Error messages notify you when entries result in out-of-range settings. If all settings are acceptable, the relay enables them, closes the ALARM contact momentarily, and clears the event buffer.

Setting ranges appear to the right of each numerical entry. Setting limits and units appear in brackets. The relay does not display these ranges during the actual set procedure.

ID	39 character string to identify relay in event reports.
Schm	Select Failure to Trip Fault Current scheme (1 - 6)
50FT	Fault detecting overcurrent element (0.50 - 45 secondary amperes)
Ttpu	62TT timer time delay pickup (0.25 - 63.75 cycles)
Ttdo	62TT timer time delay dropout (0.25 - 63.75 cycles)
62FC	62FC timer time delay pickup (0.25 - 63.75 cycles)
50LD	Load detecting overcurrent element (0.10 - 45 secondary amperes)
62LD	62LD timer time delay pickup (0.25 - 63.75 cycles)
62LP	62LP timer time delay pickup (0.25 - 63.75 cycles)
62AP	Breaker auxiliary pending failure delay (0.25 - 63.75 cycles)
62AF	Breaker auxiliary failure delay (0.25 - 63.75 cycles)
E62A	Enable breaker auxiliary failure logic? (Y, N, 1, 2)
DRTE	Enable time delayed retrip? (Y, N)
RTSD	Retrip Seal-In delay (0.25 - 63.75 cycles) (SEL-2BFR-2)
RTTD	Retrip time delay (0.25 - 63.75 cycles)

37OP	Phase overpower element for resistor thermal protection (0.1 - 3400 watts sec)
26CF	CLOSE resistor thermal failure threshold (0.01 - 1000 secondary joules)
26CP	Pending failure thermal limit (0.01 - 1000 secondary joules)
26TF	TRIP resistor thermal failure threshold (0.01 - 1000 secondary joules)
26TP	Pending failure thermal failure threshold (0.01 - 1000 secondary joules)
47Q	Negative-sequence overvoltage element detects blown potential fuses (2 - 170 secondary volts)
62OP	62OP timer time delay pickup (0.25 - 63.75 cycles)
CRTC	CLOSE resistor cooling time-constant (1 - 1140 minutes)
TRTC	TRIP resistor cooling time-constant (1 - 1140 minutes)
59FO	Pole flashover voltage (1 - 67 secondary volts)
62FF	62FF timer time delay pickup (0.25 - 63.75 cycles)
62FP	62FP timer time delay pickup (0.25 - 63.75 cycles)
87UB	Phase current unbalance ratio for phase discordance logic (8, 16, 32, 64)
62UC	62UC timer time delay pickup (0.25 - 63.75 cycles)
62UF	62U2 timer time delay pickup (0.25 - 16383.75 cycles)
62UP	62UP timer time delay pickup (0.25 - 16383.75 cycles)
50MD	MOD TRIP overcurrent element (0.10 - 45 secondary amperes)
62M1	Set the 62M1 timer time delay pickup (0.25 - 16200 cycles)
62M2	62M2 timer time delay pickup (0.25 - 16383.75 cycles)
ModTrip	Do you want to enable MOD TRIP logic? (Y, N)
CTR	Per unit Current Transformer Ratio (1 - 10,000)
PTR	Per unit Potential Transformer Ratio (1 - 10,000)
Topen	SLOW TRIP alarm timer (0.25 - 63.75 cycles)
Tclose	SLOW CLOSE alarm timer (0.25 - 63.75 cycles)
Vwarn	Voltage across closed circuit breaker for ALRM (0.5 - 7.5 secondary volts)
TIME1	Timeout for PORT 1 communications (0 - 30 minutes, 0 = No timeout)
TIME2	Timeout for PORT 2 communications (0 - 30 minutes, 0 = No timeout)
AUTO	Destination for automatic messages (1 = PORT 1, 2 = PORT 2, 3 = both ports)
RINGS	Number of rings after which modem on PORT 1 answers (1 - 30 rings)

The Vwarn, Topen, and Tclose settings expand the breaker monitoring abilities of the SEL-2BFR Relay. The function of each is explained below:

Vwarn: The Vwarn element provides a sensitive measurement of voltage across the closed circuit breaker contacts. This element is set below the 59FO element, and is only active when the circuit breaker is closed. If measured voltage exceeds the setting while the circuit breaker is closed, the relay asserts the ALRM bit in the Relay Word for one second and records the following message in the ALRM HISTORY: "WARNING: VOLTS ACROSS CLOSED CB." You can view the ALRM History with the STATUS command.

Topen: Topen allows you to specify a nominal clearing time for the protected circuit breaker. If the circuit breaker clearing exceeds this setting, the relay asserts the ALRM bit in the Relay Word for one second and records the following message in the ALRM History: "WARNING: SLOW TRIP." Clearing time is the dropout time measured for 50LD.

Tclose: Tclose allows you to specify a nominal circuit breaker close time which is alarmed and recorded as for the Topen setting. The relay measures close time as the time to pick up the 50LD elements.

The AUTO setting selects PORT 1, PORT 2, or both serial ports for automatically transmitted messages. Event summaries and self-test warning and failure reports are automatically transmitted from port(s) designated automatic regardless of access level if the designated port is not timed out. Enter zero as the timeout setting of the appropriate port if automatic transmissions will be monitored by a dedicated channel or printed on a dedicated printer. The table below shows the effect of each possible setting:

Auto Setting	Automatic Message Destination Port
1	1
2	2
3	1 and 2

SEL-2BFR, -2/BFR COMMAND SUMMARY

Level 0

ACCESS	Answer with password (if password protection is enabled) to gain access to Level 1. Third unsuccessful attempt pulses ALARM relay.

Level 1

2ACCESS	Answer with password (if password protection enabled) to gain access to Level 2. This command always pulses the ALARM relay.
DATE m/d/y	Without arguments, relay displays date; **DATE 6/15/91 <ENTER>** sets the date to June 15, 1991. IRIG-B synchronization overrides month and day settings.
EVENT n l	Shows record for event number n, l signifies long version: **EVENT 1 l <ENTER>** shows the long form of the latest event. **EVENT 100 <ENTER>** shows the short form of the oldest event.
HEAT n	Shows internal energy of 3 close and 3 open resistors n times.
HISTORY	Shows DATE, TIME, TYPE, ENERGY, IV-TIME, and 52A-TIME for the 100 most recent events.
IRIG	Forces immediate execution of IRIG-B time code synchronization.
METER n	Shows primary current, voltage, real and reactive power n times. METER runs once; METER n runs n times (n = 1 to 255).
QUIT	Returns to Access Level 0.
SHOWSET	Displays settings without affecting them.
STATUS	Shows self-test status and ALARM history.
TARGET n	Shows data and set target lights as follows: TAR 0: Relay Targets — TAR 1: Relay Word Row 1 TAR 2: Relay Word Row 2 — TAR 3: Relay Word Row 3 TAR 4: Relay Word Row 4 — TAR 5: Relay Word Row 5 TAR 6: Relay Outputs — TAR 7: Relay Inputs TAR R: Clear Targets and return to TAR 0.
TIME h/m/s	Shows or sets time. TIME 13/32/00 sets clock to 1:32:00 PM. IRIG-B synchronization overrides this setting.
TRACE n	Traces voltage and current inputs, Relay Word bits, relay inputs and outputs n times.
TRIGGER	Triggers event report generation (event type is INT).

Level 2

LOGIC n	Shows or sets logic masks M86T, MA1, MA2, MA3, MA4, MA5. Command pulses ALARM contact closed and clears event buffers when new settings are stored.
OUT n	Closes designated output contacts if jumper JMP104 is in place (n = T, 1, 2, 3, 4, 5, or A).
PASSWORD	Shows or changes passwords: **PASSWORD 1 OTTER <ENTER>** changes Level 1 password to OTTER. **PASSWORD 2 TAIL <ENTER>** changes Level 2 password to TAIL.
SET n	Initiates setting procedure. Optional n directs relay to begin procedure at that setting. SET 50LD starts procedure at 50LD setting. SET initiates procedure at beginning. ALARM relay closes while relay computes new settings and clears long event data.

Use space, comma, semicolon, or slash to separate commands and parameters from one another. Only the first three letters of commands are significant.

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EVENT REPORTING

EVENT REPORT GENERATION

The relay generates a summary and long event report in response to the actions listed in Table 4.1. The summary event report allows a quick review of the information necessary to determine the type of relay or breaker operation. The long event report displays fifteen cycles of information for analyzing system and scheme performance.

Table 4.1: Event Report Triggering Actions

- Assertion of the 86BF TRIP output
- TRIGGER command execution
- Assertion of any element set in the MER (Mask for Event Report Trigger) logic mask

The relay generates an event report each time it asserts the 86BF Trip output, even if other event report triggering elements have already asserted. The relay triggers a second report for the same event if the trip occurs after the first report ends. Thus the relay records the beginning and end of each event for which it trips. A second event report is not provided if the TRIP output first asserts at or less than thirteen cycles after the first report is triggered.

Relay elements set in the MER mask trigger the event report generator in a level sensitive manner. The relay does not generate multiple event reports when additional relay elements pick up. Only the first relay element of any continuous sequence triggers an event report.

Triggering is recorded to the nearest quarter-cycle (4.17 ms) and referenced to the 8th row of data in the report. All reports trigger at row 8. This system allows you to determine the total duration of a long event which triggers two event reports. Simply calculate the time difference between the report generated at event inception and the report generated by assertion of the 86BF TRIP output.

SUMMARY EVENT REPORT

The relay automatically transmits summary reports from port(s) designated AUTOMATIC regardless of access level, as long as the designated port has not timed out. If automatic transmissions are monitored by a dedicated channel or printed on a dedicated printer, enter zero for the timeout setting of the appropriate port.

Due to the length of the full report, it is not automatically transmitted. You can display the full report with the EVENT command.

The summary event report includes:

- Relay terminal identifier
- Date and time of the event
- Event type
- Mechanical operating time of the breaker
- Electrical operating time of the breaker
- Three-pole energy dissipated in the breaker during the first fourteen cycles of the event report

The following shows an example summary event report:

```
Example 500 kV Breaker                         Date: 6/1/92          Time: 09:45:27.729

Type: TRIP3   52A (cyc):  2.50   IV-Time (cyc):  2.50   Energy (MJ):  14.21

=>>
```

The contents of the summary event report are described below.

TYPE: The relay determines event type by tracking the 86BF TRIP output state and the inputs asserted during the event. Ten event types are recognized:

Event "Type" Classification	**Meaning**
86BFT	86BF TRIP output asserted
TRIPA	A-phase TRIP input asserted
TRIPB	B-phase TRIP input asserted
TRIPC	C-phase TRIP input asserted
TRIPAB	A-phase and B-phase TRIP inputs asserted
TRIPBC	B-phase and C-phase TRIP inputs asserted
TRIPCA	C-phase and A-phase TRIP inputs asserted
TRIP3	A-, B- and C-phase TRIP inputs asserted
CLOSE	CLOSE input asserted
INT	Any recorded event not containing a TRIP or CLOSE input assertion

Internally-triggered events can be triggered manually with the TRIGGER command or by assertion of an element set in the MER logic mask.

86BF TRIP output contact closure always generates an event report.

52A: The mechanical operating time of the circuit breaker in cycles, shown in quarter-cycle steps.

For trips, the time measured from the instant any TRIP input asserts to the time the 52A input deasserts.

For closes, the time measured from the instant the CLOSE input asserts to the time the 52A input asserts.

IV-TIME: The electrical operating time of the circuit breaker.

For trips, the time measured from the instant a TRIP input asserts to the instant the 50LD overcurrent element drops out.

For closes, the time measured from the instant the CLOSE input asserts to the instant the 59FO overvoltage element drops out, or until the 50LD overcurrent element picks up (whichever is less).

ENERGY: The three-pole energy dissipated in the breaker spanning the first fourteen cycles of each event report is computed.

For breaker operations, this is the total energy dissipated in the resistors and interrupters.

TIME TAG: When the reported event occurs, the relay saves the date and time.

The SEL-2BFR Relay stores the 100 latest event summaries in nonvolatile memory. The relay retains these summaries through losses of control power and setting changes. Use the HISTORY command to view the summary reports.

LONG EVENT REPORT

The long event report contains 60 quarter-cycles of pre-fault, fault, and post-fault voltage and current information. For each quarter-cycle of voltage and current information, the relay also records the states of all Relay Word elements, outputs, and inputs. This information is useful in reviewing event inception and duration, relay element response, and breaker reaction time.

The nine latest event records are stored in volatile memory. You can review the stored summary reports quickly with the HISTORY command; use the EVENT command to display the long form of each event report.

INTERPRETATION OF CURRENT AND VOLTAGE DATA

The relay receives secondary quantities via the rear panel, completes the processes listed below, and retains the data for event reporting. The event reports display current and voltage samples in secondary units.

1. Input analog signals are filtered by two-pole, low pass filters.
2. Filtered analog signals are sampled four times per power system cycle and converted to numerical values.
3. With respect to the present sample, the previous sample was taken one quarter-cycle earlier and appears to be leading the present sample by 90°.

Event report values can be used to represent the signals as phasors:

The previous value of the output is the Y-component.
The present value of the output is the X-component.

It may seem confusing to refer to the older data as the leading component of the phasor. The following example may help.

Consider a sine wave having zero phase shift with respect to t=0 and a peak amplitude of 1. Now consider two samples, one taken at t=0, the other taken 90° later. They have values 0 and 1, respectively. By the above rules, the phasor components are (X,Y) = (1,0).

Now consider a cosine function. Its samples taken at t=0 and t+90° are 1 and 0; its phasor representation is (0,1). The phasor (0,1) leads the phasor (1,0) by 90°. This coincides with a 90° lead of the cosine function over the sine function.

To construct a phasor diagram of voltages and currents, select a pair of adjacent rows from an area of interest in the event report. On Cartesian coordinates, plot the lower row (newer data) as the X-components and the upper row (older data) as the Y-components. Rotate the completed diagram to any angle of reference. The magnitude of any phasor equals the square root of the sum of its squares.

Note that moving forward one quarter-cycle rotates all phasors 90°. You can verify this by plotting the phasor diagram with rows 1 and 2, then rows 2 and 3 of an event report.

Current and voltage samples displayed in the even reports have not been digitally filtered. Small dc offsets may produce non-zero sample values when no ac signal is applied. These small offsets do not affect the breaker protection function.

To construct a phasor diagram of voltages or currents, select a pair of adjacent rows from an area of interest in the event report. On Cartesian coordinates, plot the lower row (newer data) as the P-components and the upper row (older data) as the Q-components. Rotate the completed diagram to any angle of reference. The magnitude of any phasor equals the square root of the sum of its components' squares.

Note that moving forward one quarter-cycle rotates all phasors 90°. You can verify this by plotting the phasor diagram with rows 1 and 2, then rows 2 and 3 of an event report.

For example, two consecutive filter outputs of a voltage channel could be:

Row Q: 65.98 volts
Row P: 11.63 volts

Convert these to polar form (magnitude and angle):

$$|V| = \text{sqrt}(P^2 + Q^2)$$
$$/V = \text{arg}(Q/P)$$

$$|V| = 67 \text{ volts rms}$$
$$/V = 80°$$

CONNECTION CHECK

The following procedure provides a quick method of checking the current connection polarity with event report data. Consider Figure 4.1, below.

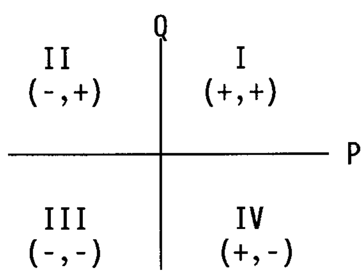

Figure 4.1: Coefficients of the Rectangular Coordinates of Phasors in Each Quadrant

If a phasor is expressed in rectangular coordinate format (P,Q), you can determine the phasor quadrant from the signs of the rectangular coordinates which represent it. For example, a phasor whose rectangular coordinates (P,Q) are both positive lies in quadrant I. A phasor with rectangular coordinate signs (+,-) lies in quadrant IV.

This fact may help you check the polarity and sequence of current connections to the relay.

1. With currents connected to the relay, type **TRIGGER <ENTER>** to execute the trigger command.

2. Type **EVENT 1 L<ENTER>** to view the event report generated. Press **<CTRL>S** to stop the event report before the first two rows of data scroll off the screen.

3. Using the first two rows of the event report (Row 1 = Q, Row 2 = P), determine the quadrant of the A-phase current using the signs of the P and Q samples.

4. Take note of the A-phase current quadrant, then determine the quadrants of the B- and C-phase currents. No two phase currents should lie in the same quadrant. You can also use this information to check phase rotation.

EVENT REPORT HEADER

The event report begins with a descriptor of the relay which generated it. In the sample event reports, the descriptor includes the relay identification string "Example 500 kV Breaker," the date and time the event was triggered, the Firmware Identification string, and headers for each of the data columns.

You can change the header with the SET command.

RELAY CURRENTS AND VOLTAGES

The data for each quarter-cycle appears under the relay descriptor, date, and time. Each row presents data one quarter-cycle later than the row above it; each column presents data from a given input, output, or Relay Word element.

The first three columns on the left side contain the line-to-neutral currents for each of the three phases: A, B, and C. These are scaled to secondary amperes.

The next three columns show the phase voltages across the breaker in the same order as the currents, scaled to secondary volts.

RELAY WORD

The state of each element in the Relay Word is shown in hexadecimal representation in the five columns marked R1 through R5. Each eight bit Relay Word row is converted to a two digit hexadecimal number and reported in the event report each quarter-cycle. You can decode the two digit hexadecimal number into an eight digit binary number using the table included in the SHOWSET command in *Section 3: Communications*. Because every Relay Word bit is shown each quarter-cycle, it is simple to determine the sequence of events recorded in the event report.

OUTPUT CONTACTS

The relay records the states of the contact outputs in the column labelled "Outs." The following table summarizes column headings and contents. When outputs are asserted, these columns list the corresponding descriptors. For example, if one row of the "Outs" columns contains "...3...," A3 is the only output contact asserted.

Outs Column Headings	Descriptor	Contents
86TP	T	86BF TRIP Output
A1	1	A1 Programmable Output
A2	2	A2 Programmable Output
A3	3	A3 Programmable Output
A4	4	A4 Programmable Output
A5	5	A5 Programmable Output
AL	A	ALARM Output

INPUT CONTACTS

The group of columns labeled "Ins" displays the state of each contact input, listing a descriptor in the appropriate column when the associated input asserts. "Ins" column headings and contents appear in the following table. For example, if one row of the "Ins" columns reads "TTT5..," the three trip inputs are asserted and breaker 52A contact is still closed.

Ins Column Headings	Descriptor	Contents
TPA	T	A-PHASE TRIP input
TPB	T	B-PHASE TRIP input
TPC	T	C-PHASE TRIP input
52A	5	52A STATUS input
MOD	M	MOD STATUS input
CL	C	CLOSE input

EVENT SUMMARY

After presenting fifteen cycles of data, the relay lists a one-row summary of event data. The information presented here is identical to the information included in the summary event report automatically generated following the event. A description of this summary appears at the beginning of this section.

SETTINGS DISPLAY

The final data in the event report show the current relay settings. These appear in the same format as the SHOWSET command. All event reports include this information for reference purposes.

FIRMWARE IDENTIFICATION

The SEL-2BFR Relay event report includes a Firmware Identification Data (FID) string below the Relay ID string in each event report. The FID data describes the firmware installed in the relay when the event report was triggered. The string format is as follows:

FID = [PN] - R[RN] - V[VS] - D[RD],

Where:

[PN] = Product Name

[RN] = Revision Number

[VS] = Version Specifications

[RD] = Release Date

Please contact the factory for information concerning available versions of the SEL-2BFR Relay. Version specifications are not intended for ordering purposes but as an identification of the software installed in a relay.

EXAMPLE EVENT REPORTS

Introduction

This section contains four example event reports generated by the SEL-2BFR Relay in response to three simulated breaker failure events. The four reports represent an example of a successful instantaneous breaker retrip, a B-phase breaker failure to trip fault current during a three-phase fault, and a trip resistor thermal failure.

The event reports use a sequence of event format which allows performance analysis of the system by quarter-cycles. Through this analysis, you can observe pre-fault voltage across the breaker and current through the breaker, determine whether or not the breaker was closed using the 52A Inputs column and line current magnitudes, and learn when elements asserted by examining the Relay Word columns.

Example 1: Successful Instantaneous Retrip

Fault Description

The SEL-2BFR Relay generated this event report in response to a three-phase trip input. The event report shows the instantaneous retrip of the protected breaker and the successful clearing of the three-phase fault. The full event report is shown below followed by the row by row analysis.

In this example, relay logic mask MA1 was set with the TA, TB, and TC Relay Word bits. Thus, the output contact asserts whenever TRIPA, TRIPB, or TRIPC is asserted. The A1 programmable output contact can be connected to operate breaker trip coil #2. This design, including the dc connections and logic mask settings, realizes the instantaneous retrip function and is shown in ***Section 5: Applications***.

Example Event Report 1: Successful Instantaneous Retrip of the Protected Breaker

Example 500 kV Breaker   Date: 6/1/92   Time: 09:17:54.454
FID=SEL-BFR-R105-V1-D910212

Amps and Volts Sec

Currents			Voltages			Relay Word					Outs	Ins
											8AAAAAA	TTT5MC
											612345L	PPP2OL
IA	IB	IC	VA	VB	VC	R1	R2	R3	R4	R5	T	ABCAD
0.81	-0.94	0.00	-0.08	0.00	0.00	0C	00	00	00	00	....	...5M.
0.47	0.41	-1.00	0.00	0.00	0.00	0C	00	00	00	00	....	...5M.
-0.91	0.81	-0.03	0.00	0.00	0.00	0C	00	00	00	00	....	...5M.
-0.56	-0.56	1.00	-0.08	-0.08	0.00	0C	00	00	00	00	....	...5M.
0.81	-0.94	0.00	-0.08	0.00	0.00	0C	00	00	00	00	....	...5M.
0.47	0.44	-1.00	0.00	0.00	0.00	0C	00	00	00	00	....	...5M.
4.19	4.66	-9.01	0.00	0.00	0.00	0C	00	00	00	00	....	...5M.
-8.67	7.04	1.50	-0.08	-0.08	0.00	1C	07	00	00	00	.1.....	TTT5M.
-3.28	-5.79	8.95	-0.08	0.00	0.00	1C	07	00	00	00	.1.....	TTT5M.
8.45	-7.13	-1.44	0.00	0.00	-0.08	1C	07	00	00	00	.1.....	TTT5M.
3.22	5.57	-8.92	0.00	0.00	0.00	1C	07	00	00	00	.1.....	TTT5M.
-8.54	6.91	1.47	-0.08	-0.08	0.00	1C	07	00	00	00	.1.....	TTT5M.
-3.32	-5.76	8.95	-0.08	0.00	0.00	1C	07	00	00	00	.1.....	TTT5M.
8.45	-7.13	-1.44	0.00	0.00	0.00	1C	07	00	00	00	.1.....	TTT5M.
-1.13	0.78	0.22	-54.81	65.49	-10.59	1C	27	00	00	01	.1.....	TTT5M.
0.06	-0.16	-0.03	-36.12	-34.04	70.49	0C	27	00	00	01	.1.....	TTT5M.
-0.09	-0.03	0.00	59.98	-61.32	1.17	0C	27	00	00	01	.1.....	TTT5M.
-0.06	-0.06	0.00	36.54	33.20	-69.66	0C	3F	00	00	00	.1.....	TTT5M.
-0.06	-0.06	0.00	-59.31	61.23	-1.75	04	3F	00	00	00	.1.....	TTT.M.
-0.06	-0.06	0.00	-35.71	-33.54	69.49	02	3F	00	00	00	.12....	TTT.M.
-0.03	-0.06	0.00	59.98	-61.40	1.25	02	3F	00	00	00	.12....	TTT.M.
-0.06	-0.06	0.00	36.54	33.20	-69.74	02	3F	00	00	00	.12....	TTT.M.
-0.06	-0.06	0.00	-59.31	61.23	-1.67	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.54	69.49	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	59.98	-61.32	1.25	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	36.46	33.29	-69.74	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-59.31	61.23	-1.67	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.54	69.49	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	59.98	-61.32	1.25	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	36.46	33.29	-69.74	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-59.40	61.23	-1.59	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.54	69.49	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	59.98	-61.32	1.17	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	36.46	33.29	-69.74	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-59.40	61.23	-1.59	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.62	69.49	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	59.98	-61.32	1.17	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	36.46	33.37	-69.74	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-59.40	61.15	-1.59	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.62	69.49	02	38	00	00	00	..2....	....M.
-0.03	-0.06	0.00	59.98	-61.32	1.17	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	36.37	33.37	-69.74	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-59.40	61.15	-1.50	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.62	69.49	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	59.98	-61.32	1.17	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	36.37	33.37	-69.74	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-59.40	61.15	-1.50	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.62	69.49	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	59.98	-61.23	1.17	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	36.37	33.37	-69.74	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-59.48	61.15	-1.50	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.62	69.49	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	59.98	-61.23	1.08	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	36.29	33.45	-69.74	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-59.48	61.15	-1.42	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.70	69.49	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	59.98	-61.23	1.08	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	36.29	33.45	-69.74	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-59.48	61.15	-1.42	02	38	00	00	00	..2....	....M.
-0.06	-0.06	0.00	-35.71	-33.70	69.49	02	38	00	00	00	..2....	....M.

Example Event Report 1 (continued)

```
Type: TRIP3   52A (cyc):  2.75   IV-Time (cyc):  2.75   Energy (MJ):  14.31

Schm = 2        50FT  = 8.60     TTpu  = 6.00     TTdo   = 2.00    62FC = 4.00
50LD = 0.52     62LD  = 5.50     62LP  = 3.25
62AP = 5.25     62AF  = 7.50     E62A  = N        DRTE   = N       RTTD = 2.00
37OP = 2.25     26CF  = 1.45     26CP  = 1.09     26TF   = 4.56    26TP = 3.42
47Q  = 18.70    62OP  = 3.00     CRTC  = 80       TRTC   = 80
59FO = 4.01     62FF  = 30.00    62FP  = 25.00
87UB = 16       62UC  = 12.00    62UF  = 60.00    62UP   = 50.00
50MD = 0.10     62M1  = 600.00   62M2  = 600.00   ModTrip= Y
CTR  = 600      PTR   = 4300
Topen= 2.25     Tclose= 10.25    Vwarn = 0.47
TIME1= 5        TIME2 = 0        AUTO  = 2        RINGS  = 3

Logic settings:
M86T  MA1  MA2  MA3  MA4  MA5  MER
 C1   00   02   00   20   00   20
 80   07   00   00   40   00   48
 81   00   00   02   40   04   42
 00   00   00   00   55   00   55
 00   00   00   00   50   00   5F
 --   --   --   --   --   --   00
 --   --   --   --   --   --   07
```

Note: The SEL-2BFR-2 Relay includes the RTSD setting (not shown).

Prefault Data

The following is the first four cycles (quarter-cycles 1 - 16) of Event Report 2, showing prefault and event triggering conditions.

```
                Amps and Volts Sec

          Currents              Voltages           Relay Word       Outs     Ins
                                                                  8AAAAAA  TTT5MC
                                                                  612345L  PPP2OL
    IA      IB      IC      VA      VB      VC   R1 R2 R3 R4 R5   T        ABCAD     Quarter-Cycle

  0.81   -0.94    0.00   -0.08    0.00    0.00   0C 00 00 00 00   .......  ...5M.          1
  0.47    0.41   -1.00    0.00    0.00    0.00   0C 00 00 00 00   .......  ...5M.          2
 -0.91    0.81   -0.03    0.00    0.00    0.00   0C 00 00 00 00   .......  ...5M.          3
 -0.56   -0.56    1.00   -0.08   -0.08    0.00   0C 00 00 00 00   .......  ...5M.          4

  0.81   -0.94    0.00   -0.08    0.00    0.00   0C 00 00 00 00   .......  ...5M.          5
  0.47    0.44   -1.00    0.00    0.00    0.00   0C 00 00 00 00   .......  ...5M.          6
  4.19    4.66   -9.01    0.00    0.00    0.00   0C 00 00 00 00   .......  ...5M.          7
 -8.67    7.04    1.50   -0.08   -0.08    0.00   1C 07 00 00 00   .1.....  TTT5M.          8

 -3.28   -5.79    8.95   -0.08    0.00    0.00   1C 07 00 00 00   .1.....  TTT5M.          9
  8.45   -7.13   -1.44    0.00    0.00   -0.08   1C 07 00 00 00   .1.....  TTT5M.         10
  3.22    5.57   -8.92    0.00    0.00    0.00   1C 07 00 00 00   .1.....  TTT5M.         11
 -8.54    6.91    1.47   -0.08   -0.08    0.00   1C 07 00 00 00   .1.....  TTT5M.         12

 -3.32   -5.76    8.95   -0.08    0.00    0.00   1C 07 00 00 00   .1.....  TTT5M.         13
  8.45   -7.13   -1.44    0.00    0.00    0.00   1C 07 00 00 00   .1.....  TTT5M.         14
 -1.13    0.78    0.22  -54.81   65.49  -10.59   1C 27 00 00 01   .1.....  TTT5M.         15
  0.06   -0.16   -0.03  -36.12  -34.04   70.49   0C 27 00 00 01   .1.....  TTT5M.         16
```

The following outline lists observed incidents shown in Example Event Report 1 by quarter-cycle.

Quarter Cycle	Event Report Shows:
1-7	Prefault conditions: • Balanced load currents and no voltage measured across the breaker. • Hexadecimal 0C in Relay Word row 1 indicates pickup of 50LD and 50MD. • 5 in 52A Input column verifies breaker closure (as does load current flow). • M in MOD Input column verifies MOD closure.

8-14 Fault Inception:

- Hexadecimal 1C in Relay Word row 1 indicates that 50FT, 50LD, and 50MD elements are picked up in at least one phase.
- Ts in TPA, TPB, and TPC columns indicate assertion of all three trip inputs. Hexadecimal 07 in Relay Word row 2 also confirms trip input assertion.
- 1 in Output A1 column indicates that the A1 output contact has operated to retrip the protected breaker.

15 Breaker Operation

- Hexadecimal 27 in Relay Word row 2 indicates 59FO element pickup due to detection of voltage across the breaker. This shows that at least one breaker pole is opening.
- Hexadecimal 01 in Relay Word row 5 indicates 47Q element pickup.

16

- Hexadecimal 1C in Relay Word row 1 changes to 0C, indicating that 50FT has dropped out in all three phases. Current samples in columns Ia, Ib, and Ic are decreasing in magnitude.

Breaker Operation and Post-Fault Data

Event report rows 17 through 28 show the completion of the breaker opening sequence, dropout of the remaining current elements, and dropout of the trip inputs.

```
              Amps and Volts Sec

         Currents              Voltages            Relay Word      Outs     Ins
                                                                   8AAAAAA  TTT5MC
                                                                   612345L  PPP2OL
   IA      IB      IC      VA      VB      VC    R1 R2 R3 R4 R5   T        ABCAD              Quarter-Cycle

 -0.09  -0.03    0.00   59.98  -61.32    1.17    0C 27 00 00 01   .1.....  TTT5M.                  17
 -0.06  -0.06    0.00   36.54   33.20  -69.66    0C 3F 00 00 00   .1.....  TTT5M.                  18
 -0.06  -0.06    0.00  -59.31   61.23   -1.75    04 3F 00 00 00   .1.....  TTT.M.                  19
 -0.06  -0.06    0.00  -35.71  -33.54   69.49    02 3F 00 00 00   .12....  TTT.M.                  20

 -0.03  -0.06    0.00   59.98  -61.40    1.25    02 3F 00 00 00   .12....  TTT.M.                  21
 -0.06  -0.06    0.00   36.54   33.20  -69.74    02 3F 00 00 00   .12....  TTT.M.                  22
 -0.06  -0.06    0.00  -59.31   61.23   -1.67    02 38 00 00 00   ..2....  ....M.                  23
 -0.06  -0.06    0.00  -35.71  -33.54   69.49    02 38 00 00 00   ..2....  ....M.                  24

 -0.06  -0.06    0.00   59.98  -61.32    1.25    02 38 00 00 00   ..2....  ....M.                  25
 -0.06  -0.06    0.00   36.46   33.29  -69.74    02 38 00 00 00   ..2....  ....M.                  26
 -0.06  -0.06    0.00  -59.31   61.23   -1.67    02 38 00 00 00   ..2....  ....M.                  27
 -0.06  -0.06    0.00  -35.71  -33.54   69.49    02 38 00 00 00   ..2....  ....M.                  28
```

Quarter
Cycle Event Report Shows:

18

- Hexadecimal 3F in Relay Word row 2 indicates pickup of the 59FO and 59H overvoltage elements, ALRM breaker operation alarm, and the trip inputs. ALRM asserts due to pickup of the 59FO element while the 52A input is asserted.
- Hexadecimal 01 in Relay Word row 5 changes to 00, indicating 47Q element dropout.

19

- Hexadecimal 0C in Relay Word row 1 changes to 04, indicating 50LD element dropout.
- 5 in 52A inputs column changes to "." indicating deassertion of the 52A input. The breaker auxiliary contact has opened.

20-22 • Hexadecimal 04 in Relay Word row 1 changes to 02, indicating 50MD element dropout and 52BV bit assertion.
- 2 in A2 output column indicates that A2 operated. A2 is set to close for 52BV bit assertion.

23 • Hexadecimal 3F in Relay Word row 1 changes to 38, indicating TRIP input dropout (also shown by disappearance of Ts from the Trip inputs columns).

24-60 • Remainder of the event report shows voltage samples measured across the open breaker. 2 in the outputs column shows that the A2 output is closed for 52BV bit assertion. M in the inputs column shows that the MOD status input is asserted, indicating MOD auxiliary contact closure.

Event Summary

The event summary shows event type, mechanical and electrical operating times of the protected breaker, and energy interrupted by the breaker during the first fourteen cycles of the event, shown in megajoules.

Event type shown is TRIP3 because all three trip inputs were asserted during the event, but the 86BF TRIP output was not asserted.

Mechanical operating time of the breaker 52A equals 2.75 cycles. This is the amount of time from the first TRIP input assertion to 52A input deassertion.

Electrical operating time IV-Time equals 2.75 cycles. This is the time from the first trip input assertion to 50LD phase overcurrent element dropout in all three phases.

Energy is the three-phase energy interrupted by the breaker during the first fourteen quarter-cycles of the event report, scaled in megajoules, primary.

Example 2: Failure to Trip Fault Current

Fault Description

The relay generated this event report in response to a simulated failure of the protected breaker to trip B-phase fault current during a three-phase fault. A row by row analysis follows the full event report below.

Example Event Report 2: B-phase Breaker Failure

```
Example 500 kV Breaker                            Date: 6/1/92        Time: 09:55:26.050
FID=SEL-BFR-R105-V1-D910212

                 Amps and Volts Sec
            Currents                 Voltages             Relay Word         Outs      Ins
                                                                            8AAAAAA   TTT5MC
                                                                            612345L   PPP2OL
    IA       IB       IC       VA       VB       VC     R1 R2 R3 R4 R5      T         ABCAD

  -1.06    0.50     0.44     0.00     0.00     0.00     0C 00 00 00 00     .......   ...5M.
  -0.13   -0.88     0.91     0.00     0.00     0.00     0C 00 00 00 00     .......   ...5M.
   0.97   -0.63    -0.44     0.00     0.00     0.00     0C 00 00 00 00     .......   ...5M.
   2.72   -0.06    -2.78     0.00     0.00     0.00     0C 00 00 00 00     .......   ...5M.

  -0.16    7.66    -7.63     0.00     0.00     0.00     0C 00 00 00 00     .......   ...5M.
  -9.20    3.72     5.29     0.00     0.00     0.00     1C 00 00 00 00     .......   ...5M.
   0.81   -8.29     7.38     0.00     0.00     0.00     1C 00 00 00 00     .......   ...5M.
   9.01   -3.88    -5.22     0.00     0.00     0.00     1C 07 00 00 00     .......   TTT5M.

  -0.88    8.10    -7.32     0.00     0.00     0.00     1C 07 00 00 00     .......   TTT5M.
  -9.10    3.69     5.29     0.00     0.00     0.00     1C 07 00 00 00     .......   TTT5M.
   0.78   -8.29     7.41     0.00     0.00     0.00     1C 07 00 00 00     .......   TTT5M.
   6.35   -3.88    -3.07    -3.17     0.00   -16.10     1C 27 00 00 00     .......   TTT5M.

  -0.81    8.13     0.38   -68.07     0.00    23.61     1C 27 00 00 00     .......   TTT5M.
   0.03    3.69    -0.06    -5.42     0.00    63.49     1C 27 00 00 00     .......   TTT5M.
  -0.06   -8.29     0.03    69.83     0.00   -29.62     1C 27 00 00 01     .......   TTT5M.
  -0.06   -3.85     0.00     6.34     0.00   -63.23     1C 27 00 00 01     .......   TTT5M.

  -0.06    8.10     0.00   -69.24     0.00    29.28     1C 37 28 00 01     .......   TTT5M.
  -0.06    3.66     0.00    -5.34     0.00    62.90     1C 3F 28 00 01     .......   TTT5M.
  -0.06   -8.29     0.00    69.83     0.00   -29.62     1C 3F 28 00 01     .1.....   TTT5M.
  -0.06   -3.85     0.00     6.34     0.00   -63.15     1C 3F 28 00 01     .1.....   TTT5M.

  -0.06    8.13     0.00   -69.24     0.00    29.28     1C 3F 28 00 01     .1.....   TTT5M.
  -0.06    3.69     0.00    -5.42     0.00    62.90     3C 3F 28 00 01     .1..4..   TTT5M.
  -0.06   -8.29     0.00    69.83     0.00   -29.62     3C 3F 28 00 01     .1..4..   TTT5M.
  -0.06   -3.85     0.00     6.34     0.00   -63.15     BC 3F 28 00 01     T1..4..   TTT5M.

  -0.06    8.13     0.00   -69.24     0.00    29.28     BC 3F 28 00 01     T1..4..   TTT5M.
  -0.03    3.66     0.00    -5.42     0.00    62.90     BC 3F 28 00 01     T1..4..   TTT5M.
  -0.06   -8.29     0.00    69.83     0.00   -29.62     BC 3F 28 00 01     T1..4..   TTT5M.
  -0.06   -3.85     0.00     6.26     0.00   -63.15     BC 3F 28 00 01     T1..4..   TTT5M.

  -0.06    8.13     0.00   -69.24     0.08    29.36     BC 3F 28 00 01     T1..4..   TTT5M.
  -0.06    3.66     0.00    -5.42     0.00    62.90     BC 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -8.29     0.00    69.83     0.00   -29.62     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -3.85     0.00     6.26     0.00   -63.15     FC 3F 28 00 01     T1..4..   TTT.M.

  -0.06    8.13     0.00   -69.24     0.00    29.36     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06    3.66     0.00    -5.42     0.00    62.82     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -8.29     0.00    69.83     0.00   -29.70     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -3.85     0.00     6.26     0.00   -63.15     FC 3F 28 00 01     T1..4..   TTT.M.

  -0.06    8.13     0.00   -69.24     0.00    29.36     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06    3.66     0.00    -5.42     0.00    62.82     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -8.29     0.00    69.83     0.00   -29.70     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -3.85     0.03     6.17     0.00   -63.15     FC 3F 28 00 01     T1..4..   TTT.M.

  -0.06    8.13     0.00   -69.24     0.00    29.36     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06    3.66     0.00    -5.42     0.00    62.82     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -8.29     0.00    69.83     0.00   -29.70     FC 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -3.28     0.00     6.17    19.52   -63.15     FC 3F 28 00 01     T1..4..   TTT.M.

  -0.06    0.31     0.00   -69.24    44.46    29.45     6C 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -0.09     0.00    -5.42   -57.73    62.82     6C 3F 28 00 01     T1..4..   TTT.M.
  -0.06   -0.06     0.00    69.83   -40.04   -29.70     6C 3F 28 00 00     T1..4..   TTT.M.
  -0.06   -0.06     0.00     6.17    57.06   -63.15     6C 3F 28 00 00     T1..4..   TTT.M.

  -0.06   -0.06     0.00   -69.24    39.88    29.45     06 3F 00 00 00     T12....   TTT.M.
  -0.06   -0.06     0.00    -5.42   -57.23    62.82     02 3F 00 00 00     T12....   TTT.M.
  -0.06   -0.06     0.00    69.83   -40.13   -29.70     02 38 00 00 00     T12....   ....M.
  -0.06   -0.06     0.00     6.09    57.06   -63.07     02 38 00 00 00     T12....   ....M.

  -0.06   -0.06     0.00   -69.24    39.88    29.45     02 38 00 00 00     T12....   ....M.
  -0.06   -0.06     0.00    -5.42   -57.23    62.82     02 38 00 00 00     T12....   ....M.
  -0.06   -0.06     0.00    69.83   -40.04   -29.78     02 38 00 00 00     T12....   ....M.
  -0.06   -0.06     0.00     6.09    57.06   -63.07     02 38 00 00 00     T12....   ....M.

  -0.06   -0.06     0.00   -69.24    39.88    29.45     02 38 00 00 00     T12....   ....M.
  -0.03   -0.06     0.00    -5.42   -57.23    62.82     02 38 00 00 00     T12....   ....M.
  -0.06   -0.06     0.00    69.83   -40.04   -29.78     02 38 00 00 00     T12....   ....M.
  -0.03   -0.06     0.00     6.09    57.14   -63.07     02 38 00 00 00     T12....   ....M.
```

Example Event Report 2 (continued)

```
Type: 86BFT   Energy (MJ):  12.66

Schm = 2          50FT   = 8.60      TTpu   = 6.00      TTdo    = 2.00      62FC = 4.00
50LD = 0.52       62LD   = 5.50      62LP   = 3.25
62AP = 5.25       62AF   = 7.50      E62A   = N         DRTE    = N         RTTD = 2.00
37OP = 2.25       26CF   = 1.45      26CP   = 1.09      26TF    = 4.56      26TP = 3.42
47Q  = 18.70      62OP   = 3.00      CRTC   = 80        TRTC    = 80
59FO = 4.01       62FF   = 30.00     62FP   = 25.00
87UB = 16         62UC   = 12.00     62UF   = 60.00     62UP    = 50.00
50MD = 0.10       62M1   = 600.00    62M2   = 600.00    ModTrip= Y
CTR  = 600        PTR    = 4300
Topen= 2.25       Tclose= 10.25      Vwarn = 0.47
TIME1= 5          TIME2 = 0          AUTO  = 2          RINGS   = 3

Logic settings:

M86T  MA1  MA2  MA3  MA4  MA5  MER
 C1    00   02   00   20   00   20
 80    08   00   00   40   00   48
 81    00   00   02   40   04   42
 00    00   00   00   55   00   55
 00    00   00   00   50   00   5F
 --    --   --   --   --   --   00
 --    --   --   --   --   --   07
```

Note: The SEL-2BFR-2 Relay includes the RTSD setting (not shown).

Prefault Data

The following is the first six cycles (quarter-cycles 1 - 24) of Event Report 2, showing pre-fault and event triggering conditions.

```
                 Amps and Volts Sec

             Currents            Voltages          Relay Word      Outs     Ins
                                                                   8AAAAAA  TTT5MC
                                                                   612345L  PPP2OL
   IA      IB      IC      VA      VB      VC    R1 R2 R3 R4 R5    T        ABCAD         Quarter-Cycle

 -1.06    0.50    0.44    0.00    0.00    0.00   0C 00 00 00 00   .......  ...5M.              1
 -0.13   -0.88    0.91    0.00    0.00    0.00   0C 00 00 00 00   .......  ...5M.              2
  0.97   -0.63   -0.44    0.00    0.00    0.00   0C 00 00 00 00   .......  ...5M.              3
  2.72   -0.06   -2.78    0.00    0.00    0.00   0C 00 00 00 00   .......  ...5M.              4

 -0.16    7.66   -7.63    0.00    0.00    0.00   0C 00 00 00 00   .......  ...5M.              5
 -9.20    3.72    5.29    0.00    0.00    0.00   1C 00 00 00 00   .......  ...5M.              6
  0.81   -8.29    7.38    0.00    0.00    0.00   1C 00 00 00 00   .......  ...5M.              7
  9.01   -3.88   -5.22    0.00    0.00    0.00   1C 07 00 00 00   .......  TTT5M.              8

 -0.88    8.10   -7.32    0.00    0.00    0.00   1C 07 00 00 00   .......  TTT5M.              9
 -9.10    3.69    5.29    0.00    0.00    0.00   1C 07 00 00 00   .......  TTT5M.             10
  0.78   -8.29    7.41    0.00    0.00    0.00   1C 07 00 00 00   .......  TTT5M.             11
  6.35   -3.88   -3.07   -3.17    0.00  -16.10   1C 27 00 00 00   .......  TTT5M.             12

 -0.81    8.13    0.38  -68.07    0.00   23.61   1C 27 00 00 00   .......  TTT5M.             13
  0.03    3.69   -0.06   -5.42    0.00   63.49   1C 27 00 00 00   .......  TTT5M.             14
 -0.06   -8.29    0.03   69.83    0.00  -29.62   1C 27 00 00 01   .......  TTT5M.             15
 -0.06   -3.85    0.00    6.34    0.00  -63.23   1C 27 00 00 01   .......  TTT5M.             16

 -0.06    8.10    0.00  -69.24    0.00   29.28   1C 37 28 00 01   .......  TTT5M.             17
 -0.06    3.66    0.00   -5.34    0.00   62.90   1C 3F 28 00 01   .......  TTT5M.             18
 -0.06   -8.29    0.00   69.83    0.00  -29.62   1C 3F 28 00 01   .1.....  TTT5M.             19
 -0.06   -3.85    0.00    6.34    0.00  -63.15   1C 3F 28 00 01   .1.....  TTT5M.             20

 -0.06    8.13    0.00  -69.24    0.00   29.28   1C 3F 28 00 01   .1.....  TTT5M.             21
 -0.06    3.69    0.00   -5.42    0.00   62.90   3C 3F 28 00 01   .1..4..  TTT5M.             22
 -0.06   -8.29    0.00   69.83    0.00  -29.62   3C 3F 28 00 01   .1..4..  TTT5M.             23
 -0.06   -3.85    0.00    6.34    0.00  -63.15   BC 3F 28 00 01   T1..4..  TTT5M.             24
```

The following outline lists observed incidents shown in Example Event Report 2 by quarter-cycle.

Quarter Cycle	Event Report Shows:
1-5	Prefault Conditions:
	• Balanced load currents and no voltage measured across the breaker.
	• Hexadecimal 0C in Relay Word row 1 indicates pickup of the 50LD and 50MD elements.
	• 5 in 52A Input column verifies breaker closure (as does load current flow).
	• M in MOD Input column verifies MOD closure.
6-7	Fault Inception:
	• Hexadecimal 1C in Relay Word row 1 indicates that 50FT, 50LD, and 50MD elements are picked up in at least one phase.
8-11	• Ts in TPA, TPB, and TPC columns indicate assertion of all three trip inputs. Hexadecimal 07 in Relay Word row 2 also confirms trip input assertion.
12-14	Breaker Operation:
	• Hexadecimal 27 in Relay Word row 2 indicates 59FO element pickup due to detection of voltage across the breaker. This shows that at least one breaker pole is opening.
15-16	• Hexadecimal 01 in Relay Word row 5 indicates 47Q element pickup.
17	• Hexadecimal 37 in Relay Word row 2 indicates 59H element pickup.
	• Hexadecimal 28 in Relay Word row 3 indicates 87UA and 87UC phase current unbalance element pickup.
18	• Hexadecimal 3F in Relay Word row 2 indicates pickup of the 59FO and 59H overvoltage elements, ALRM breaker operation alarm, and the trip inputs. The ALRM bit asserts because 52A remains asserted more than Topen cycles after trip input assertion.
19-21	• 1 in the Output column indicates A1 output pickup in response to ALRM bit assertion in the previous quarter-cycle. Output assertions due to the ALRM bit always lag by one quarter-cycle (see ***Section 2: Specifications***, Alarm Logic).
22-23	• Hexadecimal 3C in Relay Word row 1 indicates assertion of the Load Current Pending Failure bit and the 50FT, 50LD, and 50MD overcurrent elements.
	• 4 in the Output column indicates A4 output assertion due to LPF bit assertion.
24	• Hexadecimal BC in Relay Word row 1 indicates FBF bit assertion in addition to the LPF, 50FT, 50LD and 50MD bits.
	• T in the 86T Output column indicates closure of the 86BF TRIP output contacts in response to FBF bit assertion.

The first 24 quarter-cycles of data show the inception of the three-phase fault and the issue of the trip signal from the line protective relay. Assertion of the 50FT element in row 8 shows that at least one phase current magnitude is above the 50FT element setting. The SEL-2BFR Relay asserts the 86BF TRIP output in event report row 24, four cycles following assertion of trip inputs. Had the 50FT element deasserted by this time, the relay would not have issued the 86BF TRIP signal.

Breaker Failure Tripping

Event report quarter-cycles 25 through 44 appear below. The hexadecimal FC in Relay Word row 1 indicates 62LD timer expiration in quarter-cycle 31.

IA	IB	IC	VA	VB	VC	R1	R2	R3	R4	R5	Outs	Ins	Quarter-Cycle
Amps and Volts Sec													
Currents			Voltages			Relay Word					Outs 8AAAAAA 612345L T	Ins TTT5MC PPP2OL ABCAD	
-0.06	8.13	0.00	-69.24	0.00	29.28	BC	3F	28	00	01	T1..4..	TTT5M.	25
-0.03	3.66	0.00	-5.42	0.00	62.90	BC	3F	28	00	01	T1..4..	TTT5M.	26
-0.06	-8.29	0.00	69.83	0.00	-29.62	BC	3F	28	00	01	T1..4..	TTT5M.	27
-0.06	-3.85	0.00	6.26	0.00	-63.15	BC	3F	28	00	01	T1..4..	TTT5M.	28
-0.06	8.13	0.00	-69.24	0.08	29.36	BC	3F	28	00	01	T1..4..	TTT5M.	29
-0.06	3.66	0.00	-5.42	0.00	62.90	BC	3F	28	00	01	T1..4..	TTT.M.	30
-0.06	-8.29	0.00	69.83	0.00	-29.62	FC	3F	28	00	01	T1..4..	TTT.M.	31
-0.06	-3.85	0.00	6.26	0.00	-63.15	FC	3F	28	00	01	T1..4..	TTT.M.	32
-0.06	8.13	0.00	-69.24	0.00	29.36	FC	3F	28	00	01	T1..4..	TTT.M.	33
-0.06	3.66	0.00	-5.42	0.00	62.82	FC	3F	28	00	01	T1..4..	TTT.M.	34
-0.06	-8.29	0.00	69.83	0.00	-29.70	FC	3F	28	00	01	T1..4..	TTT.M.	35
-0.06	-3.85	0.00	6.26	0.00	-63.15	FC	3F	28	00	01	T1..4..	TTT.M.	36
-0.06	8.13	0.00	-69.24	0.00	29.36	FC	3F	28	00	01	T1..4..	TTT.M.	37
-0.06	3.66	0.00	-5.42	0.00	62.82	FC	3F	28	00	01	T1..4..	TTT.M.	38
-0.06	-8.29	0.00	69.83	0.00	-29.70	FC	3F	28	00	01	T1..4..	TTT.M.	39
-0.06	-3.85	0.03	6.17	0.00	-63.15	FC	3F	28	00	01	T1..4..	TTT.M.	40
-0.06	8.13	0.00	-69.24	0.00	29.36	FC	3F	28	00	01	T1..4..	TTT.M.	41
-0.06	3.66	0.00	-5.42	0.00	62.82	FC	3F	28	00	01	T1..4..	TTT.M.	42
-0.06	-8.29	0.00	69.83	0.00	-29.70	FC	3F	28	00	01	T1..4..	TTT.M.	43
-0.06	-3.28	0.00	6.17	19.52	-63.15	FC	3F	28	00	01	T1..4..	TTT.M.	44

Fault Clearing

Event report quarter-cycles 45 through 60 are below. This section of the report shows interruption of the fault current.

IA	IB	IC	VA	VB	VC	R1	R2	R3	R4	R5	Outs	Ins	Quarter-Cycle
Amps and Volts Sec													
Currents			Voltages			Relay Word					Outs 8AAAAAA 612345L T	Ins TTT5MC PPP2OL ABCAD	
-0.06	0.31	0.00	-69.24	44.46	29.45	6C	3F	28	00	01	T1..4..	TTT.M.	45
-0.06	-0.09	0.00	-5.42	-57.73	62.82	6C	3F	28	00	01	T1..4..	TTT.M.	46
-0.06	-0.06	0.00	69.83	-40.04	-29.70	6C	3F	28	00	00	T1..4..	TTT.M.	47
-0.06	-0.06	0.00	6.17	57.06	-63.15	6C	3F	28	00	00	T1..4..	TTT.M.	48
-0.06	-0.06	0.00	-69.24	39.88	29.45	06	3F	00	00	00	T12....	TTT.M.	49
-0.06	-0.06	0.00	-5.42	-57.23	62.82	02	3F	00	00	00	T12....	TTT.M.	50
-0.06	-0.06	0.00	69.83	-40.13	-29.70	02	38	00	00	00	T12....	....M.	51
-0.06	-0.06	0.00	6.09	57.06	-63.07	02	38	00	00	00	T12....	....M.	52
-0.06	-0.06	0.00	-69.24	39.88	29.45	02	38	00	00	00	T12....	....M.	53
-0.06	-0.06	0.00	-5.42	-57.23	62.82	02	38	00	00	00	T12....	....M.	54
-0.06	-0.06	0.00	69.83	-40.04	-29.78	02	38	00	00	00	T12....	....M.	55
-0.06	-0.06	0.00	6.09	57.06	-63.07	02	38	00	00	00	T12....	....M.	56
-0.06	-0.06	0.00	-69.24	39.88	29.45	02	38	00	00	00	T12....	....M.	57
-0.03	-0.06	0.00	-5.42	-57.23	62.82	02	38	00	00	00	T12....	....M.	58
-0.06	-0.06	0.00	69.83	-40.04	-29.78	02	38	00	00	00	T12....	....M.	59
-0.03	-0.06	0.00	6.09	57.14	-63.07	02	38	00	00	00	T12....	....M.	60

Quarter Cycle	Event Report Shows:
45-46	Fault Clearing
	• Hexadecimal FC in Relay Word row 1 changes to 6C, indicating FBF and 50FT bit dropout.
47-48	• Hexadecimal 01 in Relay Word row 5 changes to 00, indicating 47Q element dropout.
49	• Hexadecimal 6C in Relay Word row 1 changes to 06, indicating dropout of the LBF, LPF, and 50LD bits, leaving only 50MD and 52BV asserted.
	• 2 in the Outputs column indicates A2 output contact assertion due to 52BV bit assertion.
50	• Hexadecimal 06 in Relay Word row 1 changes to 02, indicating 50MD element dropout.
51	• Hexadecimal 3F in Relay Word row 2 changes to 38, indicating trip input deassertion, also shown in the trip inputs columns.
52-60	• The final rows of the event report show the state the breaker was left in prior to MODTrip and reset logic operation.

Event Summary

The event summary shows event type and energy interrupted by the breaker during the last fourteen cycles of the event. The values are in megajoules.

Event type shown is 86BFT because the relay closed the 86BF TRIP contacts during the event.

The report does not include mechanical and electrical operating times for the breaker because the relay issued an 86BF TRIP. The breaker did not operate correctly, so operating times would be meaningless.

Energy is the three-phase energy interrupted by the breaker during the first fourteen quarter-cycles of the event report, scaled in megajoules primary.

Example Event Reports 3 and 4: Thermal Failure of the A-Phase Trip Resistor

Fault Description

The SEL-2BFR Relay generated these event reports in response to thermal failure of the A-phase trip resistor. Event Report 3 shows the three-phase fault which required the breaker to operate. B-and C-phase breaker poles clear their contribution to the fault. The A-phase trip resistor did not completely operate, allowing current to continue flowing. Event Report 3 shows pre-fault data and breaker operation. Event Report 4 shows 86BF Trip operation to isolate the failed breaker. Row by row analysis for each report follows the full event reports below.

Example Event Report 3: Thermal Failure of the A-Phase Trip Resistor

Example 500 kV Breaker   Date: 6/1/92   Time: 08:58:17.725
FID=SEL-BFR-R105-V1-D910212

Amps and Volts Sec

Currents			Voltages			Relay Word					Outs	Ins
											8AAAAAA 612345L T	TTT5MC PPP2OL ABCAD
IA	IB	IC	VA	VB	VC	R1	R2	R3	R4	R5		
0.97	-0.59	-0.50	0.00	-0.08	-0.08	0C	00	00	00	00	....	...5M.
-0.03	0.78	-0.88	-0.08	-0.08	0.00	0C	00	00	00	00	....	...5M.
-1.06	0.44	0.50	-0.08	0.00	0.00	0C	00	00	00	00	....	...5M.
-0.06	-0.94	0.84	-0.08	0.00	0.00	0C	00	00	00	00	....	...5M.
0.97	-0.59	-0.50	0.00	0.00	-0.08	0C	00	00	00	00	....	...5M.
3.32	-0.16	-3.32	0.00	0.00	0.00	0C	00	00	00	00	....	...5M.
-0.84	7.98	-7.26	-0.08	0.00	0.00	0C	00	00	00	00	....	...5M.
-9.10	3.16	5.79	-0.08	0.00	0.00	1C	07	00	00	00	....	TTT5M.
1.41	-8.54	7.01	0.00	-0.08	-0.08	1C	07	00	00	00	....	TTT5M.
8.95	-3.32	-5.69	-0.08	-0.08	0.00	1C	07	00	00	00	....	TTT5M.
-1.50	8.35	-6.98	-0.08	0.00	0.00	1C	07	00	00	00	....	TTT5M.
-9.04	3.13	5.76	-0.08	0.00	0.00	1C	07	00	00	00	....	TTT5M.
1.41	-8.54	7.01	0.00	0.00	-0.08	1C	07	00	00	00	....	TTT5M.
5.82	-2.75	-2.94	-1.08	24.61	-19.94	1C	27	00	00	00	....	TTT5M.
-0.75	0.25	0.34	-15.27	40.38	28.45	0C	27	00	00	00	....	TTT5M.
-0.47	-0.09	-0.06	-0.33	-60.15	61.40	0C	27	00	00	00	....	TTT5M.
0.03	-0.06	0.00	15.52	-36.37	-33.79	0C	27	00	00	01	....	TTT5M.
0.44	-0.06	0.00	0.33	59.48	-61.07	0C	3F	00	00	01	....	TTT5M.
-0.13	-0.06	0.00	-15.52	36.21	33.37	04	3F	00	00	01	.1.....	TTT5M.
-0.56	-0.06	0.00	-0.33	-59.65	60.82	04	3F	10	00	01	.1.....	TTT5M.
0.03	-0.06	0.00	15.52	-36.37	-33.70	04	3F	18	00	01	.1.....	TTT5M.
0.44	-0.06	0.00	0.33	59.48	-61.07	04	3F	18	00	01	.1.....	TTT5M.
-0.13	-0.06	0.00	-15.52	36.12	33.37	06	38	18	00	01	.12....	....M.
-0.56	-0.06	0.00	-0.33	-59.65	60.82	06	38	18	00	01	.12....	....M.
0.03	-0.06	0.00	15.52	-36.37	-33.70	06	38	18	00	01	.12....	....M.
0.44	-0.06	0.00	0.25	59.48	-61.07	06	38	18	00	09	.12....	....M.
-0.16	-0.06	0.00	-15.52	36.12	33.45	0C	38	18	00	09	.1.....	....M.
-0.56	-0.06	0.00	-0.33	-59.65	60.82	0C	38	18	00	09	.1.....	....M.
0.03	-0.06	0.00	15.52	-36.37	-33.79	0C	38	18	00	09	.1.....	....M.
0.44	-0.06	0.00	0.25	59.56	-61.07	0C	38	18	00	09	.1.....	....M.
-0.16	-0.06	0.00	-15.52	36.21	33.45	0C	38	18	00	09	.1.....	....M.
-0.56	-0.06	0.00	-0.33	-59.65	60.82	0C	38	18	00	09	.1.....	....M.
0.03	-0.06	0.00	15.52	-36.29	-33.79	0C	38	18	00	09	.1.....	....M.
0.44	-0.06	0.00	0.25	59.56	-61.07	0C	38	18	00	09	.1.....	....M.
-0.16	-0.06	0.00	-15.52	36.12	33.45	0C	38	18	00	09	.1.....	....M.
-0.56	-0.06	0.00	-0.25	-59.73	60.82	0C	38	18	00	09	.1.....	....M.
0.03	-0.06	0.00	15.52	-36.29	-33.79	0C	38	18	00	09	.1.....	....M.
0.44	-0.06	0.00	0.25	59.56	-60.98	0C	38	18	00	09	.1.....	....M.
-0.13	-0.06	0.00	-15.52	36.12	33.45	06	38	18	00	09	.12....	....M.
-0.56	-0.06	0.00	-0.25	-59.73	60.73	06	38	18	00	09	.12....	....M.
0.03	-0.06	0.00	15.52	-36.29	-33.79	06	38	18	00	09	.12....	....M.
0.44	-0.06	0.00	0.25	59.56	-60.98	06	38	18	00	09	.12....	....M.
-0.16	-0.06	0.00	-15.52	36.04	33.54	0C	38	18	00	09	.1.....	....M.
-0.56	-0.06	0.00	-0.25	-59.73	60.73	0C	38	18	00	09	.1.....	....M.
0.03	-0.06	0.00	15.52	-36.29	-33.87	0C	38	18	00	09	.1.....	....M.
0.44	-0.06	0.00	0.25	59.56	-60.98	0C	38	18	00	09	.1.....	....M.
-0.16	-0.06	0.00	-15.52	36.04	33.54	0C	38	18	00	09	.1.....	....M.
-0.56	-0.06	0.00	-0.25	-59.73	60.73	0C	38	18	00	09	.1.....	....M.
0.03	-0.06	-0.03	15.52	-36.21	-33.87	0C	38	18	00	09	.1.....	....M.
0.44	-0.06	0.00	0.25	59.56	-60.98	0C	38	18	00	09	.1.....	....M.
-0.16	-0.06	0.00	-15.52	36.04	33.54	0C	38	18	00	09	.1.....	....M.
-0.56	-0.06	0.00	-0.25	-59.73	60.73	0C	38	18	00	09	.1.....	....M.
0.03	-0.06	-0.03	15.52	-36.21	-33.87	0C	38	18	00	09	.1.....	....M.
0.44	-0.06	0.00	0.25	59.65	-60.98	0C	38	18	00	09	.1.....	....M.
-0.16	-0.06	0.00	-15.52	35.96	33.62	0C	38	18	00	09	.1.....	....M.
-0.56	-0.06	0.00	-0.25	-59.73	60.73	0C	38	18	00	09	.1.....	....M.
0.03	-0.06	-0.03	15.52	-36.21	-33.87	0C	38	18	00	09	.1.....	....M.
0.44	-0.06	0.00	0.25	59.65	-60.98	0C	38	18	00	09	.1.....	....M.
-0.16	-0.06	0.00	-15.52	35.96	33.62	0C	38	18	00	09	.1.....	....M.
-0.56	-0.06	0.00	-0.25	-59.81	60.73	0C	38	18	00	09	.1.....	....M.

Example Event Report 3 (continued)

```
Type: TRIP3   52A (cyc): 3.75   IV-Time (cyc):  2.75   Energy (MJ):   9.50

Schm = 2        50FT   = 8.60     TTpu  = 6.00      TTdo    = 2.00     62FC = 4.00
50LD = 0.52     62LD   = 5.50     62LP  = 3.25
62AP = 5.25     62AF   = 7.50     E62A  = N         DRTE    = N        RTTD = 2.00
37OP = 2.25     26CF   = 1.45     26CP  = 1.09      26TF    = 4.56     26TP = 3.42
47Q  = 18.70    62OP   = 3.00     CRTC  = 80        TRTC    = 80
59FO = 4.01     62FF   = 30.00    62FP  = 25.00
87UB = 16       62UC   = 12.00    62UF  = 60.00     62UP    = 50.00
50MD = 0.10     62M1   = 600.00   62M2  = 600.00    ModTrip= Y
CTR  = 600      PTR    = 4300
Topen= 2.25     Tclose= 10.25     Vwarn = 0.47
TIME1= 5        TIME2 = 0         AUTO  = 2         RINGS   = 3

Logic settings:

M86T  MA1  MA2  MA3  MA4  MA5  MER
 C1   00   02   00   20   00   20
 80   08   00   00   40   00   48
 81   00   00   02   40   04   42
 00   00   00   00   55   00   55
 00   00   00   00   50   00   5F
 --   --   --   --   --   --   00
 --   --   --   --   --   --   07
```

Note: The SEL-2BFR-2 Relay includes the RTSD setting (not shown).

Example Event Report 4: Thermal Failure of the A-Phase Trip Resistor

```
Example 500 kV Breaker                        Date: 6/1/92       Time: 08:58:18.375
FID=SEL-BFR-R105-V1-D910212

                 Amps and Volts Sec
           Currents              Voltages            Relay Word       Outs      Ins
                                                                      8AAAAAA   TTT5MC
                                                                      612345L   PPP2OL
    IA      IB      IC      VA      VB      VC     R1 R2 R3 R4 R5     T         ABCAD

  0.03   -0.06    0.00   15.52  -35.62  -34.45    0C 38 18 10 09    .1..4..   ....M.
  0.44   -0.06    0.00    0.08   59.98  -60.57    0C 38 18 10 09    .1..4..   ....M.
 -0.16   -0.06    0.00  -15.52   35.46   34.20    0C 38 18 10 09    .1..4..   ....M.
 -0.56   -0.06    0.00   -0.08  -60.06   60.40    0C 38 18 10 09    .1..4..   ....M.

  0.03   -0.06   -0.03   15.52  -35.54  -34.45    0C 38 18 10 09    .1..4..   ....M.
  0.44   -0.06    0.00    0.08   59.98  -60.57    0C 38 18 10 09    .1..4..   ....M.
 -0.16   -0.06    0.00  -15.52   35.46   34.29    0C 38 18 10 09    .1..4..   ....M.
 -0.56   -0.06    0.00   -0.17  -60.06   60.40    0D 38 18 30 09    T1..4..   ....M.

  0.03   -0.06    0.00   15.52  -35.54  -34.45    0D 38 18 30 09    T1..4..   ....M.
  0.44   -0.06    0.00    0.08   60.06  -60.57    0D 38 18 30 09    T1..4..   ....M.
 -0.16   -0.06    0.00  -15.52   35.37   34.29    0D 38 18 30 09    T1..4..   ....M.
 -0.56   -0.06    0.00   -0.08  -60.15   60.40    0D 38 18 30 09    T1..4..   ....M.

  0.03   -0.06    0.00   15.52  -35.54  -34.45    0D 38 18 30 09    T1..4..   ....M.
  0.44   -0.06    0.00    0.08   60.06  -60.57    0D 38 18 30 09    T1..4..   ....M.
 -0.16   -0.06    0.00  -15.52   35.37   34.29    0D 38 18 30 09    T1..4..   ....M.
 -0.56   -0.06    0.00   -0.08  -60.15   60.40    0D 38 18 30 09    T1..4..   ....M.

  0.03   -0.06   -0.03   15.52  -35.54  -34.54    0D 38 18 30 09    T1..4..   ....M.
  0.25   -0.06    0.00   -3.92   60.06  -60.57    07 38 18 30 09    T12.4..   ....M.
 -0.09   -0.06    0.00  -68.99   35.37   34.37    07 38 18 30 08    T12.4..   ....M.
 -0.06   -0.06    0.00    0.08  -60.15   60.40    07 38 10 30 08    T12.4..   ....M.

 -0.06   -0.06    0.00   70.08  -35.46  -34.54    07 38 00 30 08    T12.4..   ....M.
 -0.06   -0.06    0.00    0.67   60.06  -60.48    07 38 00 30 08    T12.4..   ....M.
 -0.06   -0.06    0.00  -69.58   35.37   34.37    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.06    0.00    0.17  -60.15   60.40    02 38 00 30 00    T12.4..   ....M.

 -0.06   -0.06    0.00   70.08  -35.46  -34.54    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.06    0.00    0.67   60.06  -60.48    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.06    0.00  -69.58   35.29   34.37    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.03    0.00    0.17  -60.15   60.31    02 38 00 30 00    T12.4..   ....M.

 -0.06   -0.06    0.00   70.08  -35.46  -34.54    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.06    0.00    0.58   60.06  -60.48    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.06    0.00  -69.58   35.29   34.37    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.06    0.00    0.17  -60.15   60.31    02 38 00 30 00    T12.4..   ....M.

 -0.06   -0.06    0.00   70.08  -35.37  -34.62    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.06    0.00    0.58   60.06  -60.48    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.06    0.00  -69.58   35.29   34.45    02 38 00 30 00    T12.4..   ....M.
 -0.06   -0.06    0.00    0.17  -60.15   60.31    02 38 00 30 00    T12.4..   ....M.
```

Example Event Report 4 (continued)

```
-0.06  -0.06   0.00  70.08 -35.37 -34.62   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.50  60.15 -60.48   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00 -69.58  35.20  34.45   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.17 -60.23  60.31   02 38 00 30 00  T12.4..  ....M.

-0.06  -0.06  -0.03  70.08 -35.37 -34.62   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.50  60.15 -60.48   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00 -69.58  35.20  34.45   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.17 -60.23  60.31   02 38 00 30 00  T12.4..  ....M.

-0.06  -0.06   0.00  70.08 -35.29 -34.62   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.50  60.15 -60.40   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00 -69.58  35.20  34.45   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.17 -60.23  60.31   02 38 00 30 00  T12.4..  ....M.

-0.06  -0.06   0.00  70.08 -35.29 -34.62   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.50  60.15 -60.40   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00 -69.58  35.20  34.45   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.17 -60.23  60.31   02 38 00 30 00  T12.4..  ....M.

-0.06  -0.06   0.00  70.08 -35.29 -34.62   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.50  60.15 -60.40   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00 -69.58  35.20  34.45   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.17 -60.23  60.31   02 38 00 30 00  T12.4..  ....M.

-0.06  -0.06   0.00  70.08 -35.29 -34.62   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.50  60.15 -60.40   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00 -69.58  35.20  34.45   02 38 00 30 00  T12.4..  ....M.
-0.06  -0.06   0.00   0.17 -60.23  60.31   02 38 00 30 00  T12.4..  ....M.

Type: 86BFT   Energy (MJ):    0.61

Schm = 2         50FT   = 8.60     TTpu   = 6.00     TTdo    = 2.00      62FC = 4.00
50LD = 0.52      62LD   = 5.50     62LP   = 3.25
62AP = 5.25      62AF   = 7.50     E62A   = N        DRTE    = N         RTTD = 2.00
37OP = 2.25      26CF   = 1.45     26CP   = 1.09     26TF    = 4.56      26TP = 3.42
47Q  = 18.70     62OP   = 3.00     CRTC   = 80       TRTC    = 80
59FO = 4.01      62FF   = 30.00    62FP   = 25.00
87UB = 16        62UC   = 12.00    62UF   = 60.00    62UP    = 50.00
50MD = 0.10      62M1   = 600.00   62M2   = 600.00   ModTrip= Y
CTR  = 600       PTR    = 4300
Topen= 2.25      Tclose= 10.25     Vwarn = 0.47
TIME1= 5         TIME2 = 0         AUTO   = 2        RINGS   = 3

Logic settings:

M86T  MA1  MA2  MA3  MA4  MA5  MER
  C1   00   02   00   20   00   20
  80   08   00   00   40   00   48
  81   00   00   02   40   04   42
  00   00   00   00   55   00   55
  00   00   00   00   50   00   5F
  --   --   --   --   --   --   00
  --   --   --   --   --   --   07
```

Note: The SEL-2BFR-2 Relay includes the RTSD setting (not shown).

Prefault Data, Event Report 3

The first four cycles (quarter-cycles 1 - 16) of Event Report 3 appear below, showing pre-fault and event triggering conditions.

Amps and Volts Sec Currents			Voltages			Relay Word					Outs	Ins	
											8AAAAAA 612345L T	TTT5MC PPP2OL ABCAD	
IA	IB	IC	VA	VB	VC	R1	R2	R3	R4	R5			Quarter-Cycle
0.97	-0.59	-0.50	0.00	-0.08	-0.08	0C	00	00	00	00	....	...5M.	1
-0.03	0.78	-0.88	-0.08	-0.08	0.00	0C	00	00	00	00	....	...5M.	2
-1.06	0.44	0.50	-0.08	0.00	0.00	0C	00	00	00	00	....	...5M.	3
-0.06	-0.94	0.84	-0.08	0.00	0.00	0C	00	00	00	00	....	...5M.	4
0.97	-0.59	-0.50	0.00	0.00	-0.08	0C	00	00	00	00	....	...5M.	5
3.32	-0.16	-3.32	0.00	0.00	0.00	0C	00	00	00	00	....	...5M.	6
-0.84	7.98	-7.26	-0.08	0.00	0.00	0C	00	00	00	00	....	...5M.	7
-9.10	3.16	5.79	-0.08	0.00	0.00	1C	07	00	00	00	....	TTT5M.	8
1.41	-8.54	7.01	0.00	-0.08	-0.08	1C	07	00	00	00	....	TTT5M.	9
8.95	-3.32	-5.69	-0.08	-0.08	0.00	1C	07	00	00	00	....	TTT5M.	10
-1.50	8.35	-6.98	-0.08	0.00	0.00	1C	07	00	00	00	....	TTT5M.	11
-9.04	3.13	5.76	-0.08	0.00	0.00	1C	07	00	00	00	....	TTT5M.	12
1.41	-8.54	7.01	0.00	0.00	-0.08	1C	07	00	00	00	....	TTT5M.	13
5.82	-2.75	-2.94	-1.08	24.61	-19.94	1C	27	00	00	00	....	TTT5M.	14
-0.75	0.25	0.34	-15.27	40.38	28.45	0C	27	00	00	00	....	TTT5M.	15
-0.47	-0.09	-0.06	-0.33	-60.15	61.40	0C	27	00	00	00	....	TTT5M.	16

The following outline lists observed incidents in Example Event Report 3 by quarter-cycle.

Quarter Cycle	Event Report Shows:
1-7	Prefault conditions: • Balanced load currents and no voltage measured across the breaker. • Hexadecimal 0C in Relay Word row 1 indicates 50LD and 50MD element pickup. • 5 in 52A Input column verifies breaker closure (as does load current flow). • M in MOD Input column verifies MOD closure.
8-13	Fault Inception: • Hexadecimal 1C in Relay Word row 1 indicates that 50FT, 50LD, and 50MD elements are picked up in at least one phase. • Ts in TPA, TPB, and TPC columns indicate assertion of all three trip inputs. Hexadecimal 07 in Relay Word row 2 also confirms trip input assertion.
14	Breaker Operation: • Hexadecimal 27 in Relay Word row 2 indicates 59FO element pickup due to detection of voltage across the breaker. This shows that at least one breaker pole is opening.
15-16	• Hexadecimal 1C in Relay Word row 1 changes to 0C, indicating that 50FT has dropped out in all three phases. Current samples in columns Ia, Ib, and Ic are decreasing in magnitude.

Breaker Operation

Event report rows 17 through 28 show the partial completion of the breaker opening sequence, dropout of the B- and C-phase currents, dropout of the trip inputs, and pickup of elements in the thermal protection logic.

Amps and Volts Sec

Currents			Voltages			Relay Word					Outs	Ins	
											8AAAAAA	TTT5MC	
											612345L	PPP2OL	
IA	IB	IC	VA	VB	VC	R1	R2	R3	R4	R5	T	ABCAD	Quarter-Cycle
0.03	-0.06	0.00	15.52	-36.37	-33.79	0C	27	00	00	01	....	TTT5M.	17
0.44	-0.06	0.00	0.33	59.48	-61.07	0C	3F	00	00	01	....	TTT5M.	18
-0.13	-0.06	0.00	-15.52	36.21	33.37	04	3F	00	00	01	.1.....	TTT5M.	19
-0.56	-0.06	0.00	-0.33	-59.65	60.82	04	3F	10	00	01	.1.....	TTT5M.	20
0.03	-0.06	0.00	15.52	-36.37	-33.70	04	3F	18	00	01	.1.....	TTT5M.	21
0.44	-0.06	0.00	0.33	59.48	-61.07	04	3F	18	00	01	.1.....	TTT5M.	22
-0.13	-0.06	0.00	-15.52	36.12	33.37	06	38	18	00	01	.12....	....M.	23
-0.56	-0.06	0.00	-0.33	-59.65	60.82	06	38	18	00	01	.12....	....M.	24
0.03	-0.06	0.00	15.52	-36.37	-33.70	06	38	18	00	01	.12....	....M.	25
0.44	-0.06	0.00	0.25	59.48	-61.07	06	38	18	00	09	.12....	....M.	26
-0.16	-0.06	0.00	-15.52	36.12	33.45	0C	38	18	00	09	.1.....	....M.	27
-0.56	-0.06	0.00	-0.33	-59.65	60.82	0C	38	18	00	09	.1.....	....M.	28

Quarter Cycle	Event Report Shows:
17	• Hexadecimal 01 in Relay Word row 5 indicates 47Q element pickup.
18	• Hexadecimal 3F in Relay Word row 2 indicates 59FO and 59H overvoltage element pickup, ALRM breaker operation alarm, and the trip inputs.
19	• Hexadecimal 0C in Relay Word row 1 changes to 04 indicating 50LD element dropout.
	• 1 in the Output column indicates A1 output pickup in response to ALRM bit assertion the previous quarter-cycle. Output assertions due to the ALRM bit always lag by one quarter-cycle (see *Section 2: Specifications*, Alarm Logic.
20	• Hexadecimal 10 in Relay Word row 3 indicates pickup of the 87UB phase current unbalance element.
21-22	• Hexadecimal 10 in Relay Word row 3 changes to 18, indicating pickup of the 87UC phase current unbalance element.
23-25	• Hexadecimal 04 in Relay Word row 1 changes to 06, indicating 52BV bit pickup.
	• Hexadecimal 3F in Relay Word row 2 changes to 38, indicating TRIP input dropout, which is also shown by the disappearance of the Ts from the Trip inputs columns.
	• 5 in 52A inputs column changes to "." indicating 52A input deassertion. The breaker auxiliary contact has opened.
	• 2 in A2 output column indicates operation of the A2 output. A2 is set to close for assertion of the 52BV bit.
26	• Hexadecimal 09 in Relay Word row 5 indicates DOPA bit pickup.
	• Hexadecimal 0C in Relay Word row 1 indicates 50LD and 50MD element pickup and 52BV bit dropout.
27-60	• Remainder of the event report shows the 50LD element dropout and pickup one more time, indicating that A-phase current is on the pickup boundary of the 50LD element setting. M in the inputs column shows that the MOD status input is asserted, indicating that the MOD auxiliary contact is closed.

Event Summary, Event Report 3

The event summary shows event type, mechanical and electrical operating times of the protected breaker, and energy interrupted by the breaker during the first fourteen cycles of the event, shown in megajoules.

Event type shown is TRIP3 because all three trip inputs were asserted during the event, but the 86BF TRIP output was not asserted.

Mechanical operating time of the breaker 52A equals 3.75 cycles. This is the amount of time from the first TRIP input assertion to 52A input deassertion.

Electrical operating time IV-Time equals 2.75 cycles. This is the time from the first trip input assertion to 50LD phase overcurrent element dropout in all three phases.

Energy is the three-phase energy interrupted by the breaker during the first fourteen quarter-cycles of the event report, scaled in megajoules primary.

From the instant the DOPA bit asserts in quarter-cycle 26, the relay adds energy to the A-phase trip resistor thermal model.

Prefault Data, Event Report 4

The following is the first four cycles (quarter-cycles 1 - 16) of Event Report 4, showing pre-fault and event triggering conditions.

```
              Amps and Volts Sec

          Currents              Voltages             Relay Word      Outs     Ins
                                                                    8AAAAAA  TTT5MC
                                                                    612345L  PPP2OL
    IA      IB      IC      VA      VB      VC    R1 R2 R3 R4 R5    T        ABCAD                 Quarter-Cycle

  0.03   -0.06    0.00   15.52 -35.62 -34.45    0C 38 18 10 09    .1..4..  ....M.                      1
  0.44   -0.06    0.00    0.08  59.98 -60.57    0C 38 18 10 09    .1..4..  ....M.                      2
 -0.16   -0.06    0.00  -15.52  35.46  34.20    0C 38 18 10 09    .1..4..  ....M.                      3
 -0.56   -0.06    0.00   -0.08 -60.06  60.40    0C 38 18 10 09    .1..4..  ....M.                      4

  0.03   -0.06   -0.03   15.52 -35.54 -34.45    0C 38 18 10 09    .1..4..  ....M.                      5
  0.44   -0.06    0.00    0.08  59.98 -60.57    0C 38 18 10 09    .1..4..  ....M.                      6
 -0.16   -0.06    0.00  -15.52  35.46  34.29    0C 38 18 10 09    .1..4..  ....M.                      7
 -0.56   -0.06    0.00   -0.17 -60.06  60.40    0D 38 18 30 09    T1..4..  ....M.                      8

  0.03   -0.06    0.00   15.52 -35.54 -34.45    0D 38 18 30 09    T1..4..  ....M.                      9
  0.44   -0.06    0.00    0.08  60.06 -60.57    0D 38 18 30 09    T1..4..  ....M.                     10
 -0.16   -0.06    0.00  -15.52  35.37  34.29    0D 38 18 30 09    T1..4..  ....M.                     11
 -0.56   -0.06    0.00   -0.08 -60.15  60.40    0D 38 18 30 09    T1..4..  ....M.                     12

  0.03   -0.06    0.00   15.52 -35.54 -34.45    0D 38 18 30 09    T1..4..  ....M.                     13
  0.44   -0.06    0.00    0.08  60.06 -60.57    0D 38 18 30 09    T1..4..  ....M.                     14
 -0.16   -0.06    0.00  -15.52  35.37  34.29    0D 38 18 30 09    T1..4..  ....M.                     15
 -0.56   -0.06    0.00   -0.08 -60.15  60.40    0D 38 18 30 09    T1..4..  ....M.                     16
```

The following outline lists observed incidents shown in Example Event Report 4 by quarter-cycle.

Quarter Cycle	Event Report Shows:
1-7	Event Continues: ● Hexadecimal 0C in Relay Word row 1 indicates 50LD and 50MD element pickup. ● Hexadecimal 38 in Relay Word row 2 indicates 59FO, 59H, and ALRM bit pickup. ● Hexadecimal 18 in Relay Word row 3 indicates 87UB and 87UC phase current unbalance element pickup. ● Hexadecimal 10 in Relay Word row 4 indicates pickup of the TRPA bit, A-phase trip resistor thermal pending failure. ● Hexadecimal 09 in Relay Word row 5 indicates DOPA and 47Q bit pickup. ● 1 in Outputs column indicates A1 output assertion due to ALRM bit assertion. ● 4 in Outputs column indicates A4 output assertion due to TRPA bit assertion. ● M in MOD Input column verifies MOD closure.
8-16	86BF TRIP: ● T in 86T Output column indicates 86BF TRIP output assertion. ● Hexadecimal 0D in Relay Word row 1 indicates assertion of the 50LD, 50MD, and TTF bits. TTF asserts for trip resistor thermal failures in the presence of phase current. ● Hexadecimal 30 in Relay Word row 4 indicates TRFA and TRPA bit assertion, showing that the A-phase trip resistor thermal model has exceeded the pending failure and failure energy levels.

Post-Fault

Amps and Volts Sec

Currents			Voltages			Relay Word					Outs	Ins	
											8AAAAAA 612345L	TTT5MC PPP2OL	
IA	IB	IC	VA	VB	VC	R1	R2	R3	R4	R5	T	ABCAD	Quarter-Cycle
0.03	-0.06	-0.03	15.52	-35.54	-34.54	0D	38	18	30	09	T1..4..	....M.	17
0.25	-0.06	0.00	-3.92	60.06	-60.57	07	38	18	30	09	T12.4..	....M.	18
-0.09	-0.06	0.00	-68.99	35.37	34.37	07	38	18	30	08	T12.4..	....M.	19
-0.06	-0.06	0.00	0.08	-60.15	60.40	07	38	10	30	08	T12.4..	....M.	20
-0.06	-0.06	0.00	70.08	-35.46	-34.54	07	38	00	30	08	T12.4..	....M.	21
-0.06	-0.06	0.00	0.67	60.06	-60.48	07	38	00	30	08	T12.4..	....M.	22
-0.06	-0.06	0.00	-69.58	35.37	34.37	02	38	00	30	00	T12.4..	....M.	23
-0.06	-0.06	0.00	0.17	-60.15	60.40	02	38	00	30	00	T12.4..	....M.	24
-0.06	-0.06	0.00	70.08	-35.46	-34.54	02	38	00	30	00	T12.4..	....M.	25
-0.06	-0.06	0.00	0.67	60.06	-60.48	02	38	00	30	00	T12.4..	....M.	26
-0.06	-0.06	0.00	-69.58	35.29	34.37	02	38	00	30	00	T12.4..	....M.	27
-0.06	-0.03	0.00	0.17	-60.15	60.31	02	38	00	30	00	T12.4..	....M.	28

Quarter Cycle	Event Report Shows:
18-19	• Hexadecimal 07 in Relay Word row 1 indicates 50LD element dropout and 52BV bit pickup.
	• 2 in Outputs column indicates A2 contact assertion due to 52BV bit assertion.
20	• Hexadecimal 18 in Relay Word row 3 changes to 10, indicating 87UC dropout.
21-22	• Hexadecimal 10 in Relay Word row 3 changes to 00, indicating dropout of the 87UB phase current unbalance element.
23-28	• Hexadecimal 07 in Relay Word row 1 changes to 02, indicating 50MD element and TTF bit dropout.
29-60	• Remainder of the event report shows the state of the protected breaker prior to MODTrip and Reset logic operation.

Event Summary, Event Report 4

Event type is shown as 86BFT because the relay asserted the 86BF TRIP output during the event. Mechanical and electrical operating times are not shown because the 52A input did not change state and no trip or close inputs were asserted.

Three-phase energy dissipated in the breaker during the first fourteen cycles of the event is 0.61 megajoules primary.

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SECTION 5: APPLICATIONS

BREAKER FAILURE RELAYING OVERVIEW

In an ideal situation, when a fault occurs on a power system, the system primary protection operates to remove the faulted equipment from service. Zones of protection are arranged to minimize service disruption when local primary protection operates. When local protection fails to clear a fault, backup protection clears the fault, sometimes removing more equipment from service than the primary protection would have during correct operation.

Both local and remote backup protection is available to the system protection engineer. Remote backup consists of overlapping, time-coordinated protection zones that can operate if a fault outside the instantaneous protection zone persists. Local backup protection uses redundant equipment that operates to clear a fault if primary protection fails. The extent of redundancy depends on the availability of resources and the importance of the load.

Breaker failure relaying is one form of local backup protection. Consider using breaker failure relaying instead of remote backup if any of the following conditions are true:

- Remote backup fault clearing time is greater than maximum allowed fault clearing time due to system stability or equipment damage considerations.
- Critical loads are lost due to remote fault clearing which can be maintained using local breaker failure relaying.
- Remote fault clearing is sequential, requiring the local fault contribution to be cleared before remote relaying can detect the fault.

If the breaker fails to clear a fault, all electrically adjacent breakers must be opened. This stops a continuing fault and interrupts current flow in the failed breaker. Figure 5.1 shows a basic breaker failure scheme. 62X and 62Y are breaker failure initiate inputs from the local primary and backup line protection. The 50 overcurrent element is set to pick up for very low current levels. This element should be immune to dc and exponentially decaying ramp currents and have a high dropout ratio, resetting quickly when the protected breaker opens. When the timer expires, it energizes the 86 lockout relay, which initiates local tripping of all electrically adjacent breakers. Optionally, the 86 lockout relay can initiate transfer tripping to clear electrically adjacent remote breakers.

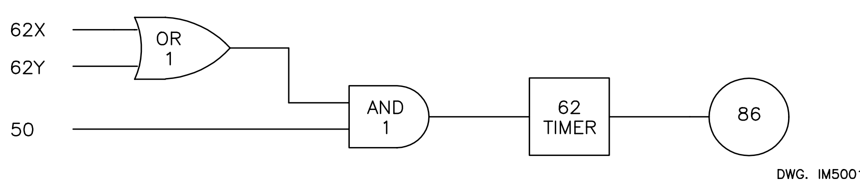

Figure 5.1: Basic Breaker Failure Protection Scheme

Time delay selection is important. Figure 5.2 illustrates the timing of the basic breaker failure scheme. Calculate an absolute maximum fault clearing time based upon system stability and equipment I^2t withstand considerations. In the event of a breaker failure, total time to clear all electrically adjacent breakers must be less than this absolute maximum. The 62 timer delay should be set to allow time for the protected breaker to operate and the 50 element to reset. Also, a short safety margin should be added. The amount of time available for a safety margin is limited by the operating time of the line protective relays and the local and remote breakers.

When the failed breaker is isolated by disconnect switches or removed from service for maintenance and testing, the breaker failure scheme should be disabled. This prevents inadvertent tripping of other breakers in service.

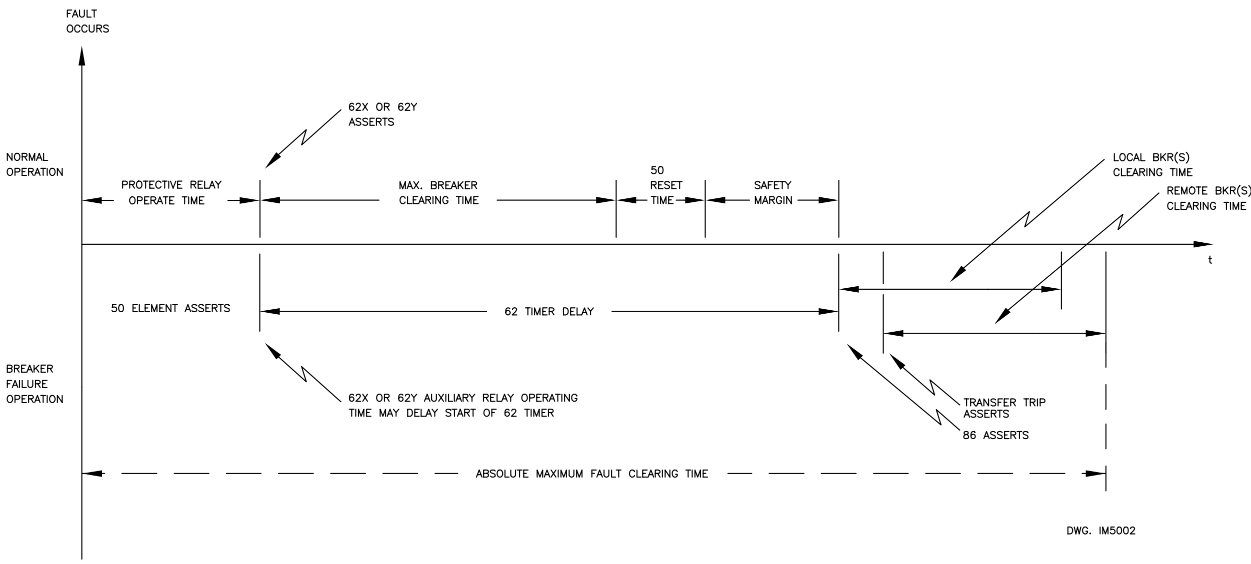

Figure 5.2: Basic Breaker Failure Scheme Timing

The breaker failure scheme discussed above protects the breaker and line equipment when the breaker fails to clear a fault. Other breaker failure modes include:

- Failure of breaker to trip load current
- Failure of breaker to open completely, leaving trip resistors in service
- Failure of breaker to close completely, leaving close resistors in service
- Failure of a breaker pole to close
- Pole flashover failure while breaker is open

You can enable the SEL-2BFR Relay to protect a breaker independently for each of these failure types, as shown below.

In ring-bus and breaker-and-a-half installations, two circuit breakers must operate to interrupt line current. Current distribution between the two breakers is unknown until the first breaker opens. The bulk of fault current initially may be carried by a single breaker. Both breakers receive the trip signal at the same time, but the 50FT element associated with the low current breaker may not assert until the other breaker opens. This causes an uncertainty with respect to the timing of 50FT element assertion. This uncertainty is not present in a single breaker arrangement. Timing uncertainty is accounted for in the SEL-2BFR Relay breaker protection schemes intended for these complex bus/breaker arrangements. The SEL-2BFR Relay is intended to protect a single breaker, regardless of the bus/breaker arrangement. In breaker-and-a-half and ring-bus arrangements, you must use an independent breaker failure relay for each breaker.

The SEL-2BFR Relay simplifies breaker failure protection schemes by combining the relay elements, timer, and logic in one small package. Panel space, wiring, and maintenance requirements are all reduced while reliability and simplicity are increased. Event reporting, remote setting and interrogation, and breaker monitoring functions add to the economy of the SEL-2BFR Relay.

SEL-2BFR Relay Application

This section contains setting calculations for an example SEL-2BFR Relay application. This information is presented so that you become familiar with the relay operation. Please select relay settings appropriate to your application.

Note: All six breaker fail schemes use the 50FT current element. This element is defined as a protection element and takes precedence over other tasks during the period of element assertion. In particular, the IRIG-B time synchronizing function will not be processed during this period. For 50FT element settings below load current (50FT element asserted during normal operating conditions) consider one of the load breaker fail schemes. Load current breaker fail schemes use the 50LD elements, and the IRIG-B time synchronizing function is unaffected.

Relay AC Current and Voltage Inputs

To effectively protect a power circuit breaker that includes tripping or closing resistors, the SEL-2BFR Relay must measure current flowing through each breaker pole and voltage drop across it. Figure 5.3 shows a single-phase of ac current and voltage inputs to the relay. The ac and dc connection diagrams for this example are included in the ***Typical AC/DC Connections*** subsection of ***Section 6: Installation***.

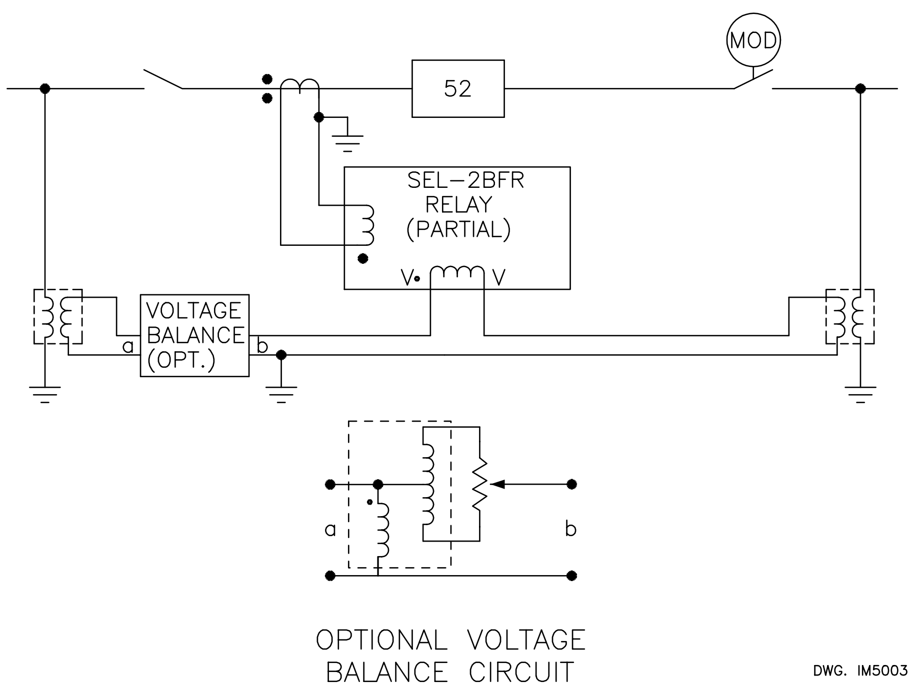

Figure 5.3: Single-Phase of AC Inputs to the Relay

Apply current to the relay from current transformers on each phase of the protected breaker. The relay calculates voltage drop across each phase breaker by measuring the difference in voltage between the secondaries of potential transformers connected on both sides of the protected breaker.

If the potential transformers on each side of the breaker do not have identical turns ratios, you must install a voltage balancing circuit between the secondary on one potential transformer and the voltage input to the relay. Figure 5.3 shows one circuit you can use to balance the input voltage.

If you do not wish to use voltage-based breaker protection features such as resistor thermal protection, flashover protection, and breaker voltage warning, you need not connect the voltage inputs.

Example Breaker

Figure 5.3 shows the example breaker arrangement. Table 5.1 lists pertinent breaker, line, and system information.

Table 5.1: Example Line/Breaker Information

System per-unit bases:	525 kV; 100 MVA; 2756 Ω; 110.0 A
Line length:	100 miles
Line impedances:	Z1 = Z2 = 0.0218 pu Z0 = 0.0758 pu
Source impedances:	ZS1 = 0.0034 pu ZS0 = 0.0055 pu
Three-pole tripping	
Zone 1, three-phase minimum fault duty:	I_{3ph} = 49.6 pu = 5456 A
Line charging current:	I_c = 350 A
CTR:	3000/5 (600/1)
PTR:	4300/1
Breaker:	Cogenel Type PK-8E (Air Blast) 500 kV, 3000 A, 3800 MVA
Maximum trip time:	2 cycles
Nominal close time:	10 cycles
Close resistors:	35 Ω/column, 2 columns
Trip resistors:	110 Ω/column, 2 columns
Transfer trip channel time:	0.5 cycle

Scheme Overview

The protection scheme in this example protects the breaker for all failures to trip. When fault current exceeds the minimum three-phase fault duty for a Zone 1 fault, the fault must be cleared in 8.5 cycles or less. All other trips must clear within 10 cycles. Because the protected breaker has trip and close resistors and three-phase potentials are available on both sides of the breaker, the example uses the SEL-2BFR Relay trip and close resistor thermal protection schemes. Breaker closure and pole flashover failures are covered. The MOD Trip logic automatically isolates the protected breaker in the event of breaker failure.

Setting Selection

Select Failure to Trip Fault Current Scheme

The SEL-2BFR Relay provides six different protection schemes for failure of the protected breaker to interrupt fault current. ***Logic Description*** in ***Section 2: Specifications*** provides logic diagrams and details regarding the operation of each scheme. Setting considerations for each of the six schemes are provided below. All six schemes are applicable to single-pole trip installations.

Table 5.2: Fault Current Scheme Setting Considerations

Scheme	Bus Configuration	Operating Considerations
1	Single, Breaker-and-a-Half, Ring-Bus	• 62TTpu setting is not used. • Set 62TTdo greater than worst case protected breaker operating time. • Set 62FC greater than 62TTdo by at least two cycles (relay logic requirement). • Trip input may be immediately deasserted.
2	Single Breaker	• 62TT timer settings are not used. • Set 62FC timer greater than local breaker operating time, plus 50FT reset time, plus a safety margin. • Trip input may be deasserted after 50FT element asserts.
3	Single Breaker	• 62TT timer settings are not used. • 62FC timer may be set without respect to 50FT element reset time if the trip input drops out when current no longer flows in the breaker. • Following initiation, trip input must remain asserted while current flows in the breaker.
4	Single, Breaker-and-a-Half, Ring-Bus	• 62FC timer setting is not used. • 62TT timer output asserts each time a trip input asserts. Setting should be greater than local breaker operating time, plus 50FT reset time, plus a safety margin. • 50FT setting must exceed maximum load current.

Scheme	Bus Configuration	Operating Considerations
5	Single, Breaker-and-a-Half, Ring-Bus	• 62TT timer settings are not used. • 62FC timer starts when trip is asserted. • Following initiation, trip input must remain asserted while current flows in the breaker.
6	Single, Breaker-and-a-Half, Ring Bus	• 62TT timer output asserts each time a trip input asserts. Setting should be greater than local breaker operating time plus a safety margin. 50FT reset time does not have to be taken into account. • 50FT setting must exceed maximum load current. • 62FC timer output asserts each time all three trip inputs assert. Setting should be greater than local breaker operating time, plus a safety margin. 50FT reset time does not have to be taken into account. • See Figure 2.7 and accompanying note in ***Section 2: Specifications***.

Additional timing considerations are listed in Table 5.3.

The timing diagrams shown below allow you to compare the timing of each breaker failure scheme to the basic scheme shown in Figure 5.2.

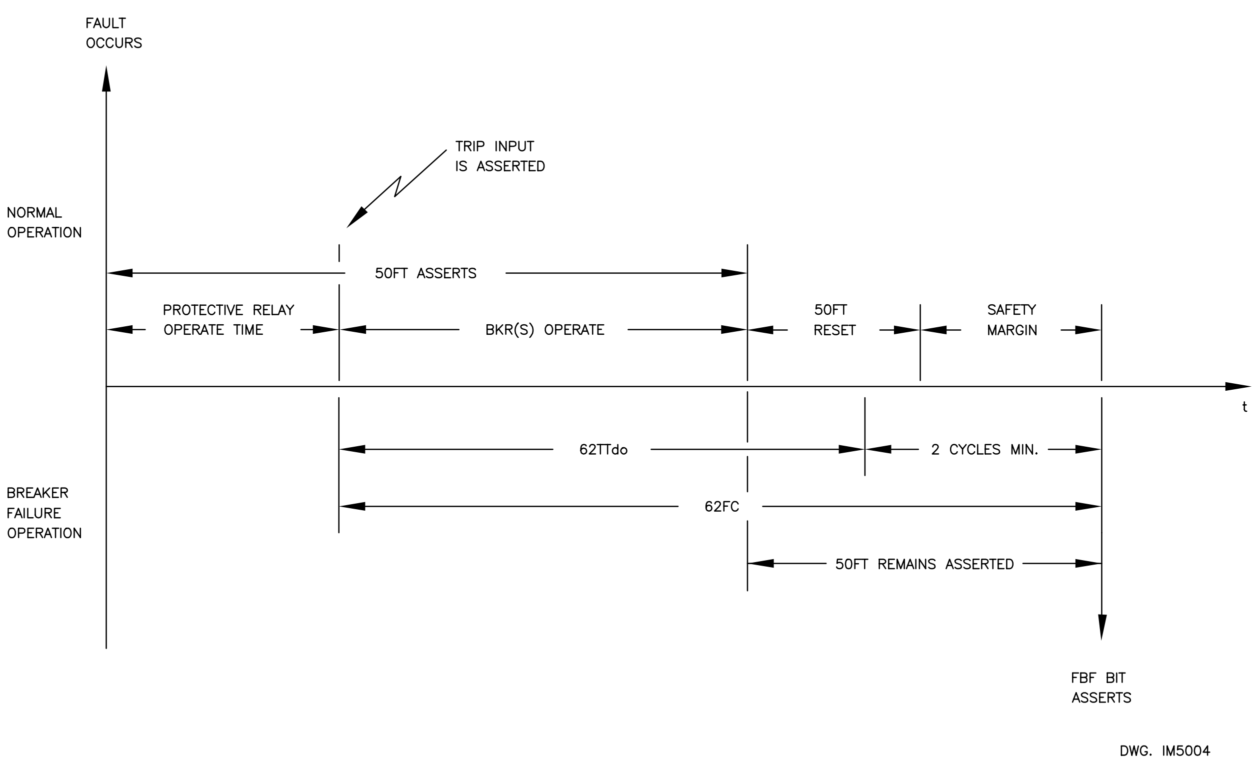

Figure 5.4: Scheme 1 Breaker Failure Timing

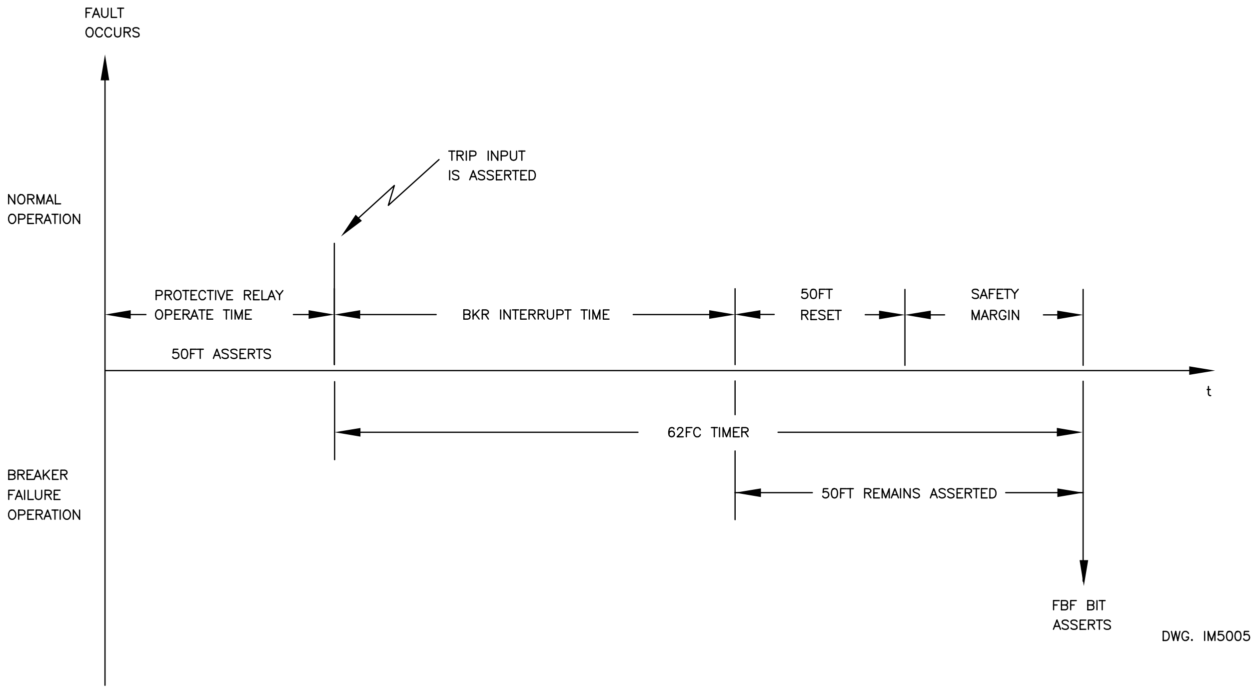

Figure 5.5: Scheme 2 Breaker Failure Timing

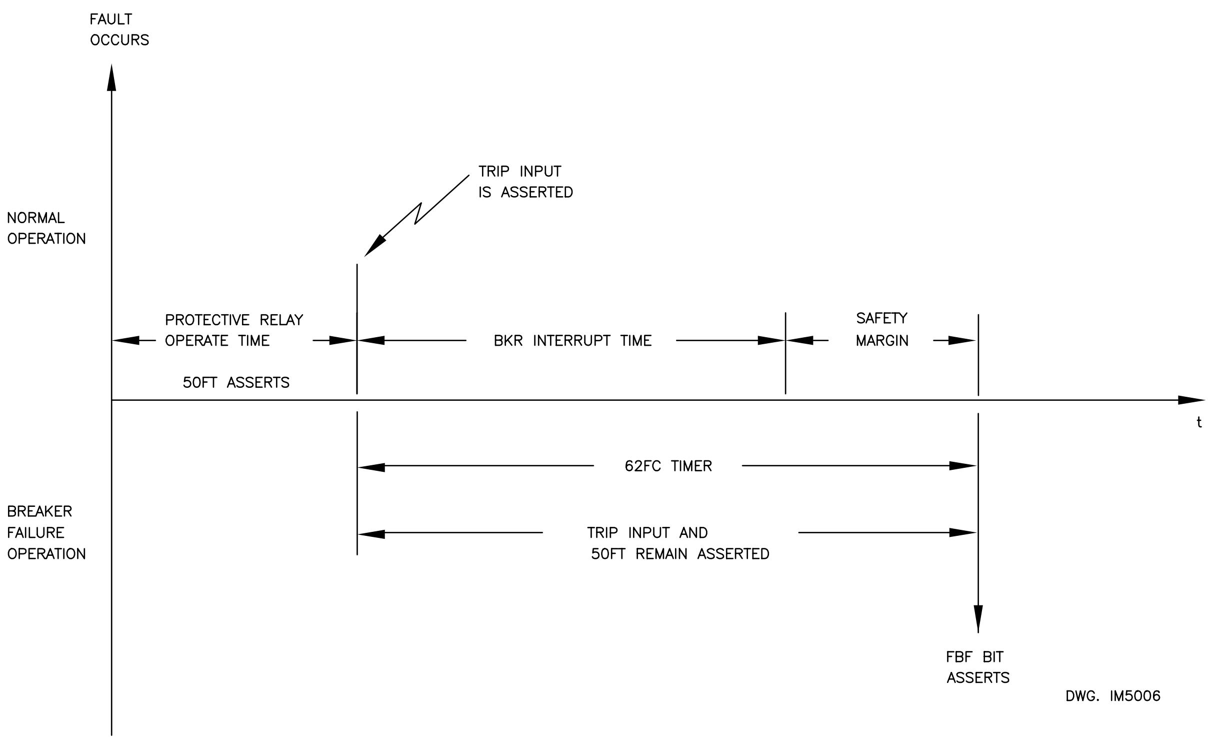

Figure 5.6: Scheme 3 Breaker Failure Timing

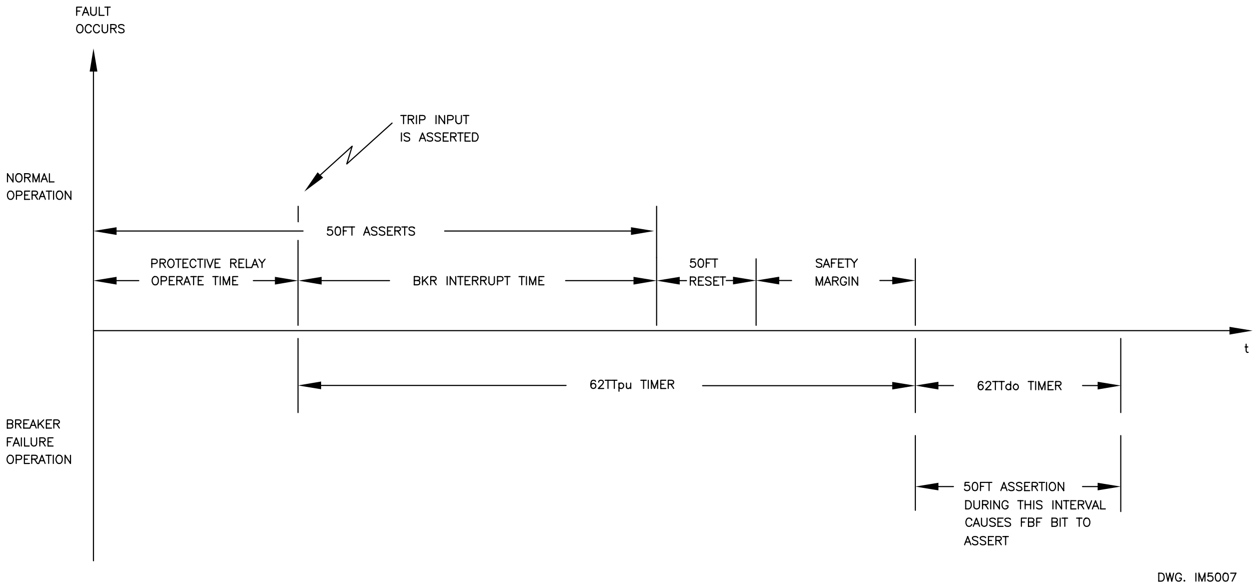

Figure 5.7: Scheme 4 Breaker Failure Timing

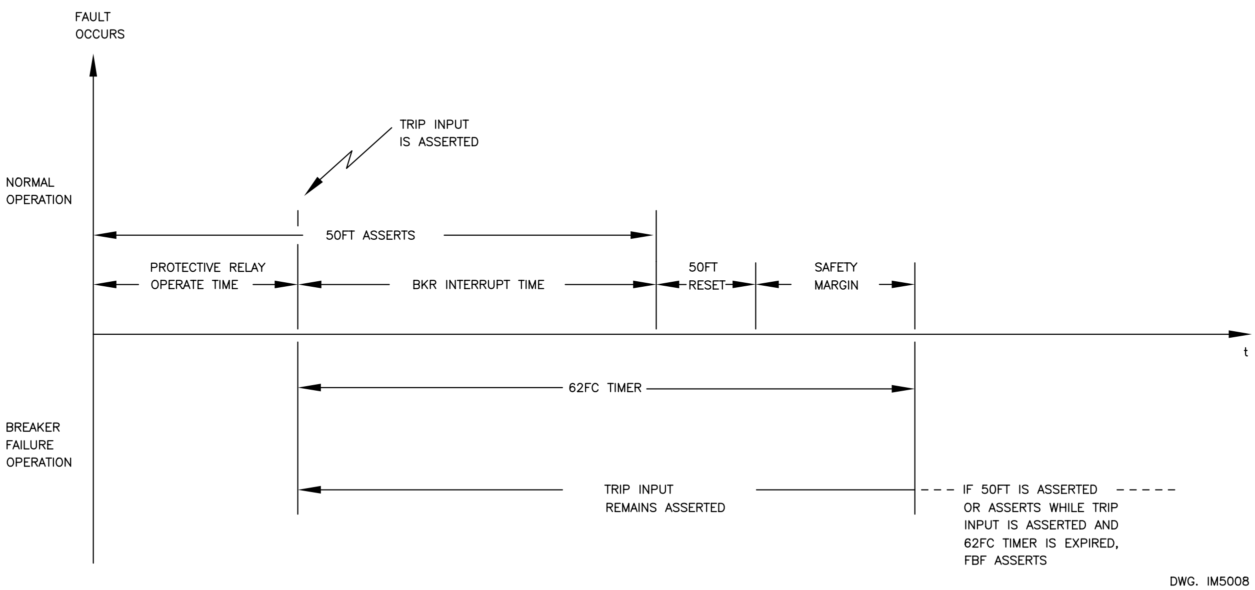

Figure 5.8: Scheme 5 Breaker Failure Timing

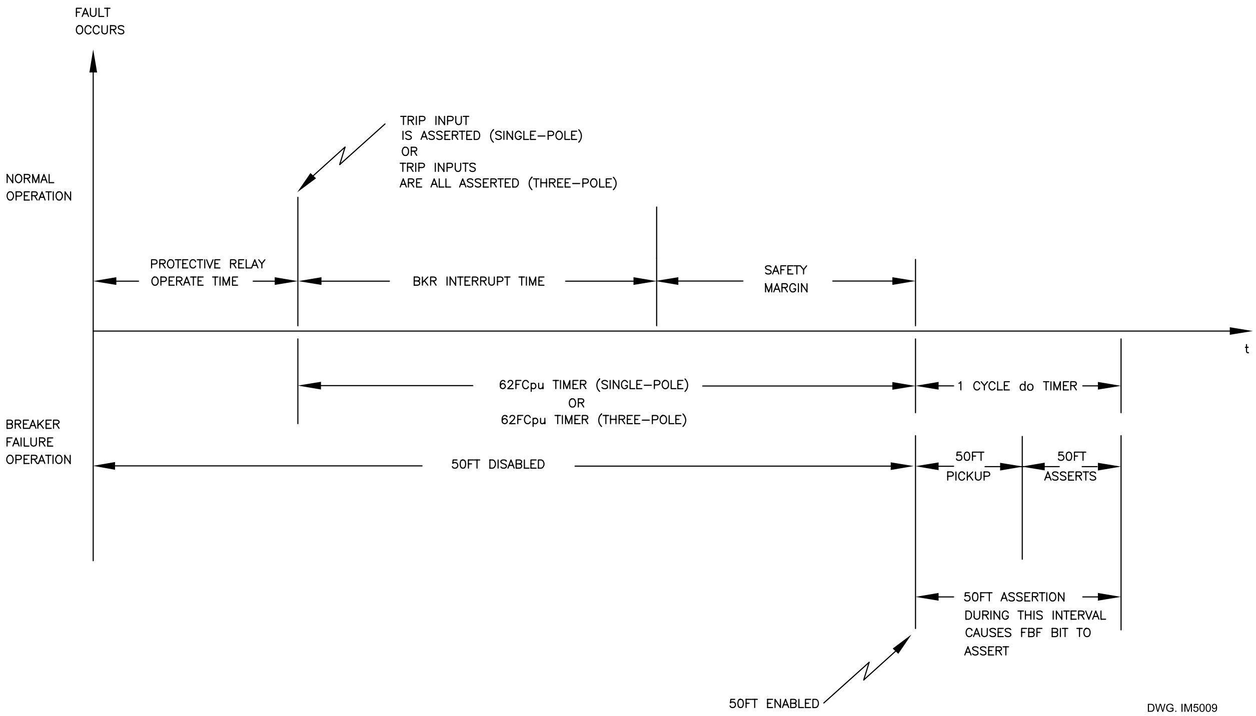

Figure 5.9: Scheme 6 Breaker Failure Timing

Select the best scheme for your application based upon the bus configuration of the protected breaker, operating considerations listed, and the timing shown above.

Because the example protected breaker is in a single breaker installation, any of the five available schemes may be used. We selected Scheme 2 based upon its simplicity and the fact that the trip input may be deasserted once the breaker failure scheme is initiated.

Select 50FT Overcurrent Element Setting

This setting selection is based upon the minimum fault duty for which the scheme is required to operate. The failure to trip fault current logic operates each time the breaker is called upon to trip phase current greater than the 50FT setting.

Note: The SEL-2BFR Relay does not discriminate between phase faults and ground faults. Fault discrimination is based strictly upon phase current magnitude. Breaker operations for ground faults with current duties above the 50FT setting are protected under the failure to break fault current logic.

For our example, system conditions require that Zone 1, three-phase faults must be cleared by the fault current breaker protection scheme if the protected breaker fails. All other trips are protected using the load or line-charging current protection logic.

When you select the 50FT element setting, account for possible error in the current element measurement. By calculating the worst-case measurement error and subtracting that value from the relay setting, you ensure that the element operates for the current level specified by your protection scheme.

In the example, minimum Zone 1 three-phase fault duty, I_{3ph}, equals:

$$I_{3\,ph} = \frac{5456 \text{ A primary}}{600} = 9.09 \text{ A secondary}$$

The 50FT element accuracy specification is ±0.025 A secondary ±5% of setting. Thus the worst-case error for a setting of 9.09 A secondary is:

50FT error = 0.025 A + (0.05) • (9.09 A)

= 0.479 A secondary

To ensure that 50FT asserts for all Zone 1, three-phase faults, we set the 50FT element:

50FT = 9.09 A – 0.479 A = 8.61 A secondary

Note: If Scheme 6 is selected, the 50FT overcurrent element has a 12 percent transient overreach. This is due to the digital filter turning on suddenly after the 62TT or 62FC pickup timers time out and then turning off suddenly one cycle later. As an example, if setting 50FT = 8.00 A secondary and the current is 7 A secondary, when the 50FT overcurrent element is enabled (digital filter turned on), the 50FT overcurrent element can still pick up:

8 A secondary – [8 A secondary • (12% / 100%)] = 7 A secondary

In this case, even though setting 50FT = 8.00 A secondary, the 50FT overcurrent element can still pick up for 7 A secondary.

Select Scheme Timer Settings

Select the scheme timer settings based upon the following factors:

- Maximum permissible fault duration
- Protective relay operating time
- Protected breaker operating time
- 50FT element reset time, if required by the selected protection scheme
- Operating times of electrically adjacent breakers
- Desired breaker failure operating safety margin

If an auxiliary interposing relay is used between the line protective relay trip output and the trip input to the SEL-2BFR Relay, you must account for the operating time of the auxiliary relay as well. Be aware that different models of auxiliary relays have a wide variety of operating times. Most scheme operating considerations are listed in Table 5.2. Additional timing considerations are listed in Table 5.3 by scheme number.

Table 5.3: Scheme Timing Considerations

Scheme	Considerations
Schemes 1, 4, 5, and 6	In these schemes, the breaker failure timer starts independently from 50FT assertion. This independence allows scheme usage in bus configurations where the 50FT element may assert after trip input assertion, such as ring-bus and breaker-and-a-half bus arrangements.
Scheme 2	In Scheme 2, the 62FC timer does not start until both the trip input and 50FT element are asserted. This feature allows definite, predictable scheme timing in single-breaker configurations where the 50FT element asserts before the trip input.
Scheme 3	You can set the 62FC timer for this scheme independently of the 50FT element reset time if the trip input deasserts when current stops flowing in the protected breaker. The 62FC timer does not start until the phase trip input is asserted and the phase 50FT element asserts.
Scheme 4	The 62TTdo timer setting defines duration of the 62TT timer output pulse. The FBF bit asserts if the timer output is high and the phase 50FT element is asserted. The FBF bit deasserts when the 62TTdo timer expires, regardless of 50FT element state.
Scheme 6	The 50FT element reset (dropout) time is the sum of: the front-end analog filter dropout time (less than a quarter-cycle) the First Order Difference (FOD) digital filter dropout time (vast majority of the reset time) The digital filter is disabled while the 62TT or 62FC pickup timers are timing in Scheme 6. Thus, 50FT element reset time does not have to be taken into account as part of the safety margin incorporated into the 62TT and 62FC pickup time delay settings. Technically, the front-end analog filter dropout time should be taken into account in the safety margin, but this is less than a quarter-cycle. (See Figure 2.7 and accompanying note in ***Section 2: Specifications***.)

Note: 50FT element pickup and dropout time curves are found in the back of ***Section 2: Specifications***.

For the example application, all Zone 1, three-phase faults must be cleared within 8.5 cycles to maintain system stability. Thus, total fault clearing time, Tt, is 8.5 cycles. Nominal operating time of local breakers, Tbl, and remote breakers, Tbr, is two cycles. Transfer trip channel time to the remote breaker, Tc, is 0.5 cycles. Operating time of the line protective relay, Tpr, for a three-phase fault near the Zone 1 boundary is two cycles. Specified reset time of the 50FT overcurrent element, T50, is less than 1.10 cycles. Safety margin time, Ts, is defined:

Ts = Tt – (Tpr + Tbl + T50 + Tbr + Tc) cycles

Ts = 8.5 – (2.0 + 2.0 + 1.10 + 2.0 + 0.5) cycles

Ts = 0.90 cycles

You can now calculate 62FC using the following equation:

62FC = Tbl + T50 + Ts = 4.0 cycles

Select 50LD Overcurrent Element Setting

The 50LD overcurrent element is used in the failure to trip load current breaker protection scheme. The 50LD element should pick up when the protected breaker is closed. This scheme detects failures of the breaker to open when breaker current is lower than the 50FT setting, such as Zone 2 faults and load breaking operations.

If the protected breaker is in a ring-bus or breaker-and-a-half arrangement, set 50LD to pick up for line-charging current of the shortest line serviced by that breaker.

Charging current for a given line can be calculated using the equation:

$$I_c = Vg \bullet Bc \text{ A primary}$$

where Vg is the line-to-ground voltage and Bc is the line capacitive susceptance.

For the example application, line-charging current, I_c, is 350 A primary or 0.58 A secondary.

The 50LD element accuracy specification is ±0.025 A secondary ±5% of setting. The error figure is calculated with the method used for 50FT. The maximum error for a setting of 0.58 A secondary is ±0.054 A secondary. To ensure that 50LD picks up any time the protected breaker is closed, we set the 50LD element:

$$50LD = 0.58 \text{ A} - 0.054 \text{ A} = 0.53 \text{ A secondary}$$

The relay also uses the 50LD element in the flashover protection logic. If you intend to use the breaker pole flashover protection logic, please refer to the logic descriptions before finalizing your 50LD setting selection.

When the protected breaker is part of a ring-bus or breaker-and-a-half installation, load current may be very low due to unequal current distribution between the two breakers. Failure to trip load current logic may still be used to protect the breaker. Because current application may be sequential, there is an uncertainty in scheme timing when used in ring-bus or breaker-and-a-half installations. Scheme timing is discussed below.

Select 62LP and 62LD Settings

The 62LP and 62LD timers are breaker pending failure and failure timers for the failure to trip load current breaker protection scheme.

It may be acceptable to extend the time delay of this protection scheme due to lower current duties associated with this type of breaker failure operation. Extending the time delay allows more time for a slow but operative breaker to clear a low-current fault. A disadvantage in the extended time delay is that a fault does remain on longer if the breaker actually fails. These considerations must be weighed when selecting time delays for this scheme. Please note that some breakers actually take more time to break low amounts of current. Consult the manufacturer of the protected breaker for details.

The timing of this protection scheme is nearly identical to that shown in Figure 5.5. The difference is that pending failure bit, LPF, is provided with this scheme. Consider using the pending failure bit to retrip the protected breaker through a second trip coil.

In our example application, 10 cycles are allowed to clear faults with current duties below 5456 A primary. Local and remote breaker operating times are considered identical to those used in selecting the 62FC delay setting. Operating time of line protective relay, Tpr, is two cycles. Specified reset time of the 50LD overcurrent element, T50, is less than 1.55 cycles. Safety margin time is defined Ts and calculated below.

Ts = Tt – (Tpr + Tbl + T50 + Tbr + Tc) cycles

Ts = 10.0 – (2.0 + 2.0 + 1.55 + 2.0 + 0.5) cycles

Ts = 1.95 cycles

62LD = Tbl + T50 + Ts = 5.5 cycles

We set the pending failure timer, 62LP, to retrip the protected breaker more than two cycles before tripping the lockout relay:

62LP = 3.25 cycles

Select 52A Supervised Breaker Failure Protection Settings

If there are conditions under which the protected breaker could be called to trip while current is below the 50LD overcurrent element setting, you may wish to enable the 52A supervised breaker failure timers 62AP and 62AF. An application where this function might be required is when the protected circuit breaker is connected to a generator-transformer unit.

In this instance, the circuit breaker could be issued a trip signal while the generator is idling. Under these conditions, current through the protected breaker is nearly zero. You can set the SEL-2BFR Relay to operate the 86 lockout relay if the relay 52A input is not deasserted after a settable time delay.

In our example application, this logic is not used. The E62A setting is set equal to N.

The time delay settings should be selected based upon the maximum time permissible to operate the protected equipment under low- or zero-current conditions. A slightly larger safety margin should be considered for this logic than is allowed for the breaker failure timers described above. The longer safety margin can allow for possible differences in expected and actual breaker auxiliary contact operating times.

Select Time-Delayed Retrip Settings

In some applications, you may wish to retrip the protected breaker through a second trip coil, perhaps using a backup dc tripping supply. The SEL-2BFR Relay can issue the retrip signal instantaneously or with a short time delay. The time delay may be desirable to allow external sequential events recorders or SCADA remote terminal units to distinguish between issue of the initial trip and retrip signals.

To enable time-delayed retripping, set DRTE equal to Y. With this setting, the relay supervises assertion of the Relay Word trip bits TA, TB, and TC with each phase 50LD overcurrent element and a settable time delay, RTTD. The programmable logic mask settings used to control the relay outputs providing the retrip function are described near the end of this section.

Select an RTTD time delay long enough to allow your external event logging equipment to distinguish between the trip and retrip signals, but short enough to allow the breaker time to operate on the retrip signal. If the RTTD time delay is too long and the initial trip does not operate the breaker, the breaker may not have time to fully open on the retrip signal before the SEL-2BFR Relay operates the bus lockout relay. Time delays between two and six cycles are typical.

In our example application, the time-delayed retrip feature is not used. The DRTE setting is N. With this setting, the relay sets the Relay Word trip bits without time delay or overcurrent supervision, allowing instantaneous retrip to be used, if desired.

Select Trip and Close Resistor Thermal Element Settings

If the protected breaker is equipped with trip and close resistors and three-phase potentials are available on both sides of the breaker, you can use the relay thermal protective elements to protect breaker resistors. Occasionally, a trip or close resistor can be left in service following a breaker operation. The relay can detect that condition, model the energy accumulated in the resistor, and trip the protected breaker or 86 lockout relay when resistor energy reaches a preset level.

Operation of the thermal protection logic is described in ***Section 2: Specifications***. Setting selection is described below.

37OP Setting

Select a 37OP element setting such that the element asserts when the minimum line current is flowing through the minimum breaker resistance possible while resistors are in circuit. The 37OP element setting is based on single-phase power dissipated in any breaker pole.

The minimum breaker resistance with resistors in circuit is found when the trip and close resistors are inserted in parallel.

For the example breaker:

$$R_{TRIP} = 2 \bullet 110\,\Omega = 220\,\Omega$$

$$R_{CLOSE} = 2 \bullet 35\,\Omega = 70\,\Omega$$

$$R_{MIN} = \frac{220 \bullet 70}{220 + 70}\,\Omega \text{ primary}$$

$$= 53\,\Omega \text{ primary}$$

Line-charging current is 350 A primary, thus the minimum resistor in circuit voltage is:

$$V_{MIN} = \frac{350\text{A} \bullet 53\,\Omega}{4300} = 4.33\text{ V secondary}$$

Line-charging current times minimum resistor in circuit voltage across the breaker yields the minimum power for which 37OP should be required to assert.

$$P_{MIN} = \frac{350\text{ A}}{600} \bullet 4.33\text{ V} = 2.52\text{ W secondary}$$

Consider 37OP element accuracy when selecting a setting. Element accuracy is specified: 37OP ±2.25 mW ±10.25% of measured power, ±2.63% of measured voltage, ±9.45% of measured current. At 37OP pickup, the maximum error is calculated:

$$\begin{aligned}
\Delta P_{MIN} &= 2.25\text{ mW} \pm 10.25\% \bullet \left(P_{MIN}\right) \pm \left[2.63\% \bullet V_{MIN} \pm 9.45\% \bullet I_c\right] W \\
\Delta P_{MIN} &= 2.25\text{ mW} + 10.25\% \bullet \left(2.52\text{ W}\right) + \left[2.63\% \bullet 4.33 + 9.45\% \bullet 0.58\right] W \\
\Delta P_{MIN} &= 2.25\text{ mW} + 258\text{ mW} + 114\text{ mW} + 54.9\text{ mW} \\
\Delta P_{MIN} &= 429\text{ mW}
\end{aligned}$$

To ensure that the 37OP element asserts under minimum resistor in circuit power and maximum error conditions, we select a 37OP element setting:

37OP = 2.52 W – 0.429 W = 2.09 W secondary.

26TF and 26TP Thermal Element Settings

Next, calculate the energy capacity of the trip and close resistors. In the example breaker, the trip resistors consist of 88 ceramic disks, having a volume per disk of 225 cm^3 and a maximum thermal capacity of 700 Joules/cm^3. The maximum thermal stress per head is found:

$$TS_{MAX} = 88\text{ disks} \bullet 225\text{ cm}^3 \bullet 700\text{ J / cm}^3$$

$$TS_{MAX} = 13.86\text{ MJ primary per breaker pole}$$

$$TS_{SEC} = \frac{13.86\text{ MJ primary}}{\text{CTR} \bullet \text{PTR}} = 5.37\text{ J secondary}$$

Thermal failure settings should prevent a normal trip and close operation from adding enough energy to damage resistors after thermal failure elements assert. Setting the relay conservatively, we select the trip resistor fail energy, 26TF:

26TF = 85% • TS_{SEC} = 4.56 J secondary.

For the example, we select the trip resistor thermal pending failure element, 26TP, to assert when the thermal model reaches 75 percent of the 26TF value, or

26TP = 75% • 26TF = 3.42 J secondary.

Calculate close resistor energy capacity the same way. In the example breaker, the close resistors consist of 28 ceramic disks. Maximum thermal stress per head is calculated as follows:

$$TS_{MAX} = 28 \text{ disks} \bullet 225 \text{ cm}^3 \bullet 700 \text{ J/cm}^3$$

$$TS_{MAX} = 4.41 \text{ MJ primary per breaker pole}$$

$$TS_{SEC} = \frac{4.41 \text{ MJ primary}}{CTR \bullet PTR} = 1.71 \text{ J secondary}$$

$$26CF = 85\% \bullet TS_{SEC} = 1.45 \text{ J secondary}$$

$$26CP = 75\% \bullet 26CF = 1.09 \text{ J secondary}$$

47Q Negative-Sequence Overvoltage Element Setting

When the breaker is closed and a potential fuse blows, the relay measures voltage across the breaker pole. Because current is flowing and voltage is measured, the relay could begin to accumulate energy in a resistor that is not in service. To prevent this, the negative-sequence overvoltage element 47Q supervises close resistor thermal models. When the 47Q element asserts, the relay disables the close resistor thermal model. Set the 47Q element to assert when negative-sequence voltage is great enough to indicate a potential fuse operation.

While the 47Q element asserts during single-pole open intervals in single-pole trip installations, single-pole trip operations do not adversely affect the thermal models because current does not flow in the open pole.

Calculate the magnitude of negative-sequence voltage for given phase voltages using the following equation.

$$V2 = \frac{1}{3}\left(VA + a^2 VB + aVC\right)$$

$$\text{where: } a \equiv 1\angle 120^\circ \text{ and } a^2 \equiv 1\angle 240^\circ$$

When the A-phase potential fuse blows, the magnitude and angle of negative-sequence voltage presented to the relay is:

$$V2 = \frac{1}{3}\left[67\text{ V}\angle 0^\circ + 0\text{V}\angle\left(0^\circ + 240^\circ\right) + 0\text{V}\angle\left(0 + 120^\circ\right)\right]$$

$$= \frac{1}{3}\left[67\text{ V}\angle 0^\circ + 0\text{ V}\angle -120^\circ + 0\text{ V}\angle 120^\circ\right]$$

$$= 22.3\text{ V}\angle 0^\circ$$

The magnitude of V2 is the same when two potential fuses operate. The accuracy specification of 47Q is ±0.27 V secondary ±15% of setting, yielding a maximum error of 3.62 V for a 22.3 V setting, so:

47Q = 22.3 V – 3.62 V = 18.69 V secondary.

Do not make the 47Q setting too sensitive. After issuing the close signal, the relay continues to measure negative-sequence voltage until all three breaker poles close. If a single-pole close resistor remains in service, the relay measures a small amount of negative-sequence voltage. This amount should not be greater than the 47Q element setting or close resistor thermal elements may be restrained for an actual failure. Calculate the negative-sequence voltage present during a close resistor failure using the equations for V2 above.

62OP Time Delay Pickup Setting

The 62OP time delay pickup timer delays heating of the resistor thermal models for a settable time following 37OP element assertion. This time delay allows thermal elements to ride through switching transients produced by capacitively coupled voltage transformers (CCVT).

For the example protected breaker, we select a setting of:

62OP = 3 cycles.

CRTC and TRTC Resistor Cooling Time Constants

The relay continuously models breaker resistor cooling. Define the modeling rate by setting CRTC and TRTC, the close and trip resistor cooling time constant settings.

The circuit breaker manufacturer should be able to provide data regarding resistor cooling time constants. If not, you can calculate these constants as follows. Assume that cooling from 200°C to near ambient temperature takes four hours or three time constants (95 percent cooled). This implies a cooling time constant of:

$$\text{CRTC} = \frac{240\ \text{minutes}}{3} = 80\ \text{minutes}$$

For the example, 80-minute cooling time constants were selected for CRTC and TRTC.

If you select an inaccurate cooling time constant, the resistor energy models may not be realistic for some time after breaker operations. For instance, if the cooling time constant is too short, a breaker resistor may actually contain more energy than is modeled, making the pending failure and failure energy levels less conservative than intended.

Select Breaker Pole Flashover Settings

See ***Logic Description*** in ***Section 2: Specifications*** for a description of breaker pole flashover protection logic operation.

If possible, set the 59FO element just lower than the voltage measured across the breaker when resistors are left in service. This setting makes the flashover logic more secure during close operations.

For the example breaker, V_{MIN}, was calculated:

V_{MIN} = 4.33 V secondary

The accuracy specification of the 59FO element is ±0.09 V secondary ±5% of settings, so:

59FO maximum error = 0.09 V + (0.05) • 4.33 V

= 0.31 V secondary

To ensure that 59FO asserts when a resistor is stuck in service

59FO = 4.33 - 0.31 = 4.02 V secondary

Set flashover failure timer setting, 62FF, based on the disruptive effects of breaker flashover on load and generation equipment and system stability. Set the flashover pending failure timer setting, 62FP, shorter than 62FF.

For the example protected breaker:

62FP = 25 cycles

62FF = 30 cycles

Select Phase Discordance/Failure to Close Settings

87UB Unbalance Current Ratio

The 87UB setting defines the divisor the relay uses to determine whether an unbalance exists between the three-phase current magnitudes. Lower unbalance ratio settings make the relay more sensitive to current unbalance. An example follows.

Assume 87UB equals eight and one per-unit current flows in each breaker pole upon closure. If A-phase and B-phase breaker poles close while the C-phase pole remains open, the relay makes the following comparisons:

$$Ia = 1\,pu > \frac{|I_a| + |I_b| + |I_c|}{8}$$

$$Ia = 1\,pu > \frac{2\text{ per-unit current}}{8}$$

$$Ib = 1\,pu > \frac{2\text{ per-unit current}}{8}$$

$$Ic = 0\,pu < \frac{2\text{ per-unit current}}{8}$$

87UC asserts because C-phase current is less than the sum of phase current magnitudes divided by 87UB. C-phase current must rise above 0.25 per unit before 87UC drops out. If 87UB equals 64, 87UC drops out when C-phase current reaches 0.031 per unit. Thus, higher 87UB settings permit greater phase current unbalance.

For the example protected breaker, 87UB = 16.

62UC Time Delay Pickup Timer Setting

Set the 62UC timer slightly higher than the nominal closing time of the protected breaker. For the example breaker, assuming a closing time of 10 cycles, we select a setting:

62UC = 12 cycles

The additional two cycles allow for possible pole scatter upon closure.

62UF and 62UP Timer Settings

When you set failure and pending failure time delays, consider the disruptive effects of breaker phase discordance on load or generation equipment and system stability. There may be a limit to the amount of time the system can withstand single phasing when the breaker carries maximum load. Use a pending failure timer setting, 62UP, shorter than 62UF.

For the example protected breaker:

62UP = 50 cycles

62UF = 60 cycles

Select MOD Trip Logic Setting

Motor-operated disconnect switches are used to isolate a circuit breaker for maintenance or in the event of a failure. You can set the SEL-2BFR Relay to operate an MOD following a breaker failure. The protection scheme must meet several requirements before the MOD Trip logic is useful.

- The relay must be able to measure all current flowing in the MOD.
- The MOD must be equipped with a form “a” auxiliary contact to indicate status.

Logic Description in ***Section 2: Specifications*** provides operational descriptions of SEL-2BFR Relay MOD Trip logic. If you want the relay to operate a motor-operated disconnect switch automatically to isolate a failed breaker, set ModTrip to Y.

If you do not use an MOD on the protected breaker, consider using this logic to indicate a “Safe to Disconnect” condition for station personnel.

If you do not wish to use the MOD Trip logic, set ModTrip to N. Overcurrent and timer setting considerations for both schemes appear below.

MOD Trip Logic Enabled, ModTrip Equals Y

50MD Overcurrent Element Setting

Set the 50MD element to pick up when protected breaker current exceeds the MOD current break rating. If you use this logic to indicate a ‘Safe to Disconnect’ condition, set 50MD below the level appropriate for the application.

In the example application, we do not attempt to operate the MOD as long as current can be detected in the protected breaker. We select the minimum setting for 50MD.

50MD = 0.10 A secondary

The 50MD element accuracy specification is ±0.025 A secondary ±5% of setting. Thus, the maximum error for a setting of 0.10 A secondary is ±0.030 A secondary.

62M1 and 62M2 Timer Settings

Timing diagrams illustrating MOD Trip logic operation appear in ***Section 2: Specifications***. Consider setting the 62M1 timer slightly higher than maximum bus clearing time. Set 62M2 higher than the amount of time necessary for the MOD to open fully.

For the example application:

62M1 = 62M2 = 600 cycles

MOD Trip Logic Disabled, ModTrip Equals N

50MD Overcurrent Element Setting

Set the 50MD element to drop out when breaker current drops below a level that is safe to operate disconnect switches (either manual or motor operated). When you select this setting, consider the element accuracy specification and the minimum allowable setting specification.

62M1 Timer Setting

Section 2: Specifications includes timing diagrams that show MOD Trip logic operation. Consider setting the 62M1 timer slightly above the maximum bus clearing time. The 62M2 timer is not used when ModTrip = N.

Select CTR and PTR Settings

Current transformer ratio (CTR) selection for line protection is often based on the transmission line current carrying capability. CTR selections also determine the magnitude of secondary fault current presented to the relay.

It is desirable to keep secondary CT currents between 50 and 100 A during maximum short circuit conditions. This reduces the likelihood of CT saturation and allows the current transformer to deliver a reliable secondary representation of the primary current during a fault condition.

The example protected breaker is equipped with a multiratio current transformer. The SEL-2BFR Relay is connected to the 3000:5 (600:1) tap, thus CTR = 600.

Select the potential transformer ratio (PTR) setting to match the primary voltage ratio (l-n) to approximately 70 $V_{l\text{-}n}$. Potentials are provided to the SEL-2BFR Relay from potential transformers on both sides of the protected breaker, each having ratios 4300:1.

The SEL-2BFR Relay uses the CTR and PTR settings in the **METER** command function to display voltage and current magnitudes in primary units. The settings should be in per unit, thus a CT ratio of 3000:5 (600:1) yields a CTR setting of 600.

Select Breaker Monitor Settings Topen, Tclose, Vwarn

The SEL-2BFR Relay uses these settings to generate alarms when operation of the protected breaker is outside these setting limits. If breaker operating time is greater than Topen or Tclose, the relay asserts Relay Word bit ALRM and stores an appropriate message in the alarm buffer.

If the relay measures voltage across the breaker that exceeds the Vwarn setting while 50LD is picked up, the relay asserts Relay Word bit ALRM and stores an appropriate message in the alarm buffer.

The example protected breaker uses the following settings:

Topen = 2.25 cycles

Tclose = 10.25 cycles

Vwarn = 0.5 volts secondary

Select Serial Port Timeout Settings TIME1 and TIME2

TIME1 and TIME2 settings specify the period of inactivity allowed before the relay automatically returns the port to Access Level 0. In this example, a modem is connected to PORT 1. Provide a definite-time setting for the port to prevent accumulation of toll charges when an operator does not hang up.

The relay allows TIME1 and TIME2 settings of 0–30 minutes. A TIME setting of zero prevents the relay from returning a port to Access Level 0 and simplifies relay access during testing.

In this example, TIME1 = 5 minutes, TIME2 = 0 minutes.

Select the Autoport Setting AUTO

AUTO specifies the port to which the relay sends automatically generated messages. If a port is timed out (see TIME1 and TIME2 settings), the relay does not send automatic messages to that port, even if the port is selected by the AUTO setting.

The relay can send automatic messages to PORT 1 only (AUTO = 1), PORT 2 only (AUTO = 2), or both ports (AUTO = 3). For the example protected breaker, AUTO = 2.

Select the External Modem Answer Setting RINGS

RINGS specifies the number of rings an auto-answer modem connected to PORT 1 waits before answering. This permits use of one substation telephone line by substation personnel and the relay. In this example, personnel have seven rings to answer the substation telephone before the modem answers (RINGS = 7).

You can set RINGS between 1 and 30.

If you do not use an external modem with the SEL-2BFR Relay, set RINGS to any value within range.

Example Setting Summary

The following is a summary of the relay settings used for this example. Please note that while the TTpu and TTdo settings are not zero, the relay ignores the settings and does not use them in failure to trip fault current Scheme 2.

Example Setting Group

```
Schm = 2        50FT   = 8.60     TTpu  = 6.00     TTdo    = 2.00     62FC = 4.00
50LD = 0.52     62LD   = 5.50     62LP  = 3.25
62AP = 5.25     62AF   = 7.50     E62A  =N         DRTE    = N        RTTD = 2.00
37OP = 2.09     26CF   = 1.45     26CP  = 1.09     26TF    = 4.56     26TP = 3.42
47Q  = 18.70    62OP   = 3.00     CRTC  = 80       TRTC    = 80
59FO = 4.01     62FF   = 30.00    62FP  = 25.00
87UB = 16       62UC   = 12.00    62UF  = 60.00    62UP    = 50.00
50MD = 0.10     62M1   = 600.00   62M2  = 600.00   ModTrip= Y
CTR  = 600      PTR    = 4300
Topen= 2.25     Tclose= 10.25     Vwarn = 0.47
TIME1= 5        TIME2 = 0         AUTO  = 2        RINGS  = 3
```

Note: The SEL-2BFR-2 Relay includes the RTSD setting (not shown).

Logic Mask Setting Selection

Section 2: Specifications explains the operational concept of programmable logic masks used in the SEL-2BFR Relay. Example logic mask settings below are provided to illustrate relay function and application. Please select logic mask settings particular to your application.

Figure 5.10 and Figure 5.11 show dc connections to the relay for this example protection scheme. When you use the relay in a single-pole tripping scheme, consider wiring single-pole breaker auxiliary contacts in series for connection to the SEL-2BFR Relay 52a inputs.

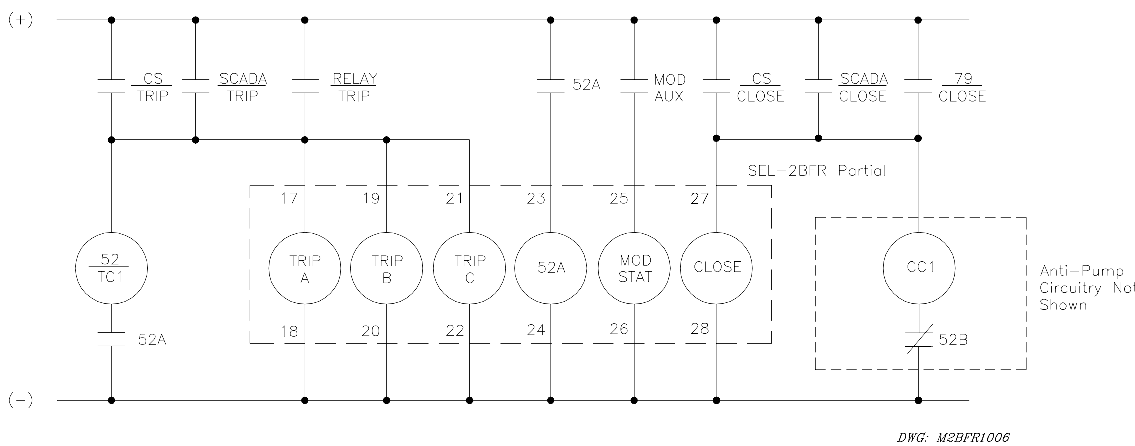

Figure 5.10: Example DC Input Connections

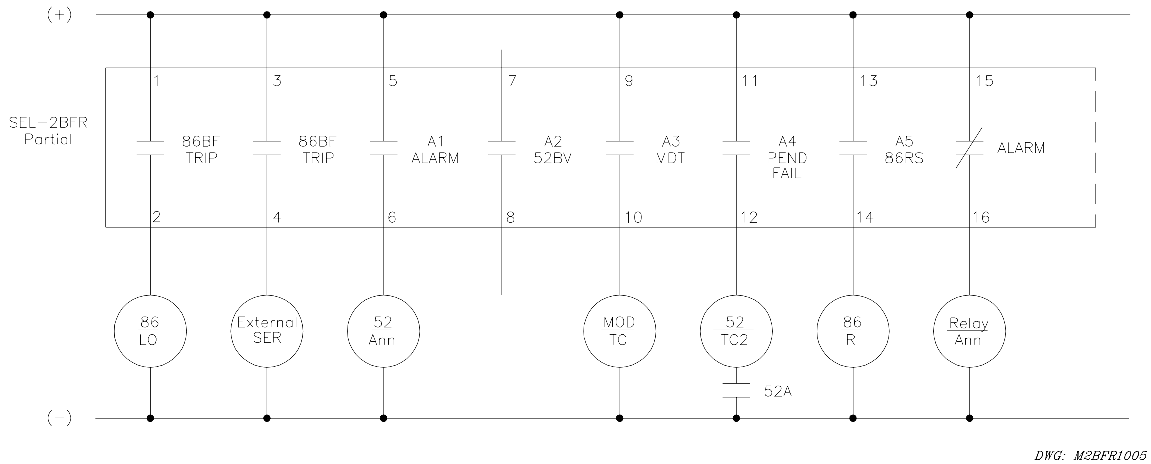

Figure 5.11: Example Contact Output Connections

M86T Mask Controls the 86BF TRIP Output

Use the 86BF TRIP output contacts to assert the 86 lockout relay when the SEL-2BFR Relay detects a breaker failure. Example logic mask settings appear below.

Logic Mask M86T

```
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF
 1    1    0    0    0    0    0    1
FOBF FOPF 59FO 59H  ALRM TC   TB   TA
 1    0    0    0    0    0    0    0
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF
 1    0    0    0    0    0    0    1
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB
 0    0    0    0    0    0    0    0
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q
 0    0    0    0    0    0    0    0
```

These settings cause the 86BF TRIP output contacts to close when one of the following occurs: failure to trip fault current (FBF), trip resistor thermal failure (TTF), failure to trip load current (LBF), breaker pole flashover failure (FOBF), phase discordance breaker failure (PDBF), or close resistor thermal failure (CTF).

MER Logic Mask Triggers Event Report Generation

Elements in the MER logic mask trigger event report generation upon assertion. The MER logic mask includes the full Relay Word plus input and output contact states. You can set the relay to trigger an event report for assertion of any input or Relay Word element. You can set the relay to trigger an event report for assertion of any output contact except ALARM.

Logic Mask MER

```
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF
 0    0    1    0    0    0    0    0
FOBF FOPF 59FO 59H  ALRM TC   TB   TA
 0    1    0    0    0    0    0    0
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF
 0    1    0    0    0    0    1    0
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB
 0    1    0    1    0    1    0    1
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q
 0    1    0    1    1    1    1    1
 *   86BF  A1   A2   A3   A4   A5 ALARM
 0    0    0    0    0    0    0    0
 *    *   CLOS MOD   52A  TPC  TPB  TPA
 0    0    0    0    0    1    1    1
```

These settings cause the relay to generate an event report when any breaker pending failure occurs, any delayed overpower element asserts, the MOD Trip (MDT) bit asserts, or any trip input is asserted.

MA1 Mask Controls the A1 Output, Breaker Operation Alarms

The MA1 logic mask is set with the ALRM bit only. With this setting, the A1 contact closes for one second when a breaker operation alarm occurs. These alarm conditions are defined in ***Section 2: Specifications***.

Logic Mask MA1

```
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF
 0    0    0    0    0    0    0    0
FOBF FOPF 59FO 59H  ALRM TC   TB   TA
 0    0    0    0    1    0    0    0
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF
 0    0    0    0    0    0    0    0
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB
 0    0    0    0    0    0    0    0
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q
 0    0    0    0    0    0    0    0
```

MA2 Controls the A2 Output, 52BV Verified Breaker Status

The MA2 logic mask contains the 52BV Relay Word bit. 52BV provides current verified breaker status. You can use this output to supervise breaker closing operations or monitor the 52a signal.

Logic Mask MA2

```
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF
 0    0    0    0    0    0    1    0
FOBF FOPF 59FO 59H  ALRM TC   TB   TA
 0    0    0    0    0    0    0    0
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF
 0    0    0    0    0    0    0    0
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB
 0    0    0    0    0    0    0    0
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q
 0    0    0    0    0    0    0    0
```

MA3 Controls the A3 Output, MOD Trip

The example application uses A3 contact assertion to trip the motor-operated disconnect switch following a breaker failure operation.

Logic Mask MA3

```
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF
 0    0    0    0    0    0    0    0
FOBF FOPF 59FO 59H  ALRM TC   TB   TA
 0    0    0    0    0    0    0    0
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF
 0    0    0    0    0    0    1    0
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB
 0    0    0    0    0    0    0    0
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q
 0    0    0    0    0    0    0    0
```

MA4 Controls the A4 Output, Pending Failure Retrip

In the example application, the A4 output contact is wired to assert a second trip coil on the protected breaker. Various protective element pending failure output bits are set in this mask. When a pending failure occurs, the A4 contact asserts the second trip coil in an attempt to open the breaker before the 86 lockout relay is asserted by the SEL-2BFR Relay 86BF Trip output.

Logic Mask MA4

```
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF
 0    0    1    0    0    0    0    0
FOBF FOPF 59FO 59H  ALRM TC   TB   TA
 0    1    0    0    0    0    0    0
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF
 0    1    0    0    0    0    0    0
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB
 0    1    0    1    0    1    0    1
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q
 0    1    0    1    0    0    0    0
```

MA5 Controls the A5 Output, 86BF Reset

You can set the SEL-2BFR Relay to automatically reset the 86 lockout relay following a breaker failure operation. ***Section 2: Specifications*** describes the 86BF Reset logic. The A5 mask contains the 86RS bit.

Logic Mask MA5

```
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF
 0    0    0    0    0    0    0    0
FOBF FOPF 59FO 59H  ALRM TC   TB   TA
 0    0    0    0    0    0    0    0
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF
 0    0    0    0    0    1    0    0
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB
 0    0    0    0    0    0    0    0
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q
 0    0    0    0    0    0    0    0
```

Other Programmable Output Applications

The versatility of programmable output contacts allows you to perform many tasks not detailed above. The following examples describe additional programmable output contact applications using the SEL-2BFR Relay.

Three-Pole Instantaneous or Time-Delayed Retrip

You may use a programmable output contact to perform instantaneous or time-delayed retrip of the protected circuit breaker. Set a single programmable logic mask with TA, TB, and TC equal to one. Connect that contact in series with a breaker 52A contact and Breaker Trip coil #2 as shown in Figure 5.12. We show the A1 contact in the example, but you can choose any contact between A1 and A5 to perform this function.

With this arrangement, each time any Relay Word trip bit TA, TB, or TC asserts, the relay asserts the A1 contact, energizing the second breaker trip coil. The trip bits assert instantaneously following assertion of a relay trip input when the DRTE setting equals N. The trip bits assert with a settable time delay and overcurrent element supervision when the DRTE setting equals Y.

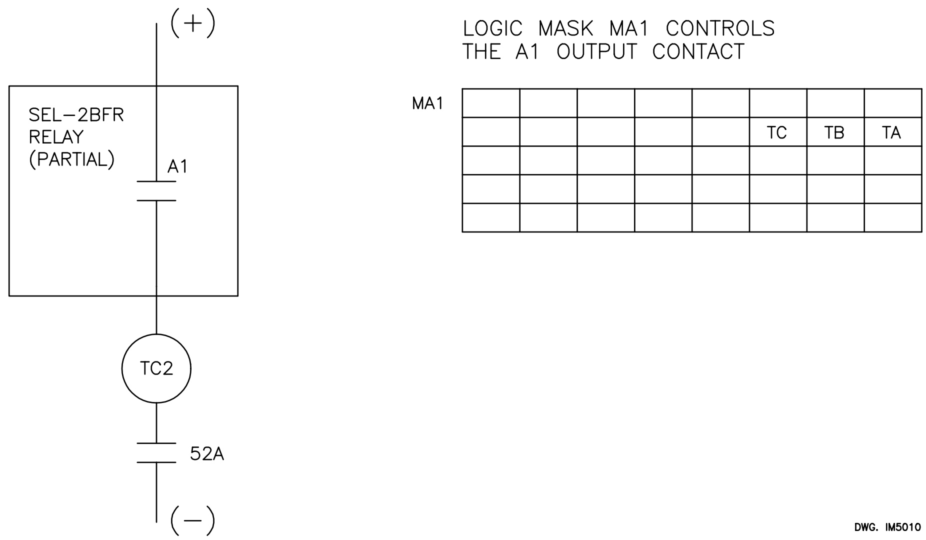

Figure 5.12: Three-Pole Instantaneous Retrip Using the A1 Output Contact

Single-Pole Instantaneous or Time-Delayed Retrip

You may use three programmable output contacts to perform single-pole instantaneous or time-delayed retrip of the protected circuit breaker. In this application, set three individual programmable output contacts to close when a single breaker trip input is asserted. For instance, MA1 could contain just the TA bit, MA2 just the TB bit, and MA3 just the TC bit. Then connect each contact in series with the appropriate 52a contact and single-pole trip coil as shown in Figure 5.13.

With this arrangement, each time a single-phase trip bit asserts, the relay asserts the corresponding programmable output contact, energizing the second trip coil and retripping the protected breaker pole. The trip bits assert instantaneously following assertion of a relay trip input when the DRTE setting equals N. The trip bits assert with a settable time delay and overcurrent element supervision when the DRTE setting equals Y.

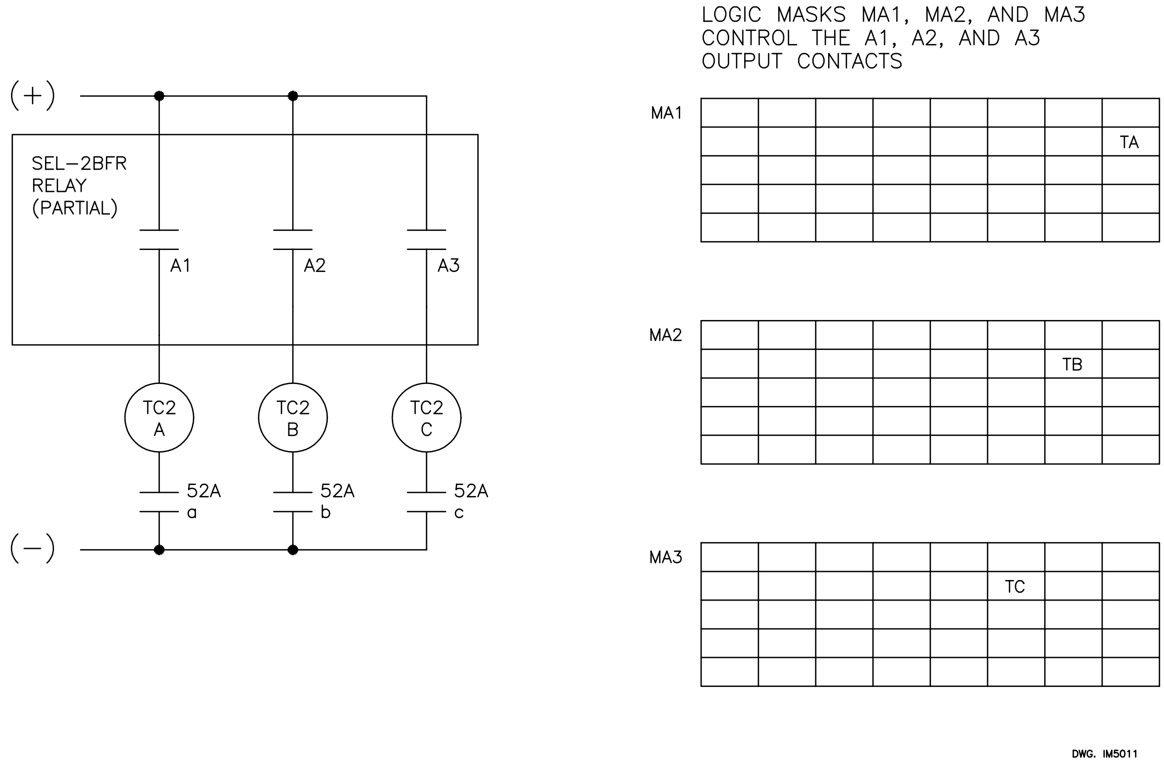

Figure 5.13: Single-Pole Instantaneous Retrip Using the A1, A2, and A3 Contacts

Loss-of-Potential Indication

In three-pole trip installations, the 47Q element asserts to indicate that a potential fuse has blown. Set 47Q in a programmable output contact logic mask and monitor that contact externally using an annunciator input, indicator lamp, or sequential events recorder input. When 47Q asserts, the programmable output contact closes, indicating a blown potential fuse.

In single-pole trip installations, you may use the 47Q element in the same manner. However, because the element may assert during single-pole-open intervals, you may want to use a time-delayed pickup timer between the relay output contact and the annunciator input or indicator lamp. The time delay should be set longer than the maximum single-pole-open interval. Thus, only permanent output contact closures activate the annunciator.

Hot Resistor Indication

When you use the SEL-2BFR Relay breaker resistor thermal protection elements, you can set a programmable output contact to close, indicating when one or more breaker resistor thermal models contain energy above the pending failure or failure level.

Set a programmable output contact mask with the appropriate trip and close resistor thermal failure or pending failure bits. The relay asserts the contact whenever the programmed bits assert. You can monitor the contact using an annunciator input, indicator lamp, or sequential events recorder input.

SETTINGS SHEET FOR THE SEL-2BFR RELAY

Binary-Hexadecimal Conversion Chart			
Binary	Hexadecimal	Binary	Hexadecimal
0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	B
0100	4	1100	C
0101	5	1101	D
0110	6	1110	E
0111	7	1111	F

Logic Mask Settings (LOGIC Command)

MASK: M86T (Trip)									Hexadecimal Setting
ROW #1: Relay Word Binary Representation	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF	
ROW #2: Relay Word Binary Representation	FOBF	FOPF	59F0	59H	ALRM	TC	TB	TA	
ROW #3: Relay Word Binary Representation	PDBF	PDPF	87UA	87UB	87UC	86RS	MTD	CTF	
ROW #4: Relay Word Binary Representation	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB	
ROW #5: Relay Word Binary Representation	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q	

MASK: MA1 (A1 Contact)									Hexadecimal Setting
ROW #1: Relay Word Binary Representation	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF	
ROW #2: Relay Word Binary Representation	FOBF	FOPF	59F0	59H	ALRM	TC	TB	TA	
ROW #3: Relay Word Binary Representation	PDBF	PDPF	87UA	87UB	87UC	86RS	MTD	CTF	
ROW #4: Relay Word Binary Representation	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB	
ROW #5: Relay Word Binary Representation	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q	

SETTINGS SHEET FOR THE SEL-2BFR RELAY

MASK: MA2 (A2 Contact)									Hexadecimal Setting
ROW #1: Relay Word Binary Representation	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF	
ROW #2: Relay Word Binary Representation	FOBF	FOPF	59F0	59H	ALRM	TC	TB	TA	
ROW #3: Relay Word Binary Representation	PDBF	PDPF	87UA	87UB	87UC	86RS	MTD	CTF	
ROW #4: Relay Word Binary Representation	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB	
ROW #5: Relay Word Binary Representation	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q	

MASK: MA3 (A3 Contact)									Hexadecimal Setting
ROW #1: Relay Word Binary Representation	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF	
ROW #2: Relay Word Binary Representation	FOBF	FOPF	59F0	59H	ALRM	TC	TB	TA	
ROW #3: Relay Word Binary Representation	PDBF	PDPF	87UA	87UB	87UC	86RS	MTD	CTF	
ROW #4: Relay Word Binary Representation	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB	
ROW #5: Relay Word Binary Representation	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q	

MASK: MA4 (A4 Contact)									Hexadecimal Setting
ROW #1: Relay Word Binary Representation	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF	
ROW #2: Relay Word Binary Representation	FOBF	FOPF	59F0	59H	ALRM	TC	TB	TA	
ROW #3: Relay Word Binary Representation	PDBF	PDPF	87UA	87UB	87UC	86RS	MTD	CTF	
ROW #4: Relay Word Binary Representation	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB	
ROW #5: Relay Word Binary Representation	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q	

MASK: MA5 (A5 Contact)									Hexadecimal Setting
ROW #1: Relay Word Binary Representation	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF	
ROW #2: Relay Word Binary Representation	FOBF	FOPF	59F0	59H	ALRM	TC	TB	TA	
ROW #3: Relay Word Binary Representation	PDBF	PDPF	87UA	87UB	87UC	86RS	MTD	CTF	
ROW #4: Relay Word Binary Representation	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB	
ROW #5: Relay Word Binary Representation	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q	

MASK: MER (Event Report Trigger)									Hexadecimal Setting
ROW #1: Relay Word Binary Representation	FBF	LBF	LPF	50FT	50LD	50MD	52BV	TTF	
ROW #2: Relay Word Binary Representation	FOBF	FOPF	59F0	59H	ALRM	TC	TB	TA	
ROW #3: Relay Word Binary Representation	PDBF	PDPF	87UA	87UB	87UC	86RS	MTD	CTF	
ROW #4: Relay Word Binary Representation	CRFA	CRPA	TRFA	TRPA	CRFB	CRPB	TRFB	TRPB	
ROW #5: Relay Word Binary Representation	CRFC	CRPC	TRFC	TRPC	DOPA	DOPB	DOPC	47Q	
ROW #6: Relay Word Binary Representation	X	86BF	A1	A2	A3	A4	A5	ALARM X	
ROW #7: Relay Word Binary Representation	X	X	CLOS	MOD	52A	TPC	TPB	TPA	

Settings Increment Chart	
Amps	in .01 steps
Cycles	in .25 steps
Volts	in .01 steps
Joules	in .01 steps
Watts	in .01 steps

Relay Settings (SET Command)

Relay Settings[1]

Description	Range			
Relay ID	Up to 39 characters	**ID**	=	________
Fault Failure Detection Scheme	1-6	**Schm**	=	________
Fault Current Detector	0.50-45.00 Amps (5 Amp model) 0.10-9.0 Amps (1 Amp model)	**50FT**	=	________
62TT Time Delay Pickup	0.25-63.75 cycles	**TTpu**	=	________
62TT Time Delay Dropout	0.25-63.75 cycles	**TTdo**	=	________
62FC Time Delay Pickup	0.25-63.75 cycles	**62FC**	=	________
Load or Line-Charging Current Detector	0.10-45.00 Amps (5 Amp) 0.02-9.0 Amps (1 Amp)	**50LD**	=	________
62LD Time Delay Pickup	0.25-63.75 cycles	**62LD**	=	________
62LP Time Delay Pickup	0.25-63.75 cycles	**62LP**	=	________
Breaker Auxiliary Pending Failure Timer	0.25-63.75 cycles	**62AP**	=	________
Breaker Auxiliary Failure Timer	0.25-63.75 cycles	**62AF**	=	________
Enable Breaker Auxiliary Failure Logic	Y or N	**E62A**	=	________
Delayed Retrip Enable	Y or N	**DRTE**	=	________
Retrip Seal-in Delay (2BFR-2)	0.25-63.75 cycles	**RTSD**[2]	=	________
Delayed Retrip Time Delay	0.25-63.75 cycles	**RTTD**	=	________
Breaker Resistor Single-phase Overpower	0.10-3400 Watts (5 Amp) 0.02-680 Watts (1 Amp)	**37OP**	=	________
Close Resistor Fail Energy	0.01-1000 Joules (5 Amp) 0.002 - 200.0 Joules (1 Amp)	**26CF**	=	________
Close Resistor Pending Fail Energy	0.01-1000 Joules (5 Amp) 0.002 - 200.0 Joules (1 Amp)	**26CP**	=	________
Trip Resistor Fail Energy	0.01-1000 Joules (5 Amp) 0.002 - 200.0 Joules (1 Amp)	**26TF**	=	________
Trip Resistor Pending Fail Energy	0.01-1000 Joules (5 Amp) 0.002 - 200.0 Joules (1 Amp)	**26TP**	=	________
Negative-Sequence Overvoltage	2.00-170.00 Volts	**47Q**	=	________
Thermal Element Time Delay Pickup	0.25-63.75 cycles	**62OP**	=	________
Close Resistor Cooling Time Constant	1.00-1140.00 min.	**CRTC**	=	________
Trip Resistor Cooling Time Constant	1.00-1140.00 min.	**TRTC**	=	________

[1] Amps, Volts, and Joules are set in secondary quantities.

[2] This setting is available only in the 2BFR-2 Version.

Relay Settings[1] (continued)

Description	Range			
Flashover Voltage Detector	1.00-67.00 Volts	**59FO**	=	________
62FF Time Delay Pickup	0.25-63.75 cycles	**62FF**	=	________
62FP Time Delay Pickup	0.25-63.75 cycles	**62FP**	=	________
Phase Current Magnitude Unbalance Ratio	8, 16, 32, 64	**87UB**	=	________
62UC Time Delay Pickup	0.25-63.75 cycles	**62UC**	=	________
62UF Time Delay Pickup	0.25-63.75 cycles	**62UF**	=	________
62UP Time Delay Pickup	0.25-63.75 cycles	**62UP**	=	________
MOD Operate Current	0.10-45.00 Amps (5 Amp) 0.02-9.0 Amps (1 Amp)	**50MD**	=	________
86BF Reset Timer M1 TDPU	0.25-16,383.75 cycles	**62M1**	=	________
86BF Reset Timer M2 TDPU	0.25-16,383.75 cycles	**62M2**	=	________
Enable MOD Trip Logic	Y-N	**ModTrip**	=	________
Per Unit Current Transformer Ratio	1-10,000	**CTR**	=	________
Per Unit Potential Transformer Ratio	1-10,000	**PTR**	=	________
CB Open Time Warning	0.25-63.75 cycles	**Topen**	=	________
BC Close Time Warning	0.25-63.75 cycles	**Tclose**	=	________
Volts Across Closed CB Warning	0.50-7.5 Volts	**Vwarn**	=	________
Port #1 Timeout	0-30 min.	**TIME1**	=	________
Port #2 Timeout	0-30 min.	**TIME2**	=	________
Autoport Selection	Port 1, 2, or 3 (both 1 and 2)	**AUTO**	=	________
# Rings after which modem answers	1-30	**RINGS**	=	________

[1] Amps, Volts, and Joules settings are in secondary quanitites.

INSTALLATION
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FIGURES

INSTALLATION

CONVENTIONAL TERMINAL BLOCK MODEL

Mounting

The relay mounts by its front vertical flanges in a 19" vertical relay rack. Use four #10 screws for mounting. This manual includes front and rear panel drawings.

Frame Ground Connection

Connect the terminal marked GND on the rear panel to frame ground for safety and performance. These terminals connect directly to the chassis ground of the instrument.

Power Connections

Connect terminals marked + (44) and - (45) on the rear panel to a source of control voltage. Control power passes through these terminals to a fuse and toggle switch if the unit has one. The power continues through a surge filter and connects to the switching power supply. Control power circuitry is isolated from the frame ground.

Secondary Circuits

The relay presents a very low burden to the secondary current and potential circuits. Each current and voltage circuit is independent of the other circuits; there is no interconnection of current or voltage circuits inside the instrument.

The relay requires difference-voltage potentials that must be obtained from voltage transformers on both sides of the circuit breaker if flashover and thermal protection functions are to be used.

Control Circuits

The control inputs are dry. To assert the 52A input, apply control voltage to the 52A input terminals. Each input is individually isolated, and a terminal pair is brought out for each input. There are no internal connections between control inputs. Each input draws about 4 mA when energized with nominal control voltage.

Control outputs are dry relay contacts rated for tripping duty. A metal-oxide varistor protects each contact. These devices have an energy rating of 80 joules, a maximum clamping voltage of 395 volts, and a minimum varistor voltage (for 1 mA dc current) of 212 volts.

Communications Circuits

Connections to the two EIA-232 serial communications ports are made via the two nine-pin connectors labeled PORT 1 and PORT 2R on the rear panel and PORT 2F on the front panel.

Communications circuits are protected by low-energy, low-voltage MOVs and passive RC filters. You can minimize communications circuit difficulties by keeping the length of the EIA-232 cables as short as possible. Lengths of twelve feet or less are recommended, and the cable length should never exceed 100 feet. Use shielded communications cable for lengths greater than ten feet. Modems are required for communications over long distances.

Route the communications cables well away from the secondary and control circuits. Do not bundle the communications wiring with secondary or control circuit wiring. If these wires are bundled, switching spikes and surges can cause noise in communications wiring. This noise can exceed communications logic thresholds and introduce errors. Route the IRIG-B clock cable away from the control wiring and secondary circuits as well.

Jumper Selection

Communication control jumpers are on the front edge of the main board. They are easily accessed by removing the top cover or front panel.

EIA-232 Jumpers

Jumper Block J6 provides EIA-232 baud rate selection. Available baud rates are 300, 1200, 2400, 4800, and 9600. To select a baud rate for a particular port, place the jumper so it connects a pin labeled with the desired port to a pin labeled with the desired rate.

Caution: Do not select two baud rates for the same port. This can damage the baud rate generator.

Password Protection Jumper

Put JMP103 in place to disable password protection. This feature is useful if passwords are not required or when passwords are forgotten.

Remote Control Enable Jumper

When JMP104 is in place, you can control relay output contacts remotely with the OUT command. With JMP104 removed, OUT command execution results in an "Aborted" message.

A5 Output Contact Jumper

With jumper JMP3 in the A4 position, the A5 output contact operates per mask MA5. With jumper JMP3 in the ALARM position, the A5 output contact operates with the ALARM output contact.

Output Contact Soldered Wire Jumpers

Output contacts can be configured as "a" or "b" contacts with soldered wire jumpers (each jumper has positions A and B). The output contact/soldered wire jumper correspondence is as follows:

Output Contact	Jumper SEL-2BFR
TRIP	JMP11
TRIP	JMP10
A1	JMP9
A2	JMP8
A3	JMP7
A4	JMP6
A5	JMP5
ALARM	JMP4

Communication Port External Power Jumpers

DC power is available from Port 1 and Port 2R to power external devices. Jumpers must be selected to route dc power to the rear panel connectors. The internal jumpers are near Port 1 and are labeled as follows: JMP12 = +5 V; JMP13 = +12 V; JMP14 = -12 V. Use caution to ensure the dc current requirement of the external equipment does not exceed the relay power supply specifications. Only route dc power to the rear ports if required for your application.

IRIG-B Installation

To synchronize the internal time clock to a source of demodulated IRIG-B time code (e.g., from a satellite time clock), connect the time source to the Auxiliary Input connector (J 201) on the rear panel. Pin definitions appear in Table 6.1.

Table 6.1: AUX INPUT Pin Definitions

Pin	Name	Description
1	+5	*
2	IRIGIN HI	Positive IRIG-B input.
3	IRIGIN LOW	Negative IRIG-B input.
4	+12	*
6	-12	*
5, 9	GND	Ground for ground wires and shields.

* Consult the factory before using these power supply outputs

The actual IRIG-B input circuit is a 56 ohm resistor in series with an opto-coupler input diode. The input diode has a forward drop of about 1.5 volts. Driver circuits should put approximately 10 mA through the diode when "on."

The IRIG-B serial data format consists of a one second frame containing 100 pulses and divided into fields. The relay decodes the second, minute, hour, and day fields and sets the internal relay clock accordingly.

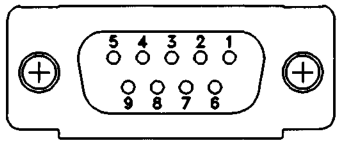
When IRIG-B data acquisition is activated either manually (with the IRIG command) or automatically, two consecutive frames are taken. The older frame is updated by one second and the two frames are compared. If they do not agree, the relay considers the data erroneous and discards it.

The relay reads the time code automatically about once every five minutes. The relay stops IRIG-B data acquisition ten minutes before midnight on New Year's Eve so the relay clock may implement the year change without interference from the IRIG-B clock. Ten minutes after midnight, the relay restarts IRIG-B data acquisition.

EIA-232 Installation

The following information provides details regarding communications port pinouts.

A pin definition of the nine-pin port connectors and cabling information for the EIA-232 ports appears in Figure 6.1. The following cable listings show several types of EIA-232 cables. These and other cables are available from SEL. Cable configuration sheets are also available at no charge for a large number of devices. Contact the factory for more information.



(female chassis connector, as viewed from outside panel)

Figure 6.1: Nine-Pin Connector Pin Number Convention

EIA-232 Cables

```
SEL-2BFR                        9-Pin *DTE DEVICE

GND  5 ------------------------- 5   GND
TXD  3 ------------------------- 2   RXD
RXD  2 ------------------------- 3   TXD          (SEL CABLE 234A)
                              +- 7   RTS
CTS  8 -----------------------+- 8   CTS

                           +- 1   DCD
                   Jumper  +- 4   DTR
                           +- 6   DSR
```

```
SEL-2BFR                        **DCE DEVICE

GND   5 ------------------------ 7   GND
TXD   3 ------------------------ 2   RXD
RTS   7 ------------------------ 20  DTR          (SEL CABLE 222)
RXD   2 ------------------------ 3   TXD
CTS   8 ------------------------ 8   CD
GND   9 ------------------------ 1   GND
```

```
SEL-PRTU                        SEL-2BFR

GND   1 ------------------------ 5   GND
TXD   2 ------------------------ 2   RXD
RXD   4 ------------------------ 3   TXD          (SEL CABLE 231)
CTS   5 ------------------------ 7   RTS
+12   7 ------------------------ 8   CTS
GND   9 ------------------------ 9   GND
```

* DTE = Data Terminal Equipment (Computer, Terminal, Printer, etc.)
** DCE = Data Communication Equipment (Modem, etc.)

```
        Data and IRIG-B

SEL-2020                    SEL-2BFR

RXD   2 ----------------- 3  TXD  ---+
TXD   3 ----------------- 2  RXD     |   (SEL CABLE 239)
GND   5 ----------------- 5  GND     |
RTS   7 ----------------- 8  CTS     |    Port 2R/J203
CTS   8 ----------------- 7  RTS  ---+
+IRIG 4 ----------------- 2  +IRIG --+
-IRIG 6 ----------------- 3  -IRIG --+   AUX Input/J201
```

```
          Data Only

SEL-2020                    SEL-2BFR

RXD   2 ----------------- 3  TXD
TXD   3 ----------------- 2  RXD
GND   5 ----------------- 5  GND          (SEL CABLE 272A)
RTS   7 ---+        +---- 8  CTS
CTS   8 ---+        +---- 7  RTS
```

Installation Checkout

You may follow the suggestions below or combine them with your standard procedures. Never implement recommendations prohibited by the rules of your normal practice.

The following equipment is required for initial checkout:

- Portable terminal or computer
- Control power to the relay power connections
- Source of three-phase voltages and at least two current sources
- Ohmmeter or contact opening/closing sensing device

1. Apply control power and make sure the terminal displays the startup message. Check the settings with the ACCESS and SHOWSET commands. Use the TIME command to set the clock.

2. Apply three-phase voltages. Execute the METER command and make sure the readings are accurate. If they are not, be sure the correct PT ratio was entered. Remember that displayed values are in primary line-to-neutral and line-to-line kV.

3. Use the TRIGGER command to generate an event record. Type **EVENT 1 <ENTER>** and examine the event record. Refer to the top row of data as the "Y" components and the next row as the "X" components. Plot the three voltage phasors to ensure that they are 120° apart, of reasonable magnitudes, and rotating in the positive-sequence direction. The zero-sequence voltage Y and X components (times a factor of three) are the totals of

the three Y components and the three X components. These sums should be near zero if balanced three-phase potentials are present. Remove three-phase voltages.

4. Apply three-phase currents and repeat steps 2 and 3 to ensure that the inputs are correct.

5. Use the TARGET command to check the state of all contact inputs and outputs.

6. Proceed to Access Level 2 with the 2ACCESS command and second password. Be sure the ALARM relay contacts close and open when the relay executes 2ACCESS. The ALARM pulse will not be detectable if the ALARM contacts are closed due to an alarm condition.

7. Test the tripping function. Be sure the 86BF TRIP output asserts when you execute the OUT T command. Also, the circuit breaker may be tripped by applying voltages, currents, and input assertions representing a fault condition for which the relay should respond.

8. Use the STATUS command to inspect the self-test status. You may wish to save the reading as part of an "as-left" record.

When local checkout is complete, check communications with the instrument via a remote interface (if used). Make sure the automatic port is properly assigned and that desired timeout intervals are selected for each port. Also, be sure to record password settings.

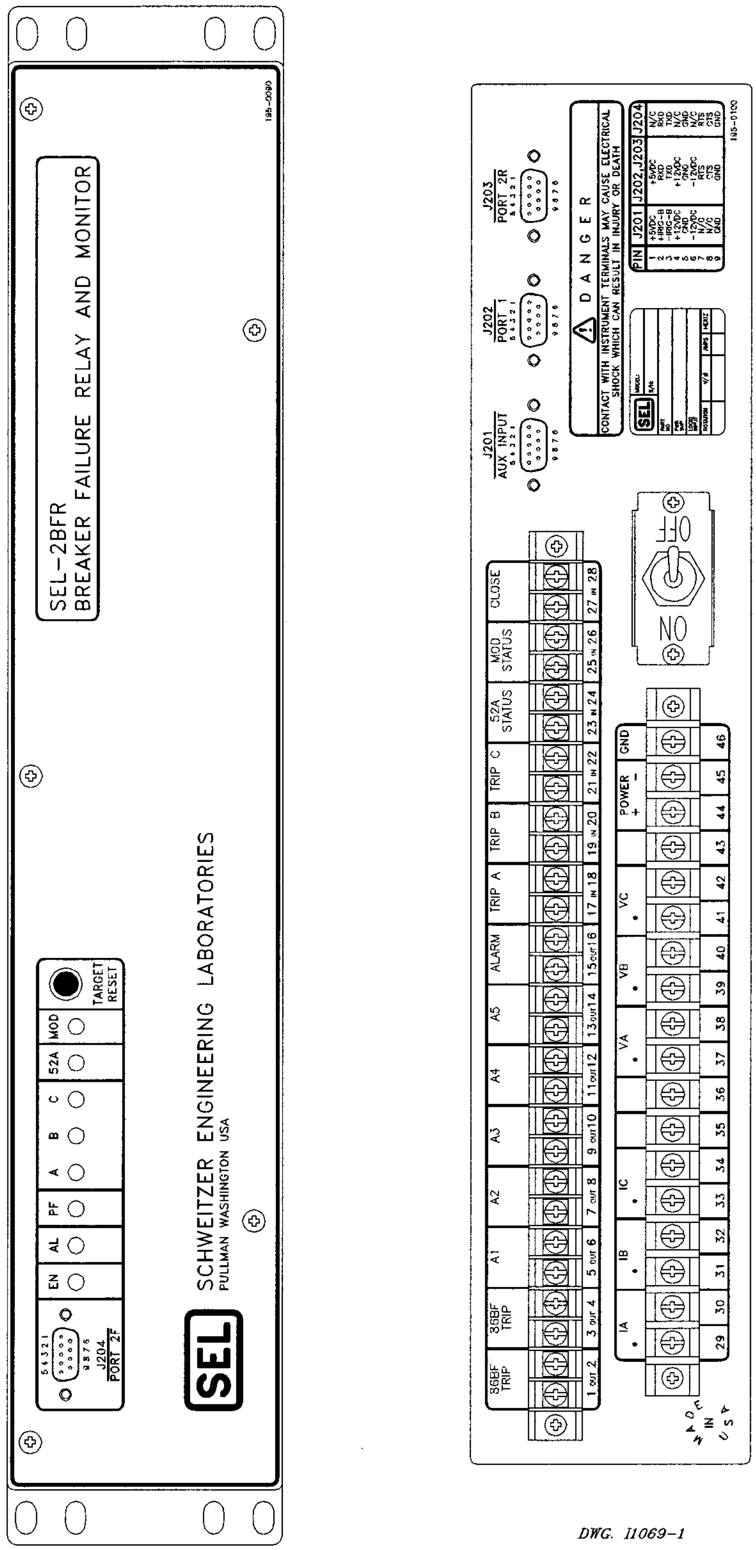
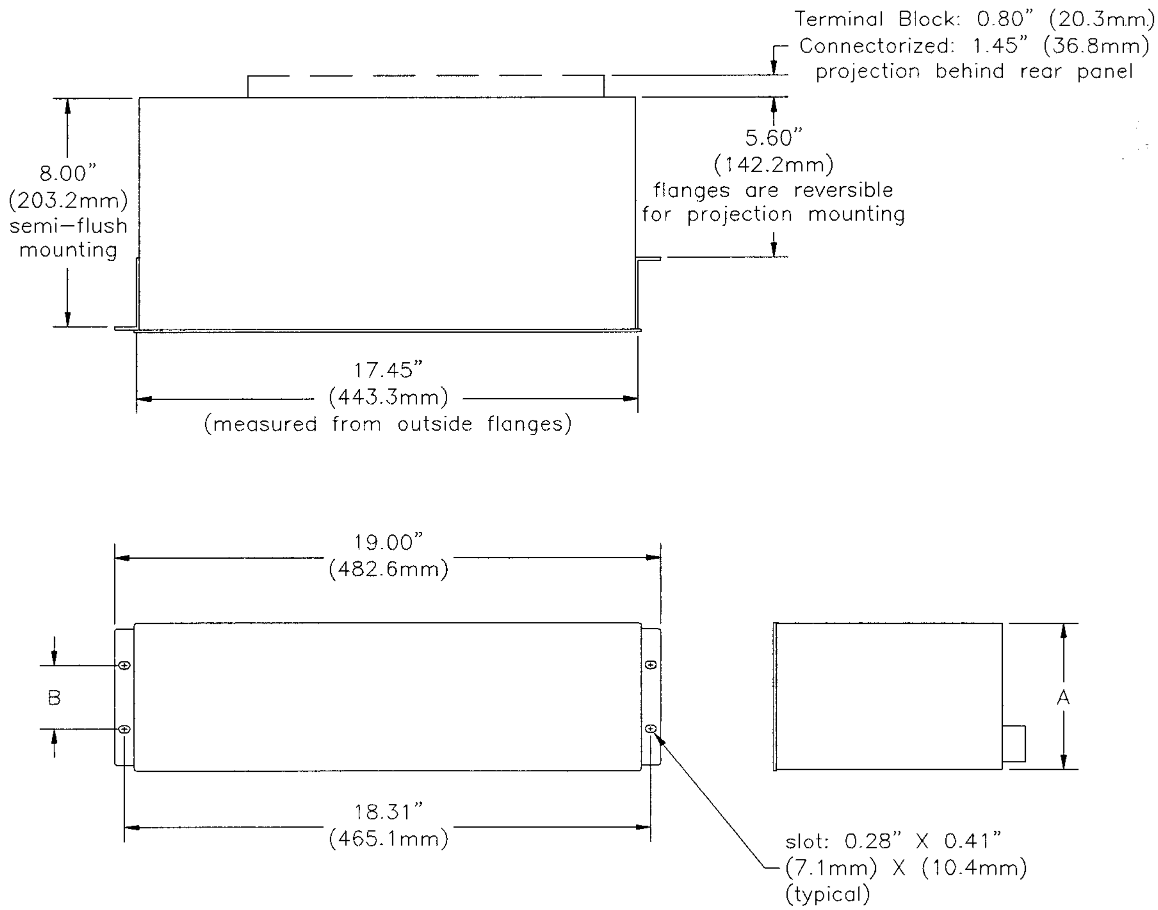


Figure 6.2: SEL-2BFR Conventional Terminal Block Model Horizontal Front and Rear Panel Drawings



DIMENSION	MAIN BOARD ONLY (2U)	ONE I/O BOARD (3U)	TWO I/O BOARDS (4U)
A	3.47" (88.1mm)	5.22" (132.6mm)	6.97" (177.0mm)
B	3.00" (76.2mm) 1.75" (44.5mm) optional	2.25" (57.2mm)	4.00" (101.6mm)

NOTE:

1. ALL TOLERANCES ARE ± 0.020" (0.51mm)
2. TO DETERMINE THE CUTOUT DIMENSIONS CONSIDER BOTH SEL'S SPECIFIED TOLERANCE AND THE CUSTOMER'S ALLOWED TOLERANCE.
3. DRAWING NOT TO SCALE
4. SLP DIMENSIONS APPLY TO THE FOLLOWING SEL DEVICES:
   a) ALL SEL-200 SERIES RELAYS EXCEPT FOR LP RELAYS WHICH INCLUDE: 279, 279H (1 Amp or 5 Amp), 251, 251C and 267-4 (1 Amp only)
   b) ALL SEL-300 SERIES RELAYS EXCEPT 321 RELAYS
   c) SEL-2020 and 2030

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Figure 6.3: SEL-2BFR Conventional Terminal Block Relay Dimensions and Drill Plan

PLUG-IN CONNECTOR MODEL

Mounting

The relay mounts by its front vertical flanges in a 19" vertical relay rack. Use four #10 screws for mounting. This manual includes front and rear panel drawings.

Frame Ground Connection

Connect the terminal marked GND (46) on the rear panel to frame ground for safety and performance. These terminals connect directly to the chassis ground of the instrument.

Power Connections

Connect terminals marked + (44) and - (45) on the rear panel to a source of control voltage. Control power passes through these terminals to a fuse. The power continues through a surge filter and connects to the switching power supply. Control power circuitry is isolated from the frame ground. A power connector is supplied with the wiring harness which connects to terminals 44 and 45. The connector can be ordered with #18-#14 AWG conductor.

Secondary Circuits

The relay presents a very low burden to the secondary current and potential circuits. Each current and voltage circuit is independent of the other circuits; there is no interconnection of current or voltage circuits inside the instrument.

The current connector supplied with the wiring harness is a shorting-type connector. When removed from the relay, the connector automatically shorts ct secondaries. The connector can be ordered with #16-#10 AWG conductors.

The relay requires difference-voltage potentials that must be obtained from voltage transformers on both sides of the circuit breaker if flashover and thermal protection functions are to be used.

A pt connector is supplied with the wiring harness. The connector can be ordered with #18-#14 AWG conductors.

Control Circuits

The control inputs are dry. To assert the 52A input, apply control voltage to the 52A input terminals. Each input is individually isolated, and a terminal pair is brought out for each input. There are no internal connections between control inputs. Each input draws 5-6 mA when energized with nominal control voltage.

Control outputs are dry relay contacts rated for 30 A make, 6 A carry, and 10 A interrupt with an L/R = 40 ms at 125 Vdc. The contacts can interrupt 10 A, L/R = 40, 125 Vdc four times in one second. Each contact is protected by a metal oxide varistor. Note, the contacts are polarity sensitive.

Communications Circuits

Connections to the two EIA-232 serial communications ports are made via the two nine-pin connectors labeled PORT 1 and PORT 2R on the rear panel and PORT 2F on the front panel.

Communications circuits are protected by low-energy, low-voltage MOVs and passive RC filters. You can minimize communications circuit difficulties by keeping the length of the EIA-232 cables as short as possible. Lengths of twelve feet or less are recommended, and the cable length should never exceed 100 feet. Use shielded communications cable for lengths greater than ten feet. Modems are required for communications over long distances.

Route the communications cables well away from the secondary and control circuits. Do not bundle the communications wiring with secondary or control circuit wiring. If these wires are bundled, switching spikes and surges can cause noise in communications wiring. This noise can exceed communications logic thresholds and introduce errors. Route the IRIG-B clock cable away from the control wiring and secondary circuits as well.

Jumper Selection

Communications port control jumpers are on the front edge of the main board. They are easily accessed by removing the top cover or front panel.

EIA-232 Jumpers

Jumper Block J6 provides EIA-232 baud rate selection. Available baud rates are 300, 1200, 2400, 4800, and 9600. To select a baud rate for a particular port, place the jumper so it connects a pin labeled with the desired port to a pin labeled with the desired rate.

Caution: Do not select two baud rates for the same port. This can damage the baud rate generator.

Password Protection Jumper

Put JMP103 in place to disable password protection. This feature is useful if passwords are not required or when passwords are forgotten.

Remote Control Enable Jumper

When JMP104 is in place, you can control relay output contacts remotely with the OUT command. With JMP104 removed, OUT command execution results in an "Aborted" message.

A5 Output Contact Jumper

With jumper JMP3 in the A4 position, the A5 output contact operates per mask MA5. With jumper JMP3 in the ALARM position, the A5 output contact operates with the ALARM output contact.

Communication Port External Power Jumpers

+5 Vdc power is available from Port 1 and Port 2R to energize external devices. JMP12 must be bridged in order to route power to the rear ports. Use caution to ensure the dc current requirement of the external equipment does not exceed the relay power supply specifications. Route dc power to the rear ports only when required by your application.

Jumper Installation Instructions

The power available from these ports is limited and should be used only for SEL-RDs, SEL-DTAs, dc-powered modems, or other low-wattage devices approved by SEL.

The power is available on either Port 1 or Port 2R. Port 2F, located on the front of the relay, does NOT have power available.

To install jumpers for supplying power through the rear EIA-232-C ports on all SEL-200 series relays (except SEL-279 and SEL-279H Relays), perform the following steps:

1. Remove the relay top cover or withdraw the main circuit board.
2. Locate jumpers JMP12 (+5 Vdc), JMP13 (+12 Vdc) and JMP14 (-12 Vdc) near the AUX INPUT connector.
3. Remove and install the needed jumpers in the "on" position.
4. Replace the top cover or reinsert the main circuit board. (Ensure that the board is correctly seated and the cables to the power supply and inputer transformers are reconnected.)

IRIG-B Installation

To synchronize the internal time clock to a source of demodulated IRIG-B time code (e.g., from a satellite time clock), connect the time source to the Auxiliary Input connector (J201) on the rear panel. Pin definitions appear in Table 6.1.

On the Plug-in Connector model, Ports 1 and 2R may be configured to accept demodulated IRIG-B input. When JMP13 and JMP14 are bridged, pins 6 and 4 will accept -IRIG-B and +IRIG-B, respectively. See Table 3.2 for port pinouts.

The actual IRIG-B input circuit is a 56 ohm resistor in series with an opto-coupler input diode. The input diode has a forward drop of about 1.5 volts. Driver circuits should put approximately 10 mA through the diode when "on."

The IRIG-B serial data format consists of a one second frame containing 100 pulses and divided into fields. The relay decodes the second, minute, hour, and day fields and sets the internal relay clock accordingly.

When IRIG-B data acquisition is activated either manually (with the IRIG command) or automatically, two consecutive frames are taken. The older frame is updated by one second and the two frames are compared. If they do not agree, the relay considers the data erroneous and discards it.

The relay reads the time code automatically about once every five minutes. The relay stops IRIG-B data acquisition ten minutes before midnight on New Year's Eve so the relay clock may implement the year change without interference from the IRIG-B clock. Ten minutes after midnight, the relay restarts IRIG-B data acquisition.

EIA-232 Installation

The following information provides details regarding communications port pinouts.

A pin definition of the nine-pin port connectors and cabling information for the EIA-232 ports appears in Figure 6.2. The following cable listings show several types of EIA-232 cables. These and other cables are available from SEL. Cable configuration sheets are also available at no charge for a large number of devices. Contact the factory for more information.

EIA-232 Cables

```
SEL-2BFR                          9-Pin *DTE DEVICE

GND  5 ------------------------- 5   GND
TXD  3 ------------------------- 2   RXD
RXD  2 ------------------------- 3   TXD          (SEL CABLE 234A)
                             ┌-- 7   RTS
CTS  8 ----------------------┴-- 8   CTS

                           ┌-- 1   DCD
                   Jumper  ├-- 4   DTR
                           └-- 6   DSR
```

```
SEL-2BFR                          **DCE DEVICE

GND   5 ------------------------ 7   GND
TXD   3 ------------------------ 2   RXD
RTS   7 ------------------------ 20  DTR          (SEL CABLE 222)
RXD   2 ------------------------ 3   TXD
CTS   8 ------------------------ 8   CD
GND   9 ------------------------ 1   GND
```

```
SEL-PRTU                        SEL-2BFR

GND   1 ------------------------ 5   GND
TXD   2 ------------------------ 2   RXD
RXD   4 ------------------------ 3   TXD        (SEL CABLE 231)
CTS   5 ------------------------ 7   RTS
+12   7 ------------------------ 8   CTS
GND   9 ------------------------ 9   GND
```

* DTE = Data Terminal Equipment (Computer, Terminal, Printer, etc.)
** DCE = Data Communication Equipment (Modem, etc.)

```
          Data and IRIG-B

SEL-2020                  SEL-2BFR

RXD   2 ---------------- 3   TXD  --+
TXD   3 ---------------- 2   RXD    |   (SEL CABLE 239)
GND   5 ---------------- 5   GND    |
RTS   7 ---------------- 8   CTS    |    Port 2R/J203
CTS   8 ---------------- 7   RTS  --+
+IRIG 4 ---------------- 2   +IRIG -+
-IRIG 6 ---------------- 3   -IRIG -+   AUX Input/J201
```

```
             Data Only

SEL-2020                  SEL-2BFR

RXD   2 ---------------- 3   TXD
TXD   3 ---------------- 2   RXD
GND   5 ---------------- 5   GND        (SEL CABLE 272A)
RTS   7 --+          +-- 8   CTS
CTS   8 --+          +-- 7   RTS
```

```
      Enhanced Data and IRIG-B

SEL-2020                  SEL-2BFR

RXD   2 ---------------- 3   TXD
TXD   3 ---------------- 2   RXD
GND   5 ---------------- 5   GND        (SEL CABLE 273A)
RTS   7 ---------------- 8   CTS
CTS   8 ---------------- 7   RTS
+IRIG 4 ---------------- 4   +IRIG*
-IRIG 6 ---------------- 6   -IRIG*
```

* When JMP13 and JMP14 are bridged.

Installation Checkout

You may follow the suggestions below or combine them with your standard procedures. Never implement recommendations prohibited by the rules of your normal practice.

The following equipment is required for initial checkout:

- Portable terminal or computer
- Control power to the relay power connections
- Source of three-phase voltages and at least two current sources
- Ohmmeter or contact opening/closing sensing device

1. Apply control power and make sure the terminal displays the startup message. Check the settings with the ACCESS and SHOWSET commands. Use the TIME command to set the clock.

2. Apply three-phase voltages. Execute the METER command and make sure the readings are accurate. If they are not, be sure the correct PT ratio was entered. Remember that displayed values are in primary line-to-neutral and line-to-line kV.

3. Use the TRIGGER command to generate an event record. Type **EVENT 1 <ENTER>** and examine the event record. Refer to the top row of data as the "Y" components and the next row as the "X" components. Plot the three voltage phasors to ensure that they are 120° apart, of reasonable magnitudes, and rotating in the positive-sequence direction. The zero-sequence voltage Y and X components (times a factor of three) are the totals of the three Y components and the three X components. These sums should be near zero if balanced three-phase potentials are present. Remove three-phase voltages.

4. Apply three-phase currents and repeat steps 2 and 3 to ensure that the inputs are correct.

5. Use the TARGET command to check the state of all contact inputs and outputs.

6. Proceed to Access Level 2 with the 2ACCESS command and second password. Be sure the ALARM relay contacts close and open when the relay executes 2ACCESS. The ALARM pulse will not be detectable if the ALARM contacts are closed due to an alarm condition.

7. Test the tripping function. Be sure the 86BF TRIP output asserts when you execute the OUT T command. Also, the circuit breaker may be tripped by applying voltages, currents, and input assertions representing a fault condition for which the relay should respond.

8. Use the STATUS command to inspect the self-test status. You may wish to save the reading as part of an "as-left" record.

When local checkout is complete, check communications with the instrument via a remote interface (if used). Make sure the automatic port is properly assigned and that desired timeout intervals are selected for each port. Also, be sure to record password settings.

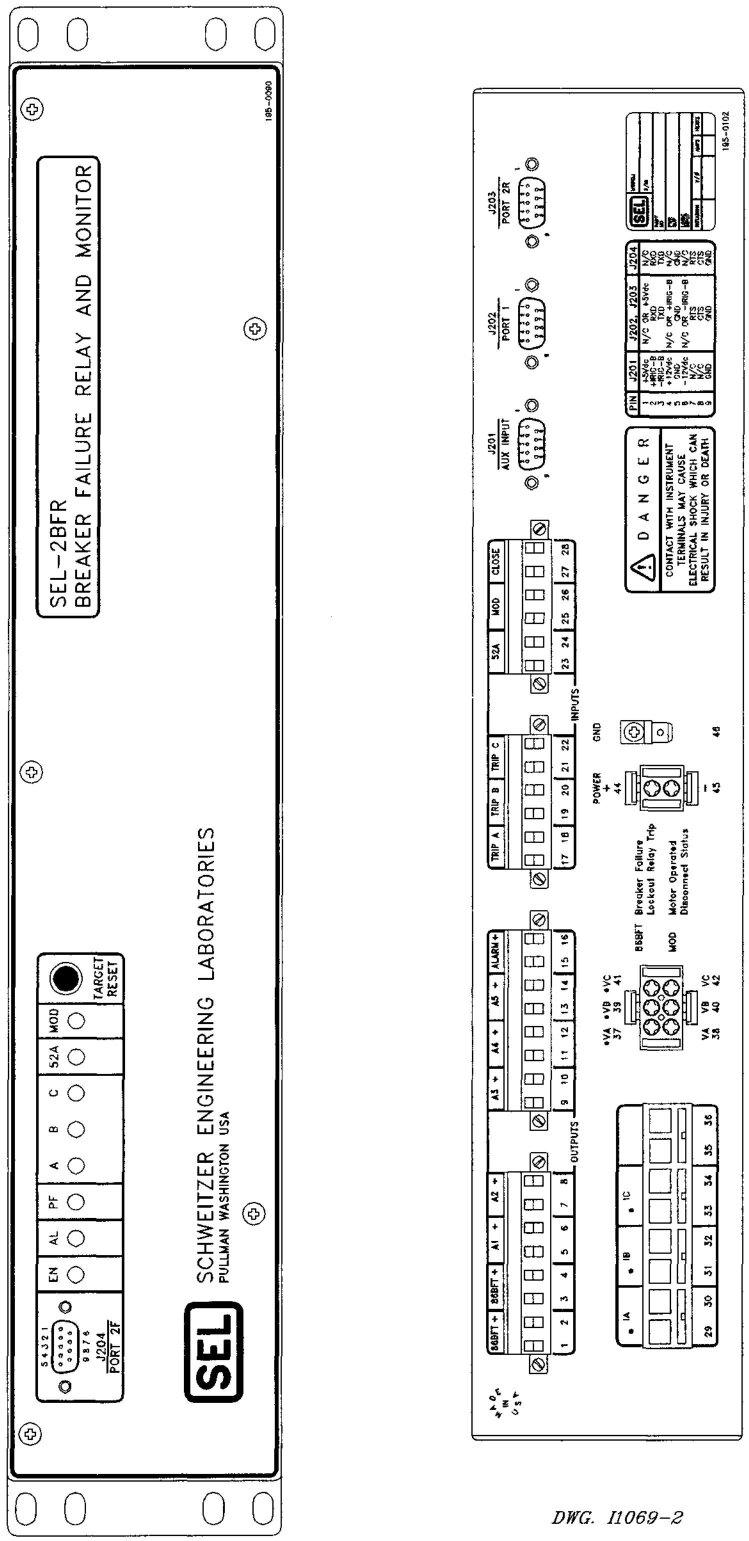

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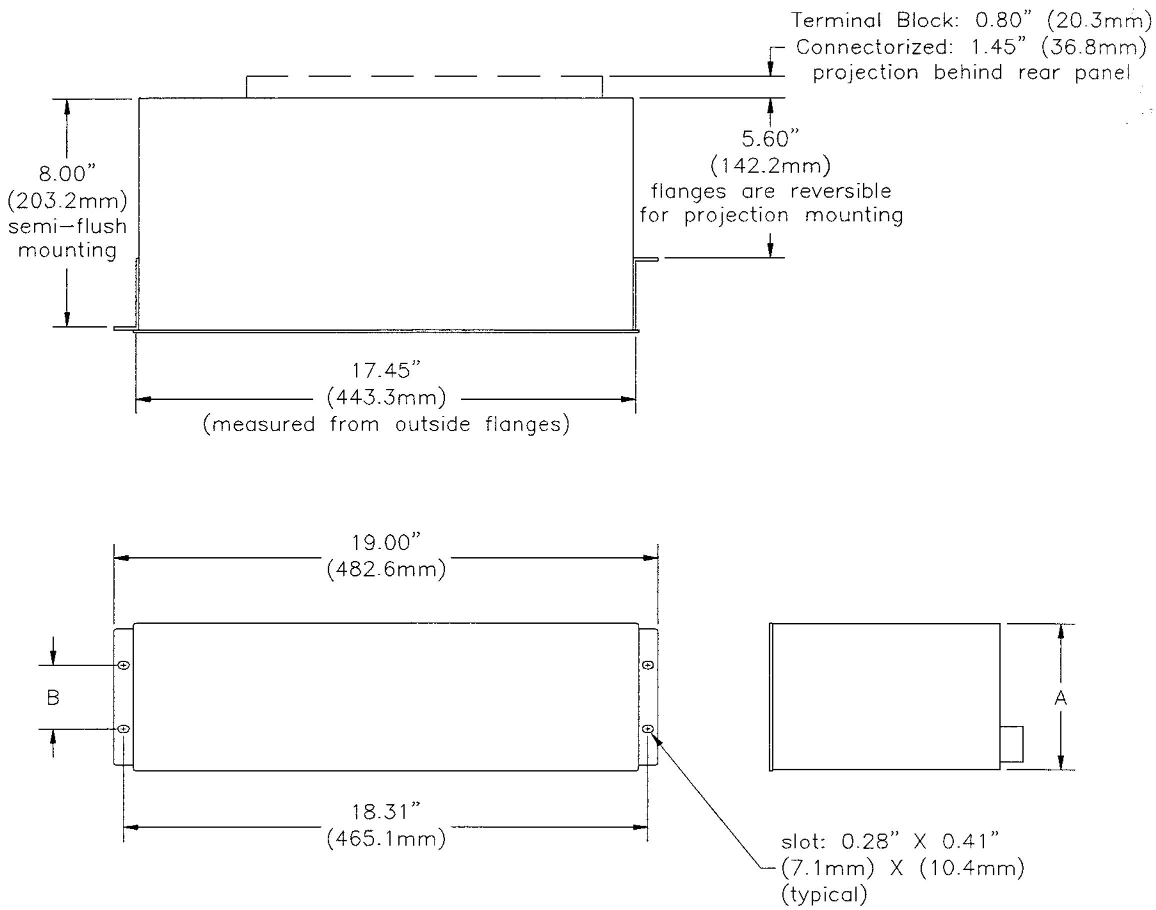
Figure 6.4: SEL-2BFR Plug-In Connector Model Horizontal Front and Rear Panel Drawings



DIMENSION	MAIN BOARD ONLY (2U)	ONE I/O BOARD (3U)	TWO I/O BOARDS (4U)
A	3.47" (88.1mm)	5.22" (132.6mm)	6.97" (177.0mm)
B	3.00" (76.2mm) 1.75" (44.5mm) optional	2.25" (57.2mm)	4.00" (101.6mm)

NOTE:

1. ALL TOLERANCES ARE ± 0.020" (0.51mm)
2. TO DETERMINE THE CUTOUT DIMENSIONS CONSIDER BOTH SEL'S SPECIFIED TOLERANCE AND THE CUSTOMER'S ALLOWED TOLERANCE.
3. DRAWING NOT TO SCALE
4. SLP DIMENSIONS APPLY TO THE FOLLOWING SEL DEVICES:
   a) ALL SEL-200 SERIES RELAYS EXCEPT FOR LP RELAYS WHICH INCLUDE: 279, 279H (1 Amp or 5 Amp), 251, 251C and 267-4 (1 Amp only)
   b) ALL SEL-300 SERIES RELAYS EXCEPT 321 RELAYS
   c) SEL-2020 and 2030

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Figure 6.5: SEL-2BFR Plug-In Connector Relay Dimensions and Drill Plan

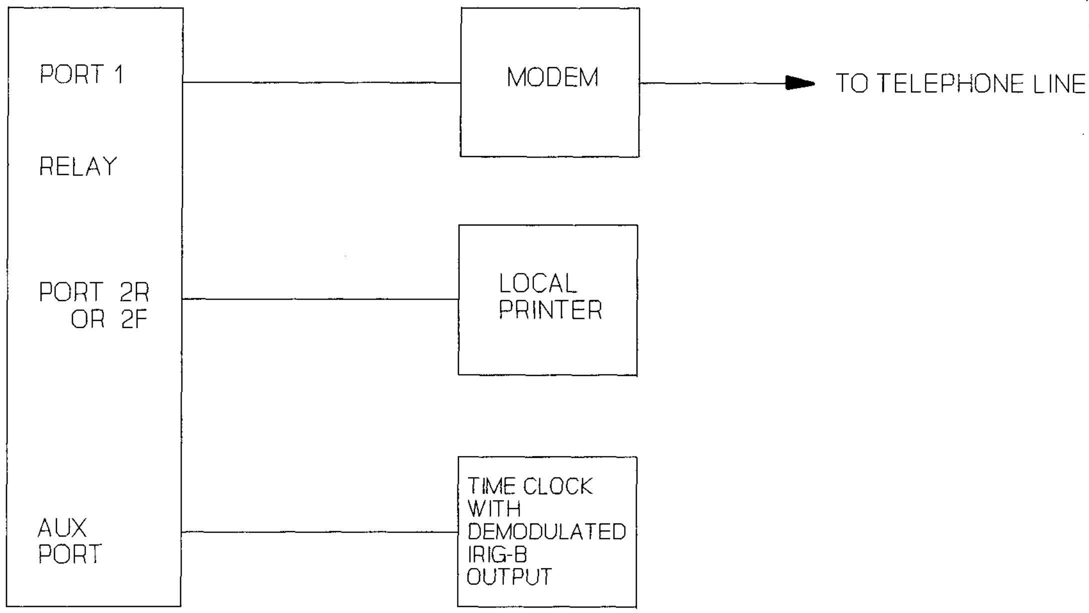


Figure 6.6: Communications and Clock Connections - One Unit at One Location

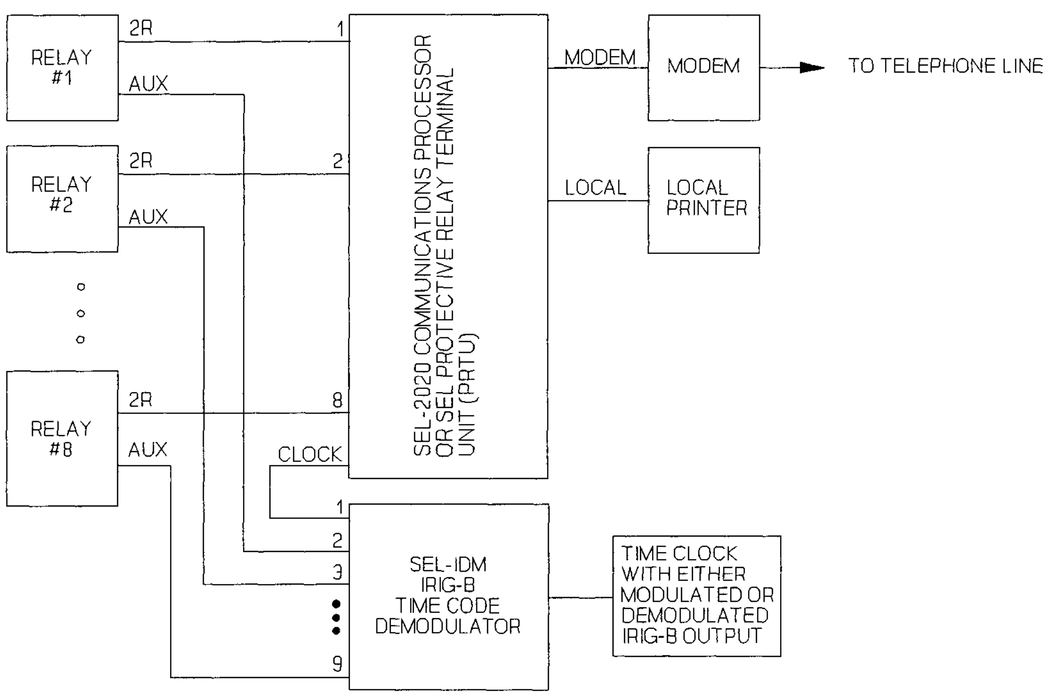


Figure 6.7: Communications and Clock Connections - Multiple Units at One Location

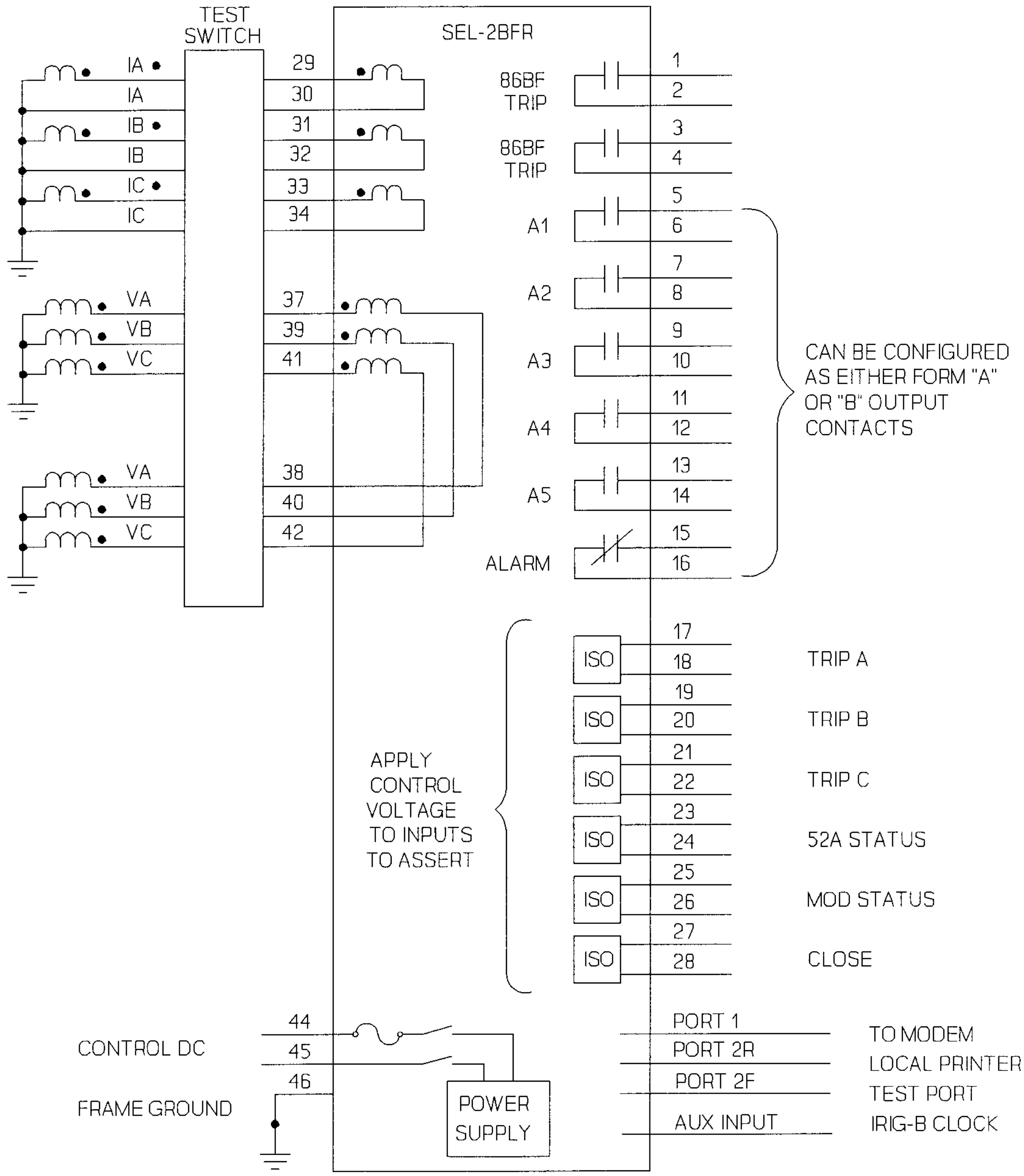


Figure 6.8: External Current and Voltage Connections

SEL DIRECTION AND POLARITY CHECK FORM

STATION ________________ DATE: __/__/__ TESTED BY ________________

SWITCH NO. ________________ EQUIPMENT ________________

INSTALLATION ________ ROUTINE ________ OTHER ________________

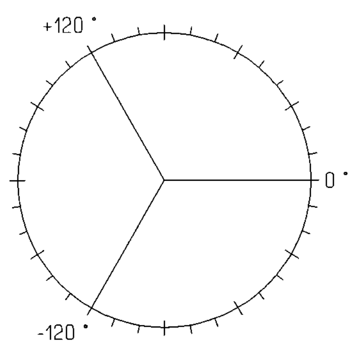
LOAD CONDITIONS:

STATION READINGS: ________ MW (OUT)(IN) ________ MVAR (OUT)(IN) ________ VOLTS ________ AMPS

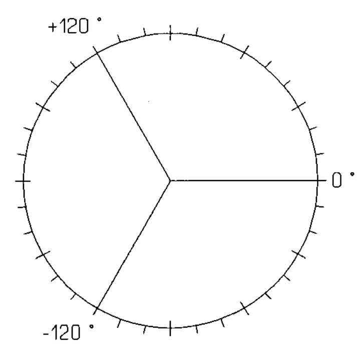
SEL READINGS: ________ MW (+)(-) ________ MVAR (+)(-)

AS SEEN ON SCREEN	Ia	Ib	Ic	Va	Vb	Vc	
COMPANY NOTATION	I( )	I( )	I( )	V( )	V( )	V( )	
1st LINE CHOSEN (Y COMPONENT)							
2nd LINE CHOSEN (X COMPONENT)							
CALCULATED MAGNITUDE $\sqrt{X^2 + Y^2}$							ROW 1
ANGLE IN DEGREES ARCTAN Y/X							
VALUE OF Va DEGREES TO SUBTRACT TO OBTAIN Va DEGREES = 0							
@ Va DEGREES = 0, ANGLE USED TO DRAW PHASOR DIAGRAM							ROW 2

USE THE VALUES IN ROWS 1 AND 2 ABOVE TO DRAW PHASOR DIAGRAMS BELOW



CURRENTS



VOLTAGES

SEL DIRECTION AND POLARITY CHECK FORM

STATION ______________________________ DATE: ___/___/___ TESTED BY ____________________

SWITCH NO. ____________________ EQUIPMENT ______________________________________

INSTALLATION ________ROUTINE ________OTHER ______________________________________

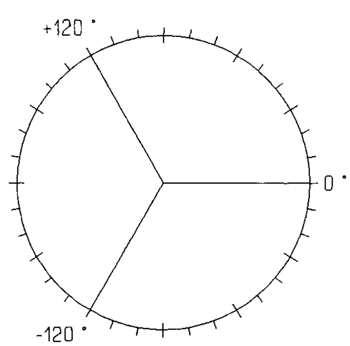
LOAD CONDITIONS:

STATION READINGS: ________MW (OUT)(IN) ________MVAR (OUT)(IN) ________ VOLTS ________ AMPS

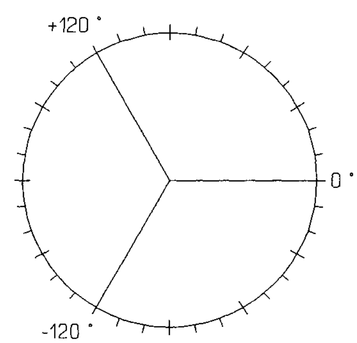
SEL READINGS: ________MW (+)(-) ________MVAR (+)(-)

AS SEEN ON SCREEN	Ia	Ib	Ic	Va	Vb	Vc	
COMPANY NOTATION	I( )	I( )	I( )	V( )	V( )	V( )	
1st LINE CHOSEN (Y COMPONENT)							
2nd LINE CHOSEN (X COMPONENT)							
CALCULATED MAGNITUDE $\sqrt{X^2 + Y^2}$							ROW 1
ANGLE IN DEGREES ARCTAN Y/X							
VALUE OF Va DEGREES TO SUBTRACT TO OBTAIN Va DEGREES = 0							
@ Va DEGREES = 0, ANGLE USED TO DRAW PHASOR DIAGRAM							ROW 2

USE THE VALUES IN ROWS 1 AND 2 ABOVE TO DRAW PHASOR DIAGRAMS BELOW



CURRENTS



VOLTAGES

MAINTENANCE & TESTING
TABLE OF CONTENTS

TABLES

FIGURES

MAINTENANCE AND TESTING

TEST PROCEDURES

Test Aids Provided by the Relay

The following features assist you during relay testing and calibration.

METER Command	The METER command shows the voltages and currents presented to the relay in primary values. The relay calculates megawatts (MW) and megavars (MVAR) from these voltages and currents. These quantities are useful for comparing relay calibration against other meters of known accuracy. When testing the relay, first verify relay calibration. Consider all tests invalid if you determine that the relay is out of calibration. Each relay is calibrated at the factory prior to shipment and should not require further adjustment. If calibration is necessary, refer to the Calibration portion of this section.
TARGET Command	The relay allows you to reassign front panel targets to indicate elements and intermediate logic results in the Relay Word as well as input and output contact status. Use the TARGET command to reassign the front panel LEDs. Once target LEDs are reassigned from the default targets, the front panel targets are no longer latching. This means the targets follow the pickup and dropout condition in much the same manner as an output contact. See ***Section 3: Communications*** for further information about the TARGET command. By employing the target LEDs for testing, you need not change the relay settings for testing purposes.
Event Reporting	The relay generates a fifteen-cycle event report in response to assertion of the 86BF TRIP output or selected triggering elements. Each event report contains voltage and current information, Relay Word bit states, and input/output contact information in quarter-cycle resolution. If you question the relay response or your test method, use the event report for assistance. Each event report is date and time tagged relative to the eighth quarter-cycle of the event report. Each report is triggered upon assertion of designated relay elements and/or contact inputs and outputs. If the timeout of a protective element results in 86BF TRIP output contact closure following the expiration of the first report, the relay generates a second event report. Thus, the relay can generate two event reports for a single fault: the first when the instantaneous element asserted, the second when the 86BF TRIP output contact closes.

Where time delayed pickup (TDPU) timers are concerned, the time tag in the event reports may be used to determine the validity of a TDPU timer setting. Simply subtract the latest event report time tag from the previous event report time tag. ***Section 2: Specifications*** has further details concerning event report generation.

Programmable Logic

Programmable logic allows you to isolate individual relay elements. See the LOGIC command description in ***Section 3: Communications*** for further details.

Low-Level Test Interface

The SEL-2BFR Relay has low-level test interface between the calibrated input module and the separately-calibrated processing module. You may test the relay in either of two ways: conventionally, by applying ac current signals to the relay inputs; or by applying low magnitude ac voltage signals to the low-level test interface. Access the test interface by removing the relay front panel.

Figure 7.1 shows the interface connections. This drawing also appears on the inside of the relay front panel. Remove the ribbon cable between the two modules to access the outputs of the input module and the inputs to the processing module (relay main board).

You can test the relay processing module using signals from the SEL-RTS Low-Level Relay Test System. Never apply voltage signals greater than 20 volts peak-peak to the low-level test interface. Figure 7.1 shows the signal scaling factors.

You can test the input module two different ways:

- Measure the outputs from the input module with an accurate voltmeter, and compare the readings to accurate instruments in the relay input circuits, or

- replace the ribbon cable, execute the METER command, and compare the relay readings to accurate instruments in the relay input circuits.

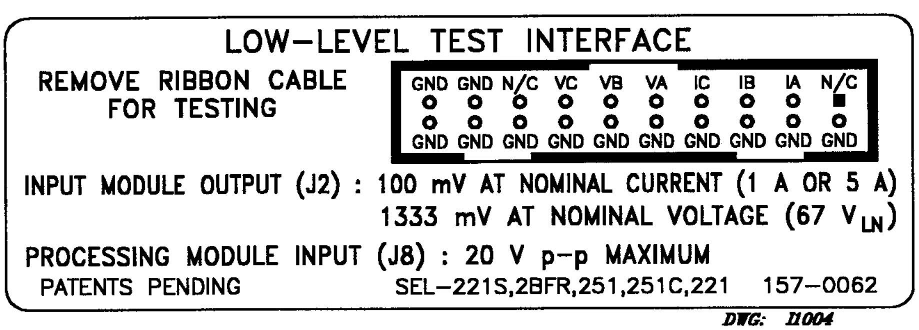


Figure 7.1: Low-Level Test Interface

On the Plug-in Connector model, the low-level test interface uses a 34-position connector rather than a 20-position connector. The input module output has been changed from J2 to J1. Pins 21-30 are no connects, pins 31 and 32 are +15 Vdc, and pins 33 and 34 are -15 Vdc.

Test Methods

There are two means of determining the pickup and dropout of relay elements: target LED illumination and output contact closure.

Testing Via Target LED Illumination

During testing you can use target LED illumination to determine relay element status. Using the TARGET command, set the front panel targets to display the element under test. Using LED illumination as an indicator, you can measure the element operating characteristics.

For example, the fault level overcurrent element 50FT appears in Relay Word row 1. When you type the command **TARGET 1 <ENTER>**, the LEDs display the status of the elements in Relay Word row 1. Thus, with Target 1 displayed, if the fault level overcurrent element (50FT) asserts, the fourth LED from the left illuminates.

When you use the TARGET command to set the target LED output to a level other than 0 (Relay Targets), the front panel target markings no longer correspond to illuminated LEDs. Also, the LEDs do not latch.

Be sure to reset front panel targets to Level 0 before returning the relay to service.

Testing Via Output Contact Assertion

To test using this method, set one programmable output contact to assert when the element under test picks up. With the LOGIC n command, set a 1 in the mask for the element under test. Set all other elements in that mask to 0.

For an "a" contact, when the condition asserts, the output contact closes. When the condition deasserts, the output contact opens.

For a "b" contact, when the condition asserts, the output contact opens. When the condition deasserts, the output contact closes.

On Conventional Terminal Block relays, programmable contacts can be specified at the factory as "a" or "b." Using contact operation as an indicator, you can measure element operating characteristics, stop timers, etc.

All contacts are "a", except for the ALARM which is "b", on the Plug-in Connector Model.

Tests in this chapter use the output contact method and assume an "a" output contact.

INITIAL CHECKOUT

The initial checkout procedure should familiarize you with the relay and ensure that all functions are operational. For a complete understanding of the relay capabilities, study Functional Specification and Description in ***Section 2: Specifications***, command descriptions in ***Section 3: Communications***, and ***Section 4: Event Reporting***.

Equipment Required

The following equipment is necessary for initial checkout.

1. Terminal with EIA-232 serial interface
2. Interconnecting cable between terminal and relay
3. Source of control power
4. Source of three-phase voltages and at least two currents
5. Ohmmeter or contact opening/closing sensing device

Checkout Procedure

In the procedure below, you will use several relay commands. ***Section 3: Communications*** provides a full explanation of all commands. However, the following information should allow you to complete the checkout without referring to the detailed descriptions.

Note: In this manual, commands to type appear in bold/uppercase: **OTTER**. Keys to press appear in bold/uppercase/brackets: **<ENTER>**.

Relay output appears in the following format:

```
Example 500 kV Line                Date: 6/1/92            Time: 01:01:01
```

■ **Step 1**

Purpose: Be sure you received the relay in satisfactory condition.

Method: Inspect the instrument for physical damage such as dents or rattles.

- **Step 2**

Purpose: Verify requirements for relay logic inputs, control power voltage level, and voltage and current inputs.

Method: Refer to the information sticker on the rear panel of the relay. Figure 7.2 provides an example. Check the information on this sticker before applying power to the relay or starting tests. Be sure your dc supply is correctly adjusted for the control and logic input requirements.

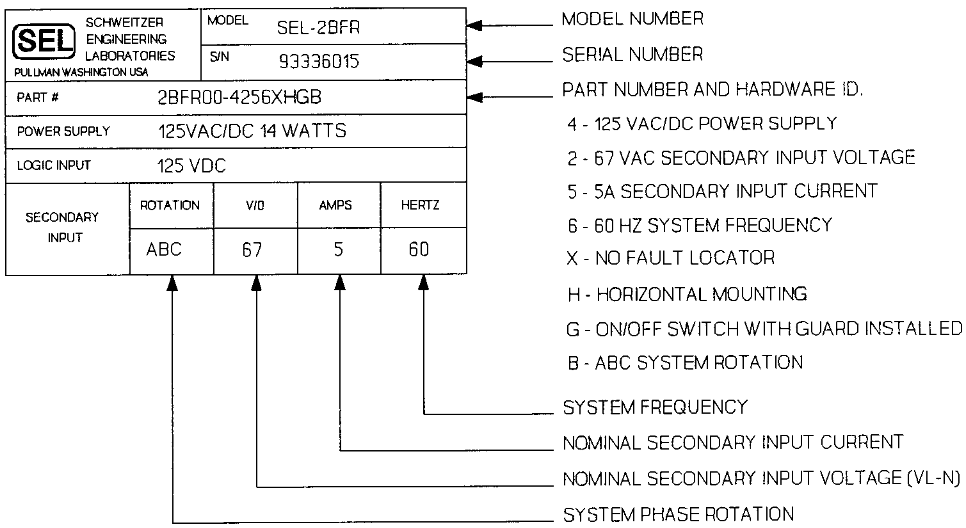


Figure 7.2: Relay Part Number and Hardware Identification Sticker

- **Step 3**

Purpose: Verify the communications interface setup.

Method: Connect a computer terminal to PORT 2 on the relay front or rear panel. The terminal should be configured to 2400 baud, eight data bits, two stop bits, and no parity. The relay is shipped from the factory with PORT 2 set to 2400 baud and PORT 1 set to 300 baud. ***Section 3: Communications*** provides additional information about port configuration. Baud rate selection is described under Jumper Selection in ***Section 6: Installation***. Figure 7.3 shows the typical communication interface setup for testing purposes.

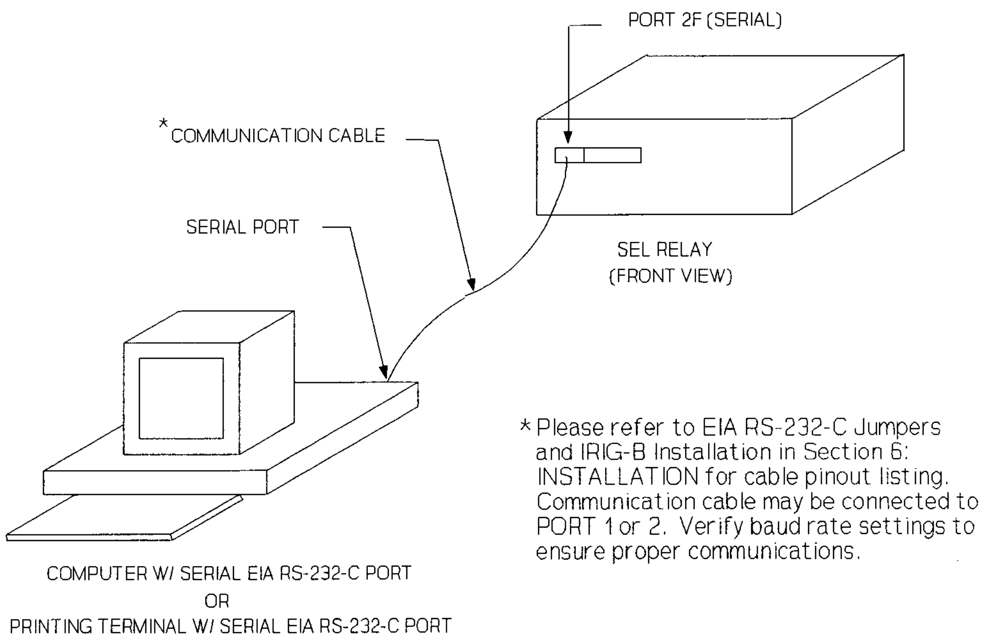


Figure 7.3: Communication Interface Setup

- **Step 4**

Purpose: Establish control power connections.

Method: Connect a frame ground to terminal marked GND on the rear panel and connect rated control power to terminals marked + and -. Polarity is unimportant. Relays supplied with 125 or 250 V power supplies may be powered from a 115 Vac wall receptacle for testing. In the final installation, we recommend that the relay receive control power from the station dc battery to avoid losing event reports stored in volatile memory if station service is lost.

- **Step 5**

Purpose: Apply control voltage to the relay and start Access Level 0 communications.

Method: Turn on the relay power. The enable target (EN) should illuminate. If not, be sure that power is present and check the fuse or fuses. The following message should appear on the terminal:

```
Example 500 kV Breaker                    Date: 6/1/92        Time: 05:18:48

SEL-BFR
=
```

The ALARM relay should pull in, holding its "b" contacts open. Since the 52BV bit is set in the MA2 logic mask, output relay A2 remains closed until you apply three-phase current above the 50LD setting and apply dc control voltage to the 52A input.

If the relays pull in, but your terminal does not display a message, check the terminal configuration. If neither occurs, turn off the power and refer to the Troubleshooting Guide later in this section.

The = prompt indicates that communications with the relay are at Access Level 0, the first of three levels. The only command accepted at this level is ACCESS, which opens communications on Access Level 1.

Note: If you are using a battery simulator, be sure the simulator voltage level is stabilized before turning the relay on.

- **Step 6**

Purpose: Establish Access Level 1 communications.

Method: Type **ACCESS** and press **<ENTER>**. At the prompt, enter the Access Level 1 password **OTTER** and press **<ENTER>**. The => prompt should appear, indicating that you have established communications at Access Level 1.

- **Step 7**

Purpose: Verify relay self-test status.

Method: Type **STATUS** and press **<ENTER>**. The following display should appear on the terminal:

```
Example 500 kV Breaker                    Date: 6/1/92          Time: 05:19:13

SELF-TEST STATUS

W=Warning F=Failure

      IA   IB   IC   VA   VB   VC
OS    -2   0    0    0    0    0
PS     5.03     15.07     -15.23
RAM   ROM   A/D   MOF   SET
OK    OK    OK    OK    OK

ALARM History:

=>
```

Step 8

Purpose: View demonstration settings entered before shipment.

Method: The relay is shipped with demonstration settings; type **SHOWSET <ENTER>** to view the settings. The terminal should display the following:

```
Settings for: Example 500 kV Breaker

Schm = 2       50FT  = 8.60     TTpu  = 6.00     TTdo   = 2.00    62FC = 4.00
50LD = 0.52    62LD  = 5.50     62LP  = 3.25
62AP = 5.25    62AF  = 7.50     E62A  = N         DRTE  = N       RTTD = 2.00
37OP = 2.25    26CF  = 1.45     26CP  = 1.09     26TF   = 4.56    26TP = 3.42
47Q  = 18.70   62OP  = 3.00     CRTC  = 80       TRTC   = 80
59FO = 4.01    62FF  = 30.00    62FP  = 25.00
87UB = 16      62UC  = 12.00    62UF  = 60.00    62UP   = 50.00
50MD = 0.10    62M1  = 600.00   62M2  = 600.00   ModTrip= Y
CTR  = 600     PTR   = 4300
Topen= 2.25    Tclose= 10.25    Vwarn = 0.47
TIME1= 5       TIME2 = 0        AUTO  = 2        RINGS  = 3

Logic settings:

M86T  MA1  MA2  MA3  MA4  MA5  MER
  C1   00   02   00   20   00   20
  80   08   00   00   40   00   48
  81   00   00   02   40   04   42
  00   00   00   00   55   00   55
  00   00   00   00   50   00   5F
  --   --   --   --   --   --   00
  --   --   --   --   --   --   07

=>
```

Note: The SEL-2BFR-2 Relay includes the RTSD setting (not shown).

The SET and LOGIC command descriptions in ***Section 3: Communications*** include a complete explanation of the settings.

Logic settings appear in hexadecimal format. A table and example of hexadecimal to binary conversion appears with the SHOWSET command description in ***Section 3: Communications***.

■ **Step 9**

Purpose: Connect voltage sources to the relay.

Method: Turn power off and connect a source of three-phase voltages to the relay at terminals marked VA•, VB•, and VC•. Connect the voltage neutral lead to terminals marked VA, VB, and VC. Apply 67 volts per phase (line-to-neutral) in positive-sequence rotation.

■ **Step 10**

Purpose: Verify correct voltage levels.

Method: Turn on the relay and use the ACCESS command and password OTTER to reach Access Level 1. Use the METER command to measure the voltages applied in Step 9. With applied voltages of 67 volts per phase and a potential transformer ratio of 4300:1, the displayed line-to-neutral voltages should be 288 kV. Current readings should all be zero. All line-to-line quantities should be balanced, differing from the line-to-neutral measurements by a factor of 1.73. Real power P and reactive power Q should be approximately 0. When finished, turn off the ac voltage sources.

■ **Step 11**

Purpose: Connect current sources to the relay.

Method: If three current sources are available, connect them to the relay in four-wire wye, as shown in Figure 7.4a. If only two current sources are available, wye-connect the sources as shown in Figure 7.4b to generate balanced positive-sequence currents:

11a. Connect the A-phase and B-phase current sources to the dotted A and B current input terminals.

11b. Connect both undotted A and B current input terminals to the undotted C current input terminal.

11c. Connect the dotted C current input terminal to both the A and B current source returns.

Set the current sources to deliver one ampere at the same angle as their phase voltages.

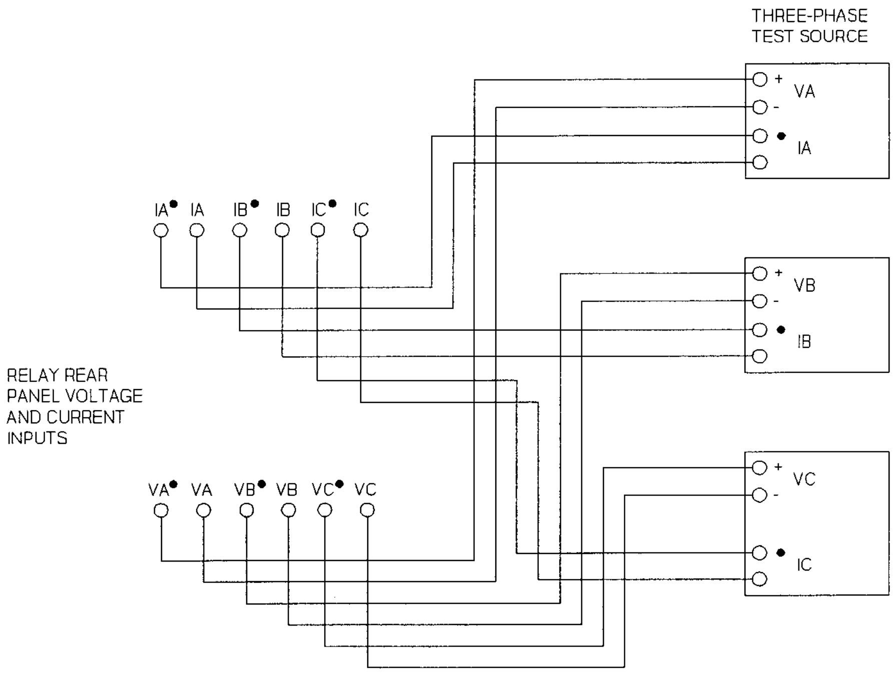


Figure 7.4a: Three-Phase Voltage and Current Source Test Connections

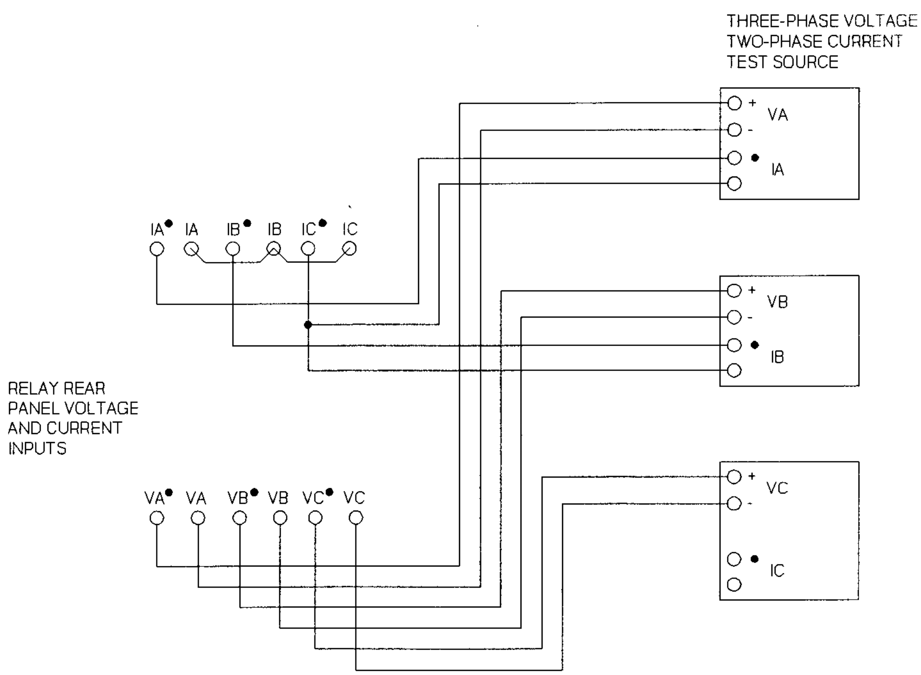


Figure 7.4b: Three-Phase Voltage and Two-Phase Current Source Test Connections

■ **Step 12**

Purpose: Verify correct current levels.

Method: Use the METER command to measure the currents applied in Step 11. With applied currents of one ampere per phase and a current transformer ratio of 600:1, the displayed line-to-neutral currents should be 600 amperes. All line-to-line quantities should be balanced, differing from the line-to-neutral measurements by a factor of 1.73. Real power P and reactive power Q should be approximately 0.

■ **Step 13**

Purpose: Verify current and voltage connections.

Method: Reduce the current source output to 0.40 amperes per phase. Set the voltage source outputs to deliver five volts per phase, balanced voltages, in phase with the currents applied. Turn on the voltage sources. Execute the METER command. Verify the voltage and current magnitudes, recalling the relay PTR and CTR settings. Power P should read approximately 15 megawatts; Q should read approximately zero megavars. If you inadvertently switched a pair of voltages or currents or rolled the polarity of a current input, the meter reading should be incorrect.

■ **Step 14**

Purpose: Verify that logic inputs assert when control voltage is applied across the respective terminal pair.

Method:

1. Set the target LEDs to display the contact inputs by typing **TARGET 7 <ENTER>**. Front panel LEDs should now follow contact inputs.
2. Apply control voltage to each input and make sure the corresponding target LED turns on. Table 7.1 lists the contact inputs.

Table 7.1: Contact Inputs

TRIPA
TRIPB
TRIPC
52A STATUS
MOD STATUS
CLOSE

3. Leave control voltage applied to the 52A and MOD STATUS inputs.

- **Step 15**

Purpose: Verify that contact outputs assert when you execute the OUT command.

Method:
1. Set the target LEDs to display the contact outputs by typing **TARGET 6 <ENTER>**. The front panel LEDs should now follow the output contacts.
2. Execute the OUT n command for each output contact. Verify that the corresponding target LED illuminates and output contact closes. Table 7.2 lists the output contacts.

Table 7.2: Output Contacts

Output	n
86BF TRIP	T
A1	1
A2	2
A3	3
A4	4
A5	5
ALARM	A

- **Step 16**

Purpose: Verify 37OP element pickup and breaker resistor thermal protection logic operation.

Method: Type **TARGET 5 <ENTER>**. This command instructs the relay to display elements in Relay Word row 5 on the front panel LEDs. Relay Word row 5 includes, from left to right:

CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q

With control voltage applied to the 52A and MOD STATUS inputs, increase A-phase current source output to 0.48 amperes per phase. A moment after A-phase current reaches 0.48 A, the relay illuminates the fourth LED from the right. This LED is labeled B, but the TARGET command requires the LED to represent the state of Relay Word bit DOPA. About two seconds after the LED illuminates, you should hear the A4 output contacts, then the 86BF TRIP output contacts close. Turn off the current and voltage sources following 86BF TRIP output assertion. Remove control voltage from the 52A and MOD STATUS inputs.

The A4 output contact closed due to CRPA bit assertion, which indicates thermal pending failure of the A-phase close resistor. The 86BF TRIP output asserted when the A-phase thermal element reached the failure energy level, causing the CTF bit to assert. Relay Word bit CRPA is set in the logic mask which controls output A4, MA4. Relay Word bit CTF is set in the M86T logic mask which controls 86BF TRIP output.

The relay generates two event reports during this test. The first is a result of TRPA bit assertion, the second is created by 86BF TRIP output assertion. The terminal screen should display each of these event summaries a few seconds after 86BF TRIP output assertion.

■ **Step 17**

Purpose: Examine the A-phase trip resistor energy content.

Method: In Access Level 1, type **HEAT <ENTER>**. The relay displays an output similar to the one shown below.

```
=>HEAT <ENTER>

RESISTOR HEAT IN PER UNIT TRIP VALUE

Example 500 kV Breaker                    Date: 6/1/92          Time: 22:13:19

ORA     CRA     ORB     CRB     ORC     CRC

0.00    4.90    0.00    0.00    0.00    0.00

=>>
```

Headings correspond to each phase open and close resistors. For example, ORA corresponds to the open resistor of phase A. CRB indicates the close resistor of phase B, and so on. The number is resistor energy per unit of the thermal element failure settings.

■ **Step 18**

Purpose: Examine an event report.

Method: In Access Level 1, type **EVENT n l <ENTER>**. The relay displays the Nth event report. Although n can be any number between 1 and 9, use 1 or 2 for this test because the relay has generated only two event reports. Press **<CTRL>S** if you would like to pause during the display. Press **<CTRL>Q** to begin scrolling again, **<CTRL>X** to cancel the report. ***Section 4: Event Reporting*** details information in event reports.

This checkout procedure demonstrates only a few relay features. For a complete understanding of relay capabilities, study the Functional Description in ***Section 2: Specifications***, the command descriptions in ***Section 3: Communications***, and ***Section 4: Event Reporting***. For more test procedures, see the Full Functional Test portion of this section.

FULL FUNCTIONAL TEST

This procedure tests relay protective and control functions more fully than the initial checkout procedure.

Equipment Required

The following equipment is necessary to complete a full functional test:

1. Communications terminal with EIA-232 serial interface
2. Data cable to connect terminal and relay
3. Source of relay control power
4. Source of synchronized three-phase voltages and at least two currents
5. Ohmmeter or contact opening/closing sensing device
6. Timer with contact inputs for start and stop
7. Plug-in mating connectors/wiring harness (Plug-in Connector Model only)

What Should Be Tested

A full functional test includes the initial checkout procedure and the additional steps described below. In general, these tests assure that the relay settings match your application rather than checking relay performance. For commissioning purposes, your company policy may require you to perform the full functional test. For maintenance purposes, a quick test of selected relay functions should suffice. For example, test operation of the Failure to Trip for Fault Current logic, each relay contact input, and each contact output.

SETTING TEST

Purpose: Ensure that the relay accepts settings.

Method:

1. Gain Level 2 Access (see ACCESS and 2ACCESS commands in ***Section 3: Communications***.

2. Change one setting. For example, change the 47Q pickup setting. Type **SET 47Q** and press **<ENTER>**.

   Following the 47Q prompt, type the new setting and press **<ENTER>**.

3. To complete the setting procedure, type **END** and press **<ENTER>**. Type **Y <ENTER>** at the prompt: OK (Y or N) ?

   The relay computes internal settings and compares them against fixed limits. If all settings fall within acceptable ranges, the ALARM contact closes momentarily as the new settings are enabled unless an alarm condition already exists.

4. Use the SHOWSET command to inspect settings. Make sure your change was accepted. Type **SHOWSET** and press **<ENTER>**.

5. Use SET and SHOWSET again to restore the initial values and check the settings.

6. Type **LOG M86T** and press **<ENTER>**.

7. Change one bit in the M86T logic mask. For example, remove the CTF bit from the third row of the Relay Word as shown in the following example.

```
LOG M86T
1 selects, 0 deselects.
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF
 1    1    0    0    0    0    0    1
 ?
FOBF FOPF 59FO 59H  ALRM TC   TB   TA
 1    0    0    0    0    0    0    0
 ?
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF
 1    0    0    0    0    0    0    1
 ? 10000000
 1    0    0    0    0    0    0    0
 ?
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB
 0    0    0    0    0    0    0    0
 ?
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q
 0    0    0    0    0    0    0    0
 ?
New M86T:
FBF  LBF  LPF  50FT 50LD 50MD 52BV TTF
 1    1    0    0    0    0    0    1
FOBF FOPF 59FO 59H  ALRM TC   TB   TA
 1    0    0    0    0    0    0    0
PDBF PDPF 87UA 87UB 87UC 86RS MDT  CTF
 1    0    0    0    0    0    0    0
CRFA CRPA TRFA TRPA CRFB CRPB TRFB TRPB
 0    0    0    0    0    0    0    0
CRFC CRPC TRFC TRPC DOPA DOPB DOPC 47Q
 0    0    0    0    0    0    0    0
OK (Y/N) ? Y
Enabled
Example 500 kV Breaker              Date: 6/1/92          Time: 22:15:42
=>>
```

8. Type **LOG M86T** and press **<ENTER>**. Make sure the bit change is present.

9. Use **LOG M86T** and SHOWSET to restore the initial values and check settings.

METER TEST

Purpose: Verify the magnitude accuracy. This test only requires a single voltage and current test source.

Method:

1. Parallel all voltage inputs by connecting terminals VA, VB, and VC with a jumper. See Figure 7.5 for the test connections.

2. Series all current inputs as shown in Figure 7.4.

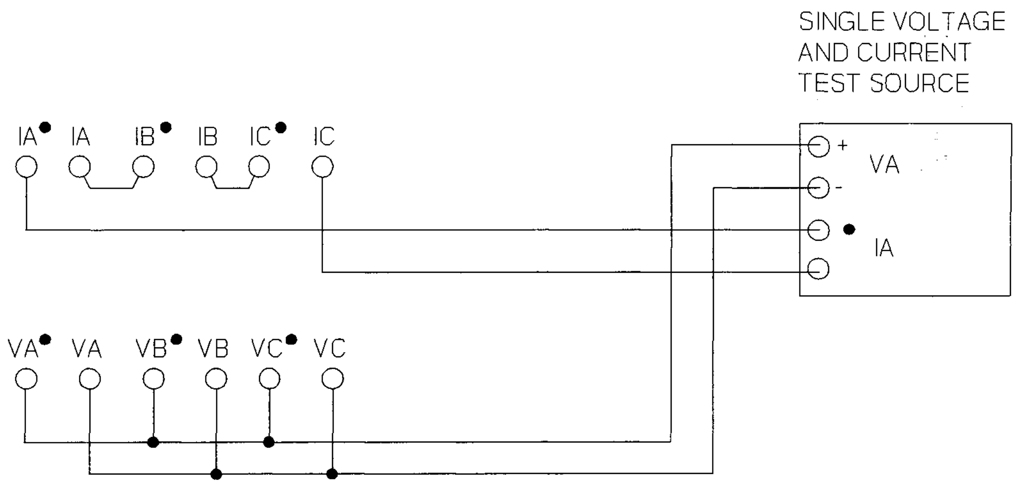


Figure 7.5: METER Test Connections

3. Apply a voltage of 50 Vac between the paralleled voltage inputs to the neutral points and a current of one ampere through the three inputs. The phase angle of the voltage and current source should be set to 0°.

4. Use the METER command to inspect measured voltages, currents, and power. Voltages VA, VB, and VC should equal the applied voltage times the potential transformer ratio setting. With the Example 500 kV Line settings, you should obtain:

   VA = VB=VC=(50 V)(4300)
   = 215 kV

   Voltages VAB, VBC, and VCA should read less than 1.5 kV.

   Similarly, currents IA, IB, and IC should equal the applied current times the current transformer ratio. With the Example 500 kV Line settings, you should obtain:

   IA = IB=IC=(1 A)(600)
   = 600 A

   Difference currents IAB, IBC, and ICA should be less than 20 amperes. The power reading, P (MW), should read:

   (VA)(IA) + (VB)(IB) + (VC)(IC) = 387 MW.

   The reactive power reading Q (MVAR) should be less than 20 MVAR.

Simultaneous application of voltage and current to the relay could cause the breaker resistor thermal elements to operate. Use the HEAT R command to reset the energy levels of the resistor thermal models after completing this test.

PHASE OVERCURRENT ELEMENT TESTS

Purpose: Verify the pickup thresholds of the 50LD, 50MD, and 50FT phase overcurrent elements.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the appropriate non-directional instantaneous phase overcurrent element. Select one of the phase overcurrent elements from the Relay Word as indicated below:

   50LD = Load detector phase overcurrent element
   50MD = MOD current detector phase overcurrent element
   50FT = Fault detector phase overcurrent element

2. Apply current to one phase and observe the pickup and dropout of each element. Record the results.

PHASE OVERVOLTAGE ELEMENT TESTS

Purpose: Verify the pickup thresholds of the 59H and 59FO phase overvoltage elements.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the appropriate phase overvoltage element. Select one of the phase overvoltage elements from the Relay Word as indicated below:

   59H = Open breaker phase overvoltage element
   59FO = Flashover phase overvoltage element

2. Apply voltage to one phase and observe the pickup and dropout of each element. Record the results.

NEGATIVE-SEQUENCE OVERVOLTAGE ELEMENT TEST

Purpose: Verify the pickup threshold of the 47Q negative-sequence overvoltage element.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the 47Q negative-sequence overvoltage element.

2. Apply voltage to one phase. Increase the phase voltage and observe the pickup and dropout of the 47Q element. Negative-sequence voltage equals

one-third of the applied single-phase voltage. Thus, with a 47Q setting of ten volts, 47Q picks up when you apply a single-phase voltage of 30 volts. Record the results.

PHASE CURRENT UNBALANCE ELEMENT TEST

Purpose: Verify the pickup threshold of the phase current unbalance elements.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the 87UA, 87UB, or 87UC phase current unbalance element. Verify the 87UB setting with the SHOWSET command.

2. Apply balanced three-phase current. Decrease the current of the phase under test until the 87U element for that phase asserts. Record the results. The element asserts when the sum of the three phase current magnitudes divided by the 87UB setting exceeds the current magnitude of the phase under test.

PHASE OVERPOWER ELEMENT TEST

Purpose: Verify the pickup threshold of the 37OP phase overpower elements.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the DOPA, DOPB, or DOPC bit. Set the 62OP timer setting to 1.00 cycle. Verify the 37OP phase overpower element setting.

2. Apply five volts to the voltage inputs of the phase under test. Increase phase current slowly and observe element pickup and dropout. The DOP_ bit should pick up when 5 V x Iphs = 37OP setting. Test each phase element in this manner. You may wish to test the elements at various values of input voltage as well, but this is not required.

3. Return the 62OP timer setting to its original value.

FAULT CURRENT BREAKER FAILURE, SCHEME 1 LOGIC TEST

Purpose: Verify operation of the Scheme 1 fault current breaker failure logic.

Method:

1. While the relay is capable of employing five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 1 by setting Schm = 1 in the relay setting group. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the FBF bit. Set 50FT in the MER mask. Verify the 62TTdo and 62FC timer settings.

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in step 1 asserts.

3. Apply A-phase current above the 50FT setting. The relay should generate an event report.

4. Assert the TRIPA input. This action causes the relay to start its 62FC timer. The external timer should also start.

5. Shortly after the TRIPA input asserts, the programmable output contact set in step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62FC timer setting.

6. Deassert the TRIPA input and shut off A-phase current.

7. This step is optional. To test Scheme 1 logic operation under conditions which could represent normal relay/breaker operation, repeat steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

8. Repeat steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

9. Assert the TRIPA input. This action should start the external timer.

10. Quickly apply A-phase current above the 50FT setting. When the TRIPA input is asserted before A-phase current is applied, A-phase current must be applied before the 62TTdo timer expires. This sequence simulates relay operation when used in a ring-bus application.

11. Shortly after applying current to the A-phase, the programmable output contact set in step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62FC timer setting.

12. Deassert the TRIPA input and shut off A-phase current.

13. This step is optional. To test Scheme 1 logic operation under conditions which could represent normal relay/breaker operation, repeat steps 9 and 10. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

14. Repeat steps 9, 10, 11, 12, and 13 (optional) for phases B and C.

FAULT CURRENT BREAKER FAILURE, SCHEME 2 LOGIC TEST

Purpose: Verify operation of the Scheme 2 fault current breaker failure logic.

Method:

1. While the relay is capable of employing five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 2 by setting Schm = 2 in the relay setting group. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the FBF bit. Set 50FT in the MER mask. Verify the 62FC timer setting.

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in step 1 asserts.

3. Apply A-phase current above the 50FT setting. The relay should generate an event report.

4. Assert the TRIPA input. This action causes the relay to start its 62FC timer. The external timer should also start.

5. Shortly after the TRIPA input asserts, the programmable output contact set in step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62FC timer setting.

6. Deassert the TRIPA input and shut off A-phase current.

7. This step is optional. To test Scheme 2 logic operation under conditions which could represent normal relay/breaker operation, repeat steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

8. Repeat steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

FAULT CURRENT BREAKER FAILURE, SCHEME 3 LOGIC TEST

Purpose: Verify operation of the Scheme 3 fault current breaker failure logic.

Method:

1. While the relay can use five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 3 by setting Schm = 3 in the relay setting group. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the FBF bit. Set 50FT in the MER mask. Verify the 62FC timer setting.

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in step 1 asserts.

3. Apply A-phase current above the 50FT setting. The relay should generate an event report.

4. Assert the TRIPA input. This action causes the relay to start its 62FC timer. The external timer should also start.

5. Shortly after the TRIPA input asserts, the programmable output contact set in step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62FC timer setting.

6. Deassert the TRIPA input and shut off A-phase current.

7. This step is optional. To test Scheme 3 logic operation under conditions which could represent normal relay/breaker operation, repeat steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

   When Scheme 3 is enabled, the TRIP input is not latched. Thus, if TRIP input deassertion occurs while phase current is applied but before 62FC timer expiration, the relay does not assert the FBF bit.

8. Repeat steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

9. Set the external timer to start when you apply current to the relay and stop when the programmable contact set in step 1 closes.

10. Assert the TRIPA input.

11. Apply A-phase current above the 50FT setting. As a result, the relay starts its 62FC timer. The external timer should also start.

12. Shortly after you apply A-phase current, the programmable output contact set in step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62FC timer setting.

13. Deassert the TRIPA input and shut off A-phase current.

14. This step is optional. To test Scheme 3 logic operation under conditions which could represent normal relay/breaker operation, repeat steps 10 and 11. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

    When Scheme 3 is enabled, the TRIP input is not latched. Thus, if the TRIP input deasserts while phase current is applied but before 62FC timer expiration, the relay does not assert the FBF bit.

15. Repeat steps 10, 11, 12, 13, and 14 (optional) for phases B and C.

FAULT CURRENT BREAKER FAILURE, SCHEME 4 LOGIC TEST

Purpose: Verify operation of the Scheme 4 fault current breaker failure logic.

Method:

1. While the relay can use five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 4 by setting Schm = 4 in the relay setting group. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the FBF bit. Set 50FT in the MER mask. Verify the 62TTpu and 62TTdo timer settings.
2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in step 1 asserts.
3. Apply A-phase current above the 50FT setting. The relay should generate an event report.
4. Assert the TRIPA input. This action causes the relay to start its 62TT timer. The external timer should also start.
5. Shortly after the TRIPA input asserts, the programmable output contact set in step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62TTpu timer setting.
6. Deassert the TRIPA input and shut off A-phase current.
7. This step is optional. To test Scheme 4 logic operation under conditions which could represent normal relay/breaker operation, repeat steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62TTpu timer expires. The FBF bit should not assert.
8. Repeat steps 3, 4, 5, 6, and 7 (optional) for phases B and C.
9. Assert the TRIPA input. Apply A-phase current 62TTpu cycles following TRIP input assertion, but before the 62TTdo timer expires. The programmable output contact set in step 1 should close, indicating FBF bit assertion.
10. Repeat step 9 for phases B and C.

FAULT CURRENT BREAKER FAILURE, SCHEME 5 LOGIC TEST

Purpose: Verify operation of the Scheme 5 fault current breaker failure logic.

Method:

1. While the relay can use five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 5 by setting Schm = 5 in the relay setting group. Using the LOGIC command, set the desired program-

mable output (A1 - A5) to follow the FBF bit. Set 50FT in the MER mask. Verify the 62FC timer setting.

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in step 1 asserts.

3. Apply A-phase current above the 50FT setting. The relay should generate an event report.

4. Assert the TRIPA input. This action starts the relay 62FC timer. The external timer should also start.

5. Shortly after TRIPA input assertion, the programmable output contact set in step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62FC timer setting.

6. Deassert the TRIPA input and shut off A-phase current.

7. This step is optional. To test Scheme 5 logic operation under conditions which could represent normal relay/breaker operation, repeat steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

   When Scheme 5 is enabled, the TRIP input is not latched. Thus, if the TRIP input deasserts while phase current is applied but before 62FC timer expiration, the relay does not assert the FBF bit.

8. Repeat steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

FAULT CURRENT BREAKER FAILURE, SCHEME 6 LOGIC TEST

Purpose: Verify operation of the Scheme 6 fault current breaker failure logic.

Method:

1. While the relay can use five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 6 by setting Schm = 6 in the relay setting group. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the FBF bit. Set 50FT in the MER mask. Verify the 62TTpu and 62FCpu timer settings.

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in step 1 asserts.

3. Apply A-phase current above the 50FT setting.

4. Assert the TRIPA input. This action causes the relay to start its 62TT timer. The external timer should also start.

5. Shortly after the TRIPA input asserts, the programmable output contact set in step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62TTpu timer setting.

6. Deassert the TRIPA input and shut off A-phase current.

7. This step is optional. To test Scheme 6 logic operation under conditions which could represent normal relay/breaker operation, repeat steps 3 and 4. This time, turn off A-phase current 0.5 to 1.0 cycles before the 62TTpu timer expires. The FBF bit should not assert.

8. Repeat steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

9. Assert the TRIPA input. Apply A-phase current 62TTpu cycles following TRIP input assertion, but before the 62TT timer one-cycle dropout time expires. The programmable output contact set in step 1 should close, indicating FBF bit assertion.

10. Repeat step 9 for phases B and C.

11. Assert the TRIPA input. At 62TTpu cycles + two cycles following TRIP input assertion, apply A-phase current. The FBF bit should not assert. Current is applied after the one-cycle window.

12. Repeat step 11 for phases B and C.

13. To test the 62FC (three-phase trip), verify that 62FCpu < 62TTpu, and wire TRIPB and TRIPC inputs in parallel with TRIPA. Then repeat steps 3 through 12, substituting 62FCpu for 62TTpu.

LOAD CURRENT BREAKER FAILURE LOGIC TEST

Purpose: Verify load current breaker failure logic operation.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the LBF bit. Set LPF in the MER mask. Verify the 62LP and 62LD timer settings.

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in step 1 asserts.

3. Apply A-phase current above the 50LD setting.

4. Assert the TRIPA input. This starts the relay 62LP and 62LD timers. The external timer should also start.

5. Shortly after TRIPA input assertion, the programmable output contact set in step 1 should close, indicating LBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62LD timer setting.

6. Deassert the TRIPA input and shut off A-phase current.

7. This step is optional. To test logic operation under conditions which could represent normal relay/breaker operation, repeat steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62LD timer expires. The LBF bit should not assert.

8. Repeat steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

9. In step 5, 62LP timer expiration can generate an event report. You can set the LPF bit in a programmable output contact mask and perform steps 3, 4, 5, 6, and 7 to test the load current pending failure logic.

52A CONTACT SUPERVISED BREAKER FAILURE LOGIC TEST

Purpose: Verify 52A supervised breaker failure logic operation.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the LBF bit. Set LPF in the MER mask. Verify the 62AP and 62AF timer settings. Verify that the function is enabled through the E62A setting.

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in step 1 asserts.

3. Assert the TRIPA input. This starts the relay 62AP and 62AF timers. The external timer should also start.

4. Shortly after TRIPA input assertion, the programmable output contact set in step 1 should close, indicating LBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62AF timer setting.

5. Deassert the TRIPA input.

6. This step is optional. To test logic operation under conditions which could represent normal relay/breaker operation, repeat steps 3 and 4. This time, deassert the 52A input 1.5 to 2.0 cycles before the 62AF timer expires. The LBF bit should not assert.

7. Repeat steps 3, 4, 5, and 6 (optional) for phases B and C.

8. In step 4, 62AP timer expiration can generate an event report. You can set the LPF bit in a programmable output contact mask and perform steps 3, 4, 5, and 6 to test the pending failure logic.

CURRENT THROUGH AN OPEN BREAKER (FLASHOVER) LOGIC TEST

Purpose: Verify current operation through open breaker logic.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the FOBF bit. Set FOPF in the MER mask. Verify the 50LD and 59FO settings, 62FP and 62FF timer settings.

2. Connect an external timer and set it to start when you apply A-phase current and stop when the programmable output you set in step 1 asserts.

3. Apply 70 volts to the voltage inputs of the phase under test.

4. Turn the voltage source off (zero volts) as you apply phase current above the 50LD setting. This action should start the external timer.

5. Shortly after you apply A-phase current, the programmable output contact set in step 1 should close, indicating FOBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62FF timer setting.

6. Shut off A-phase current.

7. Repeat steps 3, 4, and 6 three times. During the first repetition, assert the TRIPA input before applying phase voltage. During the second repetition, assert the CLOSE input (but not the TRIP input) before applying phase voltage. On the third repetition, with no inputs asserted, reduce the voltage in step 4 to some voltage above the 59FO setting but below 67 volts. In these repetitions, the relay should not assert the FOBF bit.

8. Repeat steps 3, 4, 5, 6, and 7 for phases B and C.

9. In step 5, 62FP timer expiration can cause the relay to generate an event report. You can set the FOPF bit in a programmable output contact mask and perform steps 3, 4, 5, 6, and 7 for the flashover pending failure logic.

Note: Because this test involves simultaneous application of voltage and current to the relay, the breaker resistor thermal protection elements can acquire energy. To reset resistor thermal model energies to zero, type **HEAT R <ENTER>** after each phase test.

PHASE DISCORDANCE BREAKER FAILURE LOGIC TEST

Purpose: Verify operation of the phase discordance breaker failure logic.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the PDBF bit. Set PDPF in the MER mask. Verify the 50LD setting and 62UP and 62UF timer settings.
2. Connect an external timer and set it to start when you apply A-phase current and stop when the programmable output you set in step 1 asserts.
3. Assert the CLOSE input by applying rated control voltage to the input terminals.
4. Apply A- and B-phase current above the 50LD setting. This action should start the external timer.
5. Shortly after you apply phase current, the programmable output contact set in step 1 should close, indicating PDBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the 62UF timer setting.
6. Shut off phase current.
7. Repeat steps 3, 4, and 6 twice. During the first repetition, do not assert the CLOSE input before applying phase current. During the second repetition, apply phase current below the 50LD setting. In these repetitions, the relay should not assert the PDBF bit.
8. This step is optional. To test logic operation under conditions which could represent normal relay/breaker operation, repeat steps 3 and 4. This time, turn on C-phase current 1.5 to 2.0 cycles before the 62UF timer expires. The PDBF bit should not assert.
9. Repeat steps 3, 4, 5, 6, 7, and 8 (optional) for phases A and B, the phase under test being the phase with no current applied in step 4.
10. In step 5, 62UP timer expiration can cause the relay to generate an event report. You can set the PDPF bit in a programmable output contact mask and perform steps 3, 4, 5, 6, 7, and 8 for the phase discordance pending failure logic.

CIRCUIT BREAKER CLOSE RESISTOR THERMAL FAILURE LOGIC TEST

Purpose: Verify operation of the breaker close resistor thermal failure logic.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the CTF bit. Set the CRPA, CRPB, and CRPC bits in the MER mask. Verify the 37OP, 26CP, and 26CF settings and the 62OP timer setting.

2. Connect an external timer and set it to start when you apply A-phase current and stop when the programmable output you set in step 1 asserts.

3. Assert the CLOSE input by applying dc control voltage to the CLOSE input terminals.

4. Apply five volts to the A-phase voltage input. Calculate a current magnitude such that applied power (Pa) is greater than the 37OP setting. Pa is defined:

   $$Pa = Va \times Ia \text{ watts}$$

   Where:
   Pa = applied power
   Va = applied phase voltage magnitude
   Ia = applied phase current magnitude

   Note: Applied current (Ia) must exceed 0.1 A to operate the CTF bit.

5. Calculate an estimated time to trip (TTT) by dividing the 26CF setting by Pa:

   $$TTT = \frac{26CF}{Pa} \text{ seconds}$$

6. Apply A-phase current equal to the magnitude Ia calculated above. The external timer should start upon application of A-phase current.

7. Shortly after you apply phase current, the programmable output contact set in step 1 should close, indicating TTF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the TTT value calculated above plus the 62OP timer setting.

8. Shut off phase current.

9. In step 6, accumulation of breaker resistor energy equal to the 26CP thermal pending failure value can cause the relay to generate an event report. You can set the CRPA bit in a programmable output contact mask and perform steps 3, 4, 5, 6, 7, and 8 for the close resistor thermal pending failure logic.

10. You may wish to test this logic for various values of input voltage, current, and power. Use the HEAT command to display the per unit energy content of the breaker resistor thermal models. Use the HEAT R command to reset the thermal models before each timing test.

11. Repeat steps 3 - 10 for B- and C-phases.

CIRCUIT BREAKER TRIP RESISTOR THERMAL FAILURE LOGIC TEST

Purpose: Verify operation of the breaker trip resistor thermal failure logic.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the TTF bit. Set the TRPA, TRPB, and TRPC bits in the MER mask. Verify the 37OP, 26TP, and 26TF settings and the 62OP timer setting.

2. Connect an external timer and set it to start when you apply A-phase current and stop when the programmable output you set in step 1 asserts.

3. Assert the TRIPA input by applying dc control voltage to the input terminals.

4. Apply five volts to the A-phase voltage input. Calculate a current magnitude such that applied power (Pa) is greater than the 37OP setting. Pa is defined:

   Pa = Va x Ia watts

   Where:

   Pa = applied power
   Va = applied phase voltage magnitude
   Ia = applied phase current magnitude

   Note: Applied current (Ia) must exceed 0.1 A to operate the TTF bit.

5. Calculate an estimated time to trip (TTT) by dividing the 26TF setting by Pa:

$$TTT = \frac{26TF}{Pa} \text{ seconds}$$

6. Apply A-phase current equal to the magnitude Ia calculated above. The external timer should start upon application of A-phase current.

7. Shortly after you apply phase current, the programmable output contact set in step 1 should close, indicating TTF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the TTT value calculated above plus the 62OP timer setting.

8. Shut off phase current.

9. In step 6, accumulation of breaker resistor energy equal to the 26TP thermal pending failure value can generate an event report. You can set the TRPA bit in a programmable output contact mask and perform steps 3, 4, 5, 6, 7, and 8 for the trip resistor thermal pending failure logic.

10. You may wish to test this logic for various values of input voltage, current, and power. Use the HEAT command to display the per unit energy content of the breaker resistor thermal models. Use the HEAT R command to reset the thermal models before each timing test.

11. Repeat steps 3 - 10 for B- and C-phases.

52BV LOGIC TEST

Purpose: Verify 52BV logic operation.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the 52BV bit. Using the SHOWSET command, verify the 50LD setting.

2. Apply balanced three-phase current above the 50LD setting. Assert the 52A input by applying dc control voltage to the input terminals marked 52A. Verify that the output contact set in step 1 is open.

3. Deassert the 52A input. Turn off the phase current sources. Verify that the 52BV programmable output contact is closed. Apply phase current above the 50LD setting to each phase current input in turn. Note that each time you apply current to an input, the 52BV programmable output contact opens.

4. Assert the 52A input. Note that the 52BV programmable output contact opens.

TIME DELAYED RETRIP FUNCTION TEST (SEL-2BFR)

Purpose: Verify operation of the time delayed retrip function.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the TA bit. Using the SHOWSET command, verify the 50LD setting, the RTTD setting, and the DRTE enable setting.

2. When DRTE = N: Assert the TRIP A input by applying dc control voltage to the TRIP A input terminals. Verify that the output contact set in step 1 closes.

3. Repeat steps 1 and 2 using the Relay Word TB and TC bits.

4. When DRTE = Y: Connect an external timer and set it to start when you assert the TRIP A input and stop when the programmable output you set in step 1 asserts.

5. Apply balanced three-phase current above the 50LD setting. Assert the TA input by applying dc control voltage to the TRIP A input terminals. This should start the external timer.

6. A moment later the output contact you set in step 1 should close, stopping the external timer. Take note of the time recorded. It should be approximately equal to the RTTD timer setting.

7. Repeat steps 4, 5, and 6 using the Relay Word TB and TC bits.

TIME DELAYED RETRIP FUNCTION TEST (SEL-2BFR-2)

Purpose: Verify operation of the time delayed retrip function.

Method:

1. Using the LOGIC command, set the desired programmable output (A1 - A5) to follow the TA bit. Using the SHOWSET command, verify the 50LD setting, the RTSD setting, the RTTD setting, and the DRTE enable setting.

2. Set DRTE = N. Assert the TRIP A input by applying dc control voltage to the TRIP A input terminals. Verify that the output contact set in step 1 closes.

3. Repeat steps 1 and 2 using the Relay Word TB and TC bits.

4. Set DRTE = Y. Apply balanced three-phase current above the 50LD setting. Apply dc control voltage to the TRIP A input terminal for a duration less than the RTSD setting.

5. The output contact from step 1 should not assert.

6. Connect an external timer and set it to start when you assert the TRIP A input and stop when the programmable output you set in step 1 asserts.

7. Assert the TRIP A input for a duration longer than the RTSD setting.

8. A moment later the output contact should close, stopping the external timer. Take note of the time recorded. It should be approximately equal to the RTTD timer setting.

9. Repeat steps 4 through 8 using the Relay Word TB and TC bits.

86BF TRIP AND RESET, MOD TRIP DISABLED, LOGIC TEST

Purpose: Verify operation of the 86BF TRIP reset logic when MODTrip = N.

Method:

1. Enable the 52A supervised breaker failure logic by setting E62A = Y in the relay setting group (This simplifies generation of the 86BF TRIP.). Using the LOGIC command, set the relay to issue an 86BF TRIP on assertion of the LBF bit. Set a programmable output contact (A1 - A5) to follow the 86RS bit. Verify the 62AF, 62M1, and 50MD settings.

2. Connect an external timer and set it to start when the 86BF TRIP output closes and stop when the output opens.

3. Assert the 52A input by applying dc control voltage to the 52A input terminals.

4. Assert the TRIPA input. This action starts the relay 62AF timer.

5. Shortly after TRIPA input assertion, the 86BF TRIP output should close, indicating LBF bit assertion. This action should start the external timer.

6. Deassert the TRIPA input.

7. 62m1 cycles after the 86BF TRIP output asserts, it should deassert, stopping the timer. The timer reading should be approximately equal to the 62M1 timer setting.

8. Reconnect the timer to stop when the programmable output contact set to indicate 86RS closes.

9. Repeat steps 4, 5, and 6. Approximately 5 seconds after the 86BF TRIP output opens, the 86RS bit should assert, causing the programmable output contact set in step 1 to close, stopping the external timer.

10. Note the reading on the timer. Subtract the time recorded in step 7 from the timer reading. The difference should be approximately 5 seconds.

11. Reconnect the timer to start when the programmable output contact set to indicate 86RS closes and stop when that contact opens.

12. Repeat steps 4, 5, and 6. Approximately 5 seconds after the 86BF TRIP output operates, the 86RS contact should close, then open.

13. Note the reading on the timer. The time recorded should be approximately 1 second.

14. Optional. If you apply phase current above the 50MD setting before or while the 86BF TRIP output is asserted, the relay delays deassertion of the 86BF TRIP output and assertion of the 86RS bit.

86BF TRIP AND RESET, MOD TRIP ENABLED, LOGIC TEST

Purpose: Verify operation of the 86BF TRIP reset logic when MODTrip = Y.

Method:

1. Enable the 52A supervised breaker failure logic by setting E62A = Y in the relay setting group (This simplifies generation of the 86BF TRIP.). Using the LOGIC command, set the relay to issue an 86BF TRIP on assertion of the LBF bit. Set a programmable output contact (A1 - A5) to follow the 86RS bit. Set a second programmable output contact (A1 - A5) to follow the MDT bit. Verify the 62AF, 62M1, 62M2, and 50MD settings.

2. Connect an external timer and set it to start when the 86BF TRIP output closes and stop when the programmable contact set with the MDT Relay Word bit closes.

3. Assert the 52A input by applying dc control voltage to the 52A input terminals.

4. Assert the TRIPA input. This action starts the relay 62AF timer.

5. Shortly after TRIPA input assertion, the 86BF TRIP output should close, indicating LBF bit assertion. This action should start the external timer.

6. Deassert the TRIPA input.

7. A moment after the 86BF TRIP output asserts, the contact following MDT should close, stopping the timer. The timer reading should be approximately equal to the 62M1 timer setting.

8. Reconnect the timer to start when the contact following MDT closes and stop when the 86BF TRIP contact opens.

9. Repeat steps 4, 5, and 6. A moment after the MDT output asserts, the 86BF TRIP output should deassert, stopping the external timer. Note the timer reading. It should be approximately equal to the 62M2 timer setting.

10. Reconnect the timer to stop on assertion of the contact following the 86RS bit.

11. Repeat steps 4, 5, and 6. Approximately 5 seconds after the MDT output asserts, the 86RS output should assert, stopping the external timer.

12. Note the reading on the timer. Subtract the time recorded in step 9 from the timer reading. The difference should be approximately 5 seconds.

13. Reconnect the timer to start when the programmable output contact set to indicate 86RS closes and stop when that contact opens.

14. Repeat steps 4, 5, and 6. Approximately 5 seconds after the MDT output operates, the 86RS contact should close, then open.

15. Note the reading on the timer. The time recorded should be approximately 1 second.

16. Optional. If you apply phase current above the 50MD setting before or while the 86BF TRIP output is asserted, the relay delays assertion of the MDT bit. If phase current is also above the 50LD setting the relay delays deassertion of the 86BF TRIP output. If current is above the 50LD setting or if the MOD STATUS input is asserted following assertion of the MDT bit, the relay delays assertion of the 86RS bit.

SERIAL PORTS TEST

Purpose: Verify operation of serial PORT 1.

Method: The initial checkout procedure assumes you connected a terminal to PORT 2F or PORT 2R. Set the baud rate of PORT 1 to match that of PORT 2 and switch your terminal from PORT 2 to PORT 1. Be sure you can communicate through this port. If your relay is equipped with front and rear panel PORT 2 connectors, ensure that they both operate correctly.

IRIG-B TIME CODE INPUT TEST

Purpose: Verify operation of the IRIG-B clock input port.

Method:

1. Connect a source of demodulated IRIG-B time code to the relay Auxiliary Port in series with a resistor to monitor the current. Adjust the source to obtain an "ON" current of about 10 mA.

2. Execute the IRIG command. Make sure the relay clock displays the correct date and time.

Note: A recording of the IRIG-B signal passed through a simple demodulator provides a convenient, inexpensive test of the IRIG-B port. Please contact the factory for further details.

POWER SUPPLY VOLTAGES TEST

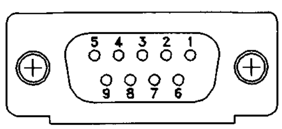
Purpose: Verify that correct output voltages are presented to PORT 1, PORT 2R, and the auxiliary port. These voltages are required by external devices which include a dc powered modem.

Method:

1. Execute the STATUS command and inspect the voltage readings for the +5 and ±15 volt supplies.

2. At the Auxiliary Port, use a voltmeter to read the +5 and ±12 volt outputs. The 12 volt outputs are derived from the 15 volt supplies using three-terminal regulators. The following pins are the read points:

<u>SEL-2BFR</u>
Pin 1: +5 Vdc if JMP12 installed
Pin 4: +12 Vdc if JMP13 installed
Pin 6: -12 Vdc if JMP14 installed



(female chassis connector, as viewed from outside panel)

Figure 7.6: SEL-2BFR Relay Nine-Pin Connector Pin Number Convention

3. Compare the +5 volt readings from the status report and voltmeter. The voltage difference should be less than 50 mV, and both readings should be within ±0.15 volts of five volts.

The 12 volt supplies should be within ±0.5 volts of their nominal values.

CALIBRATION

The SEL-2BFR Relay is factory calibrated. If you suspect that the relay is out of calibration, please contact the factory.

TROUBLESHOOTING

Inspection Procedure

Complete the following inspection procedure before disturbing the system. After you finish the inspection, proceed to the TROUBLESHOOTING TABLE.

1. Measure and record control power voltage at terminals marked + and -.
2. Check to see that the power is on, but do not turn system off if it is on.
3. Measure and record the voltage at all control inputs.
4. Measure and record the state of all output relays.
5. Inspect the cabling to the serial communications ports and be sure a communications device is connected to at least one communications port.

Troubleshooting Table

All Front Panel LEDs Dark

1. Power is off.
2. Blown fuse.
3. Input power not present.
4. Self-test failure.
5. Target command improperly set.

Note: For 1, 2, 3, and 4 the ALARM relay contacts should be closed.

System Does Not Respond to Commands

1. Communications device not connected to system.
2. Relay or communications device at incorrect baud rate or other communication parameter incompatibility, including cabling error.
3. Internal ribbon cable connector loose or disconnected.
4. System is processing event record. Wait several seconds.
5. System is attempting to transmit information, but cannot due to handshake line conflict. Check communications cabling.

6. System is in the XOFF state, halting communications. Type **<CTRL>Q** to put system in XON state.

Tripping Output Relay Remains Closed Following Fault

1. Auxiliary contact inputs improperly wired.
2. Output relay contacts burned closed.
3. Interface board failure.

No Prompting Message Issued to Terminal upon Power-Up

1. Terminal not connected to system.
2. Wrong baud rate.
3. Terminal improperly connected to system.
4. Other port designated AUTO in the relay settings.
5. Port timeout interval set to a value other than zero.
6. Main board or interface board failure.

System Does Not Respond to Faults

1. Relay improperly set. Review your settings with SET and LOGIC.
2. Improper test settings.
3. PT input cable wiring error.
4. Analog input cable between transformer-termination and main board loose or defective.
5. Check self-test status with STATUS command.
6. Check input voltages and currents with METER command and TRIGGER and EVENT sequence.

Terminal Displays Meaningless Characters

1. Baud rate set incorrectly.

2. Check terminal configuration. See ***Section 3: Communications***.

Self-Test Failure: +5 Volts

1. Power supply +5 volt output out-of-tolerance. See STATUS command.

2. A/D converter failure.

Self-Test Failure: +15 Volts

1. Power supply +15 volt output out-of-tolerance. See STATUS command.

2. A/D converter failure.

Self-Test Failure: -15 Volts

1. Power supply -15 volt output out-of-tolerance. See STATUS command.

2. A/D converter failure.

Self-Test Failure: Offset

1. Offset drift. Adjust offsets.

2. A/D converter drift.

3. Loose ribbon cable between transformers and main board.

Self-Test Failure: ROM Checksum

1. EPROM failure. Replace EPROMs.

Self-Test Failure: RAM

1. Failure of static RAM IC. Replace RAM.

Self-Test Failure: A/D Converter

1. A/D converter failure.
2. RAM error not detected by RAM test.

Alarm Contacts Closed

1. Power is off.
2. Blown fuse.
3. Power supply failure.
4. Improper EPROMs or EPROM failure.
5. Main board or interface board failure.

Firmware Upgrade Instructions

1. If the relay is in service, disable its control functions. Turn off control power to the relay.
2. Remove the relay front panel by unscrewing the five front panel screws. With the front panel removed, you can see the aluminum drawout chassis. The main board is attached to the top of the drawout chassis. The power supply and transformer assembly are attached to the bottom of the relay chassis.
3. Disconnect the power supply and transformer secondary cables from the underside of the drawout assembly.
4. Remove the drawout assembly by pulling the spacers on the bottom of the drawout chassis. You should be able to remove the assembly with your fingers. Because steps 5 and 6 involve handling electrostatic discharge (ESD) sensitive devices and assemblies, perform these steps at an ESD safe work station. This will help prevent possible damage by electrostatic discharge.
5. Note the orientation of the ICs to be replaced. Use a small screwdriver to pry the indicated ICs free from their sockets. Be careful not to bend the IC pins or damage adjacent components.
6. Carefully place the new ICs in the appropriate sockets. Check the orientation of the ICs. Be sure that each IC is in its corresponding socket. Look for IC pins that bent under or did not enter a socket hole.
7. Slide the drawout assembly into the relay chassis. Using your fingers, push the assembly in until the front of the assembly is flush with the front of the relay chassis. Reconnect

the power supply and transformer secondary cables to the receivers on the underside of the drawout assembly. Replace the relay front panel.

8. With breaker control disabled, turn relay power on and enter your settings. Execute the STATUS, METER, and TRIGGER commands to ensure that all functions are operational. Set and record your Access Level 1 and 2 passwords and the date and time. The relay is now ready to resume protective functions.

Factory Assistance

The employee-owners of Schweitzer Engineering Laboratories, Inc. are dedicated to making electric power safer, more reliable, and more economical.

We appreciate your interest in SEL products, and we are committed to making sure you are satisfied. If you have any questions, please contact us at:

Schweitzer Engineering Laboratories, Inc.
2350 NE Hopkins Court
Pullman, WA 99163-5603
Tel: (509) 332-1890
FAX: (509) 332-7990

We guarantee prompt, courteous, and professional service.

We appreciate receiving any comments and suggestions about new products or product improvements that would help us make your job easier.

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APPENDIX A - FIRMWARE VERSIONS IN THIS MANUAL

This manual covers the SEL-2BFR Relay that contains firmware bearing the following part numbers and revision numbers (most recent firmware listed at top).

Firmware Part/Revision No.	Description of Firmware
	This firmware differs from previous versions as follows: – Corrected the 62TT timer disable and reset for scheme 1 of the failure to trip for fault logic.
SEL-BFR-R118-030207 SEL-BFR-R418-030207 SEL-BFR-R707-030207 SEL-BFR-R806-030207 SEL-BFR-R907-030207 SEL-BFR-2-R101-030207 SEL-BFR-2-R401-030207	100 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 1 Amp 200 Series, 50 Hz, 5 Amp 200 Series, 50 Hz, 1 Amp
SEL-BFR-2-R100-990709 SEL-BFR-2-R400-990709	Added two new firmware versions: – These versions include a time delay on the seal-in of the trip inputs in the time delay retrip logic. This delay is accomplished with the addition of a time delay pickup timer, RTSD (Retrip Seal-In Delay). No other versions of the SEL-2BFR or SEL-BFR are affected by this modification.
	This firmware differs from previous versions as follows: – Corrected time-delayed breaker retrip logic. For single pole trip (e.g., TRIP A input asserted), the logic erroneously latched trip bit TA for any phase current above the 50LD setting level. Trip bit TA erroneously remained latched until all three phase currents fell below the 50LD setting level. The corrected logic (e.g., phase A) now latches trip bit TA when TRIP A input is asserted and the A-phase current is above the 50LD setting level. Trip bit TA then correctly remains latched until A-phase current falls below the 50LD setting level. Phases B and C operate similarly.
SEL-BFR-R117-990510 SEL-BFR-R417-990510 SEL-BFR-R706-990510 SEL-BFR-R805-990510 SEL-BFR-R906-990510	100 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 1 Amp 200 Series, 50 Hz, 5 Amp 200 Series, 50 Hz, 1 Amp

Firmware Part/Revision No.	Description of Firmware
	This firmware differs from previous versions as follows: – TB, and TC latching corrected for RTTD = 0.25.
SEL-BFR-R116 SEL-BFR-R416 SEL-BFR-R705 SEL-BFR-R804 SEL-BFR-R905	100 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 1 Amp 200 Series, 50 Hz, 5 Amp 200 Series, 50 Hz, 1 Amp
	This firmware differs from previous versions as follows: – Corrected targeting in the "Protection While Tripping Fault Current" scheme 6 logic.
SEL-BFR-R115 SEL-BFR-R415 SEL-BFR-R704 SEL-BFR-R803 SEL-BFR-R904	100 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 1 Amp 200 Series, 50 Hz, 5 Amp 200 Series, 50 Hz, 1 Amp
	This firmware differs from previous versions as follows: – 62LP and 62LD timer setting logic correction.
SEL-BFR-R114 SEL-BFR-R414 SEL-BFR-R703 SEL-BFR-R802 SEL-BFR-R903	100 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 1 Amp 200 Series, 50 Hz, 5 Amp 200 Series, 50 Hz, 1 Amp
	This firmware differs from previous versions as follows: – Seal-in inhibit of 62LP and 62LD timer logic.
SEL-BFR-R113 SEL-BFR-R413 SEL-BFR-R702 SEL-BFR-R801 SEL-BFR-R902	100 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 1 Amp 200 Series, 50 Hz, 5 Amp 200 Series, 50 Hz, 1 Amp
SEL-BFR-R112 SEL-BFR-R412 SEL-BFR-R701 SEL-BFR-R800 SEL-BFR-R901	100 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 5 Amp 200 Series, 60 Hz, 1 Amp 200 Series, 50 Hz, 5 Amp 200 Series, 50 Hz, 1 Amp

To find the firmware revision number in your relay, obtain an event report (which identifies the firmware) using the EVENT command. This is an FID number with the Part/Revision number in bold:

FID=**SEL-BFR-R112**-V1-D910212

For a detailed explanation of the FID refer to Section 4: EVENT REPORTING.

APPENDIX B - INTERNAL DIAGRAMS

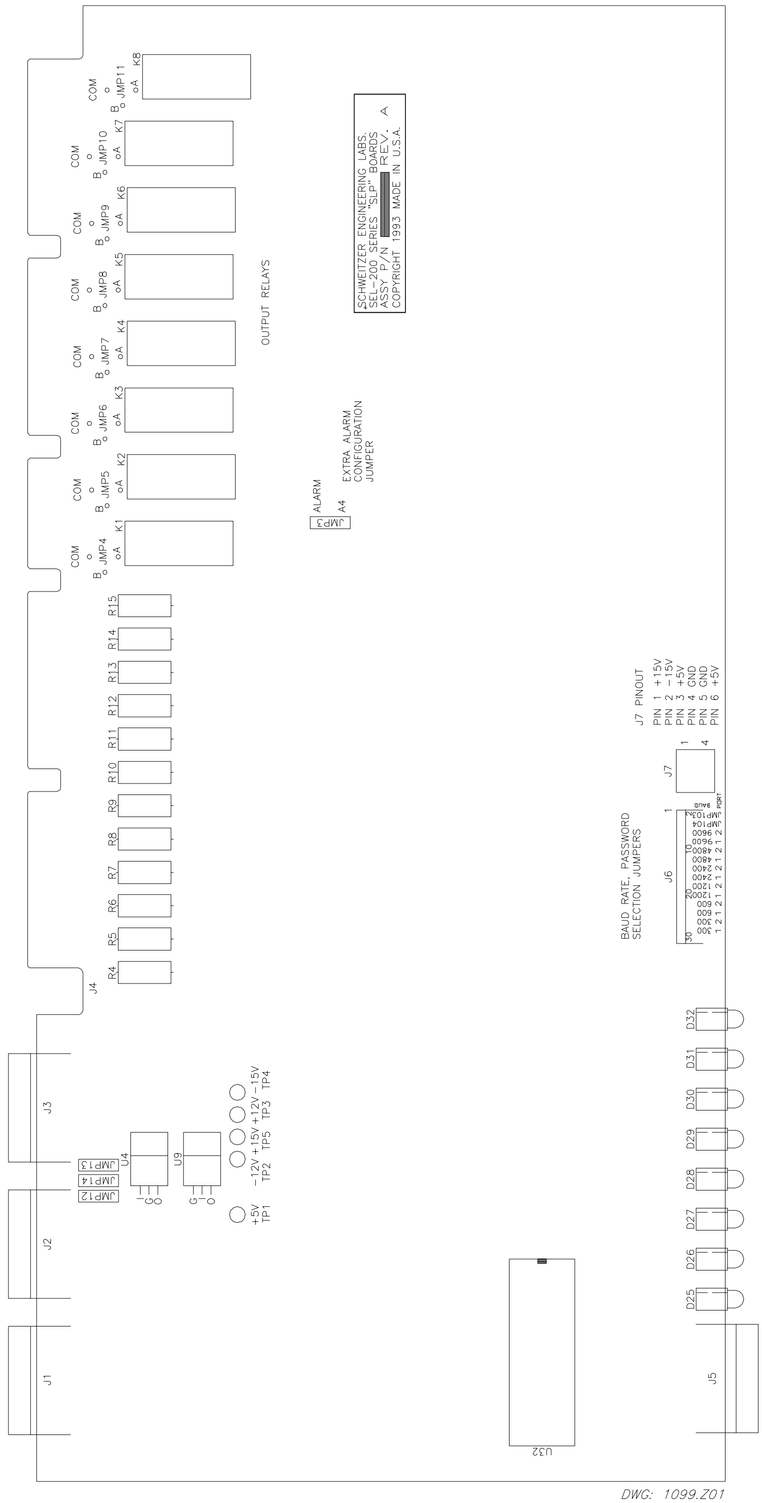


Figure B.1: SEL-2BFR, -2 Conventional Terminal Block Model Main Board Troubleshooting Test Points and Jumper Locations

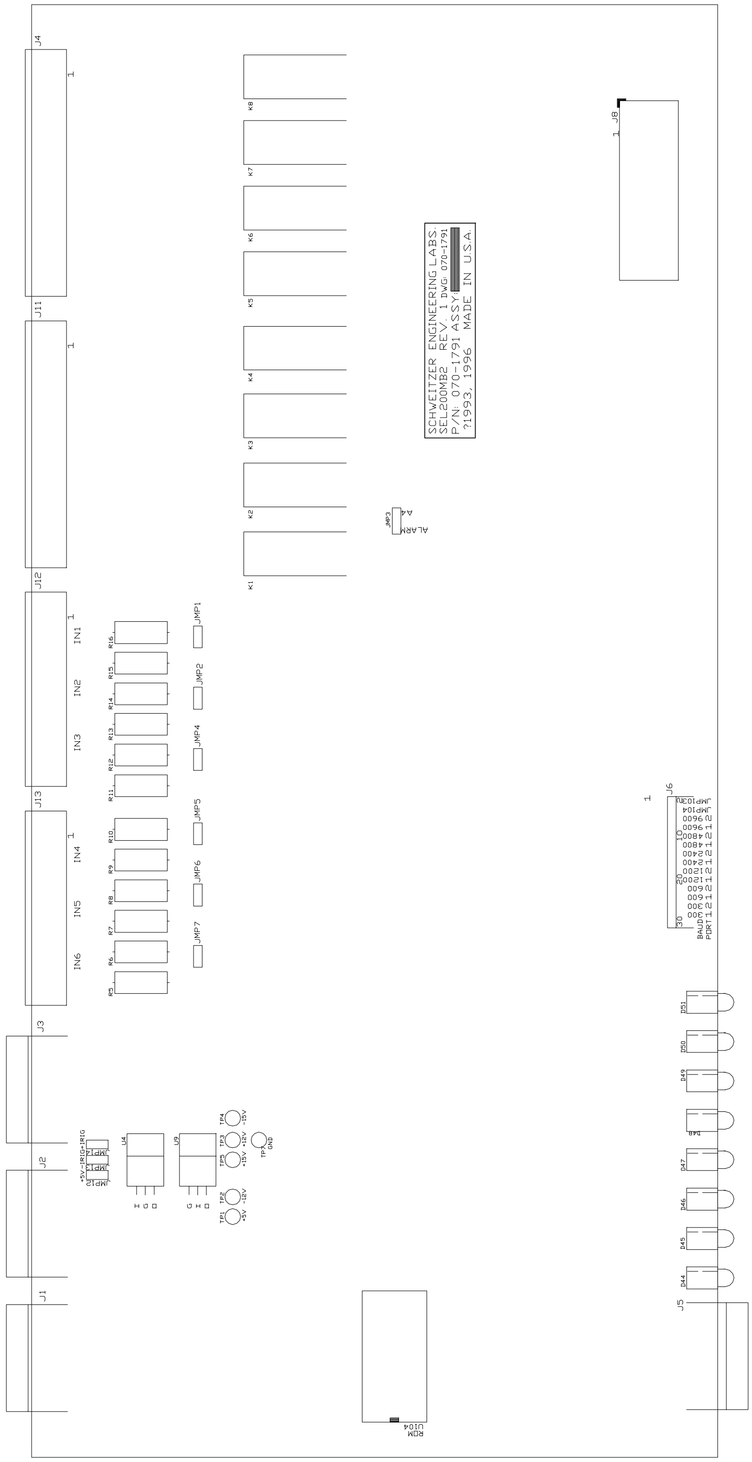


Figure B.2: SEL-2BFR, -2 Plug-in Connector Model Main Board Troubleshooting Test Points and Jumper Locations

APPENDIX C - SEL-BFR SPECIFICATIONS

SEL-BFR GENERAL SPECIFICATIONS

Voltage Inputs	0 - 150 Vac rms line-to-neutral.
Current Inputs	5 Amp Version: 15 amps per phase continuous; 500 amps for 1 second thermal rating 1 Amp Version: 3 amps per phase continuous; 100 amps for 1 second thermal rating
Output Contacts	30 amp make per IEEE C37.90 6 amp carry continuously, MOV protection provided
Optoisolated Input Ratings	24 Vdc: 15 - 30 Vdc; 4 mA at nominal voltage. 48 Vdc: 30 - 60 Vdc; 4 mA at nominal voltage. 125 Vdc: 80 - 150 Vdc; 4 mA at nominal voltage. 250 Vdc: 150 - 300 Vdc; 4 mA at nominal voltage.
Power Supply	24/48 Volt: 20 - 60 Vdc; 12 watts. 125/250 Volt: 85 - 350 Vdc or 85 - 264 Vac 10 watts nominal, 14 watts max. (all output relays energized)
Time Code Input	Relay accepts demodulated IRIG-B time code.
Communications	Two EIA-232 serial communications ports.
Dimensions	5.25" x 19.0" x 14.5" (13.34 cm x 48.26 cm x 36.83 cm) (H x W x D) Depth "D" is to end of the rear-panel terminal blocks.
Mounting	Available in horizontal and vertical mounting configurations.
Dielectric Strength	V, I inputs: 2500 Vac for 10 seconds Other: 3100 Vdc for 10 seconds (excludes EIA-232)
Operating Temperature	-40° to 158°F (-40° to 70°C)
Environment	IEC 68-2-30 Temperature/Humidity Cycle Test - six day (type tested)
Interference Tests	IEEE C37.90 SWC Test (type tested); IEC 255-6 Interference Test (type tested)
Impulse Tests	IEC 255-5 0.5 Joule, 5000 Volt Test (type tested)
RFI Tests	Type tested in field from a quarter-wave antenna driven by 20 watts at 150 MHz and 450 MHz, randomly keyed on and off one meter from relay.
ESD Test	IEC 801-2 Electrostatic Discharge Test (type tested).
Unit Weight	21 pounds (9.1 kg).
Shipping Weight	30 pounds (13.6 kg), including one instruction manual.

SEL-BFR INSTALLATION

Mounting

The relay mounts by its front vertical flanges in a 19" vertical relay rack. Use four #10 screws for mounting.

Frame Ground Connection

Connect the terminal marked GND (35 or 36) on the rear panel to frame ground for safety and performance. These terminals connect directly to the chassis ground of the instrument.

Power Connections

Connect terminals marked + (44) and - (45) on the rear panel to a source of control voltage. Control power passes through these terminals to a fuse and toggle switch, if the unit has one. The power continues through a surge filter and connects to the switching power supply. Control power circuitry is isolated from the frame ground.

Secondary Circuits

The relay presents a very low burden to the secondary current and potential circuits. Each current and voltage circuit is independent of the other circuits; there is no interconnection of current or voltage circuits inside the instrument.

The relay requires difference-voltage potentials that must be obtained from voltage transformers on both sides of the circuit breaker if flashover and thermal protection functions are to be used.

Control Circuits

The control inputs are dry. For example, to assert the 52A input, you must apply control voltage to the 52A input terminals. Each input is individually isolated, and a terminal pair is brought out for each input. There are no internal connections between control inputs.

Control outputs are dry relay contacts rated for tripping duty. A metal-oxide varistor protects each contact.

Communications Circuits

Connections to the two EIA-232 serial communications ports are made via the two nine-pin connectors labeled PORT 1 and PORT 2 on the rear panel.

Communications circuits are protected by low-energy, low-voltage MOVs and passive RC filters. You can minimize communications-circuit difficulties by keeping the length of the EIA-232 cables as short as possible. Lengths of twelve feet or less are recommended, and the cable length should never exceed 100 feet. Use shielded communications cable for lengths greater than ten feet. Modems are required for communications over long distances.

Route the communications cables well away from the secondary and control circuits. Do not bundle the communications wiring with secondary or control circuit wiring. If these wires are bundled, switching spikes and surges can cause noise in the communications wiring. This noise may exceed the communications logic thresholds and introduce errors. Route the IRIG-B clock cable away from the control wiring and secondary circuits as well.

Jumper Selection

Communication control jumpers are on the front edge of the main board. They are easily accessed by removing the top cover or front panel.

EIA-232 Jumpers

Jumper block JMP105 provides EIA-232 baud rate selection. Available baud rates are 300, 600, 1200, 2400, 4800, and 9600. To select a baud rate for a particular port, place the jumper so it connects a pin labeled with the desired port to a pin labeled with the desired baud rate.

⚠	CAUTION

Do not select two baud rates for the same port. This can damage the baud rate generator.

Password Protection Jumper

Put JMP103 in place to disable password protection. This feature is useful if passwords are not required or when passwords are forgotten.

Remote Control Enable Jumper

When JMP104 is in place, you can control relay outputs remotely with the OUT command. With JMP104 removed, OUT command execution results in an “Aborted” message.

Output Contact Soldered Wire Jumpers

Output contacts, except TRIP, can be configured as “a” or “b” contacts with soldered wire jumpers K501 through K506 (each jumper has positions A and B). The output contact/soldered wire jumper correspondence is as follows:

Output Contact	Jumper SEL-BFR
86BF TRIP (terminals 1,2)	No Jumper
86BF TRIP (terminals 3,4)	No Jumper
A1	K506
A2	K505
A3	K504
A4	K503
A5	K502
ALARM	K501

Optoisolated Input Control Voltage Jumpers

The SEL-BFR logic inputs have been improved to prevent operation of the logic input due to the conditions described in ***SEL UPDATE 94.10***. If you would like a copy of ***SEL UPDATE 94.10***, please contact the SEL factory.

The new interface board also provides field selectable input voltage selection. The operating voltages and jumper selection for each logic input are shown in the table below.

	Relay Terminals											
	39/40		41/42		43/44		45/46		47/48		49/50	
Control Voltage	JMP11	JMP12	JMP9	JMP10	JMP7	JMP8	JMP5	JMP6	JMP3	JMP4	JMP1	JMP2
250 V												
125 V		●—●		●—●		●—●		●—●		●—●		●—●
48 V	●—●	●—●	●—●	●—●	●—●	●—●	●—●	●—●	●—●	●—●	●—●	●—●

IRIG-B Installation

To synchronize the internal time clock to a source of demodulated IRIG-B time code (e.g., from a satellite clock), connect the time source to the auxiliary input connector on the rear panel. Pin definitions appear in Table C.1.

Table C.1: AUX INPUT Pin Definitions

Pin	Name	Description
2	IRIGIN HI	Positive IRIG-B input
3	IRIGIN LOW	Negative IRIG-B input
6	+5	*
7	+12	*
8	-12	*
1,5,9	GND	Ground for ground wires and shields

* Consult the factory before using these power supply outputs

The actual IRIG-B input circuit is a 56 ohm resistor in series with an optocoupler input diode. The input diode has a forward drop of about 1.5 volts. Driver circuits should put approximately 10 mA through the diode when "on."

The IRIG-B serial data format consists of a one second frame containing 100 pulses and divided into fields. The relay decodes the second, minute, hour, and day fields and sets the internal relay clock accordingly.

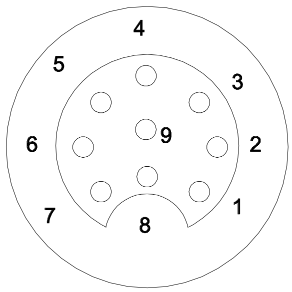
When IRIG-B data acquisition is activated either manually (with the IRIG command) or automatically, two consecutive frames are taken. The older frame is updated by one second and the two frames are compared. If they do not agree, the relay considers the data erroneous and discards it.

The relay reads the time code automatically about once every five minutes. The relay stops IRIG-B data acquisition ten minutes before midnight on New Year's Eve so the relay clock may implement the year change without interference from the IRIG-B clock. Ten minutes after midnight, the relay restarts IRIG-B data acquisition.

EIA-232 Installation

The following information contains specific details regarding communications port pinouts.

A pin definition of the nine-pin port connectors and cabling information for the EIA-232 ports appears in Figure C.1. The following cable listings show several types of EIA-232 cables. These and other cables are available from SEL. Cable configuration sheets are also available at no charge for a large number of devices. Contact the factory for more information.



(female chassis connector, as viewed from outside rear panel)

Figure C.1: Nine Pin Connector Pin Number Convention

EIA-232 Cables

Cable 123

SEL-BFR Relay 9-Pin Male Round Conxall			*DTE Device 25-Pin Male "D" Subconnector	
GND	1	———	7	GND
TXD	2	———	3	RXD
RTS	3	———	5	CTS
RXD	4	———	2	TXD
CTS	5	———	4	RTS
GND	9	———	1	GND
		┌	6	DSR
		├	8	DCD
		└	20	DTR

Cable 422

SEL-BFR Relay 9-Pin Male Round Conxall			**DCE Device 25-Pin Male "D" Subconnector	
GND	1	———	7	GND
TXD	2	———	2	TXD (IN)
RTS	3	———	20	DTR (IN)
RXD	4	———	3	RXD (OUT)
CTS	5	———	8	CD (OUT)
GND	9	———	1	GND

Cable 134

SEL-BRF Relay 9-Pin Male Round Conxall			*DTE Device 9-Pin Female “D” Subconnector	
GND	1	—	5	GND
TXD	2	—	2	RXD
RTS	3	—	8	CTS
RXD	4	—	3	TXD
CTS	5	—	7	RTS
			1	DCD
			4	DTR
			6	DSR
			9	RI

Cable 331A

SEL-BFR Relay 9-Pin Male Round Conxall			SEL-PRTU 9-Pin Male Round Conxall	
GND	1	—	1	TXD
TXD	2	—	4	RXD
RXD	4	—	2	GND
CTS	5	—	7	CTS
+12	7	—	5	RTS
GND	9	—	9	+IRIG

* DTE = Data Terminal Equipment (Computer, Terminal, Printer, etc.)
** DCE = Data Communications Equipment (Modem, etc.)

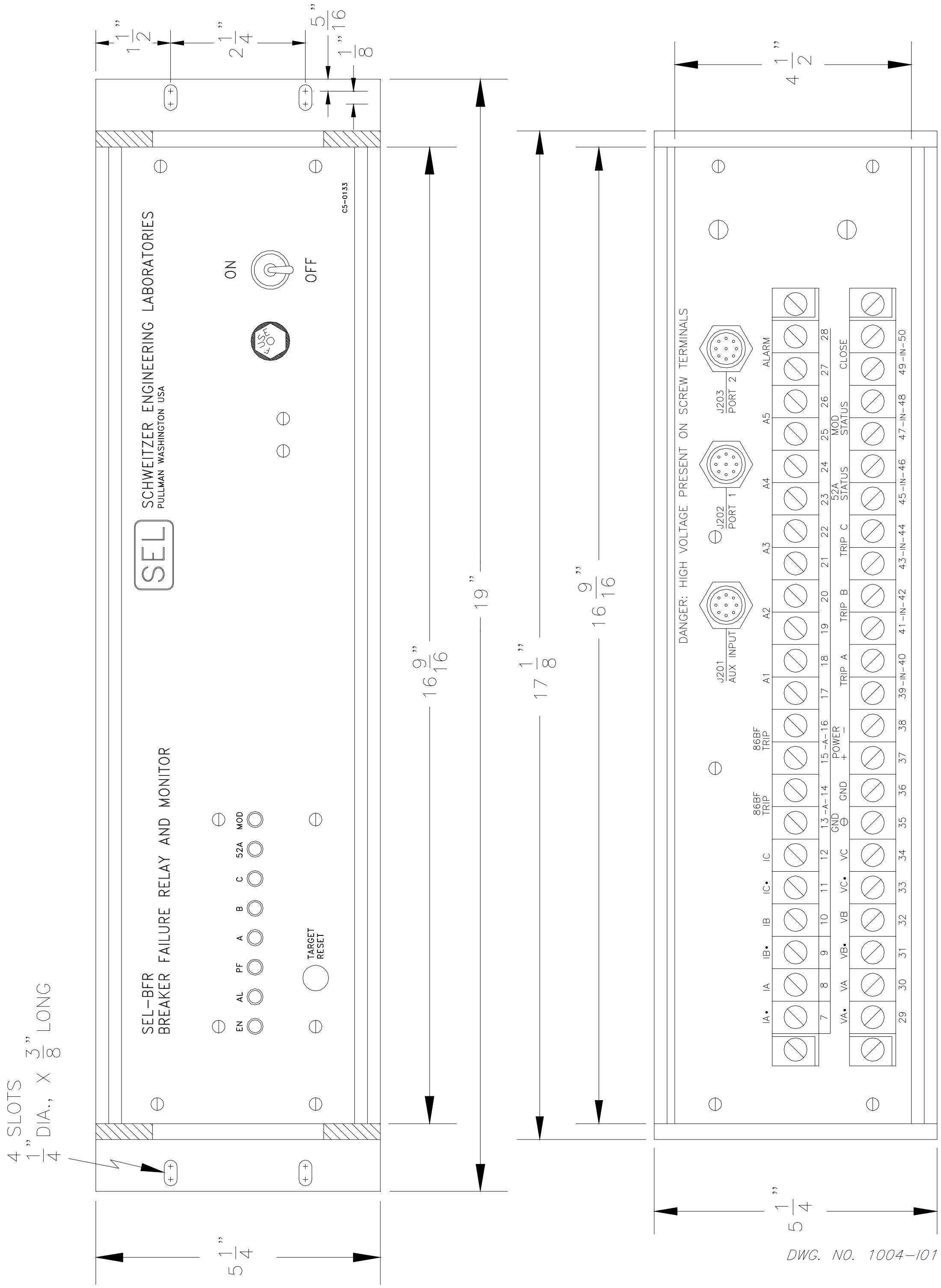


Figure C.2: Horizontal Front and Real Panel Drawings

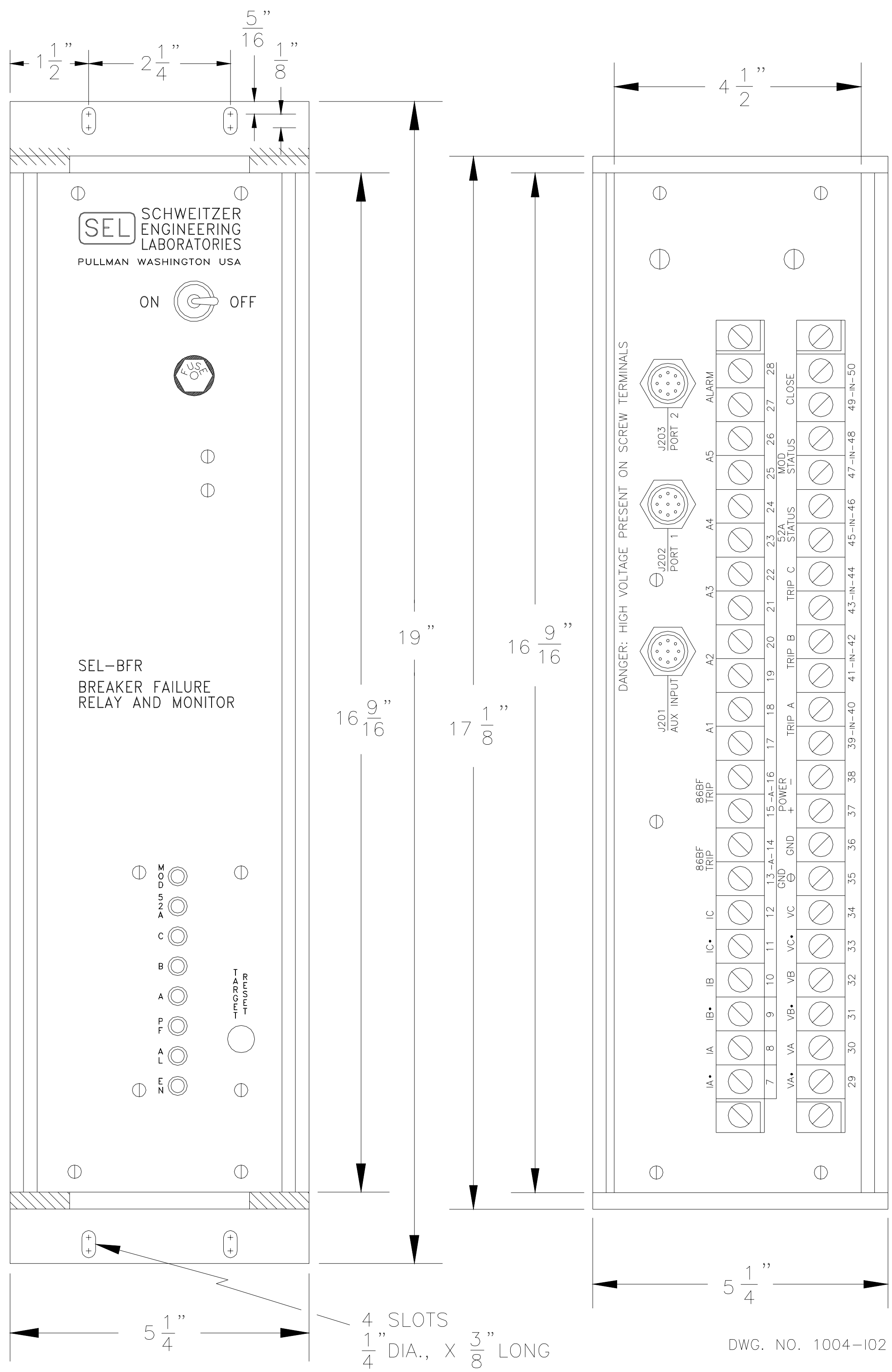


Figure C.3: Vertical Front and Rear Panel Drawings

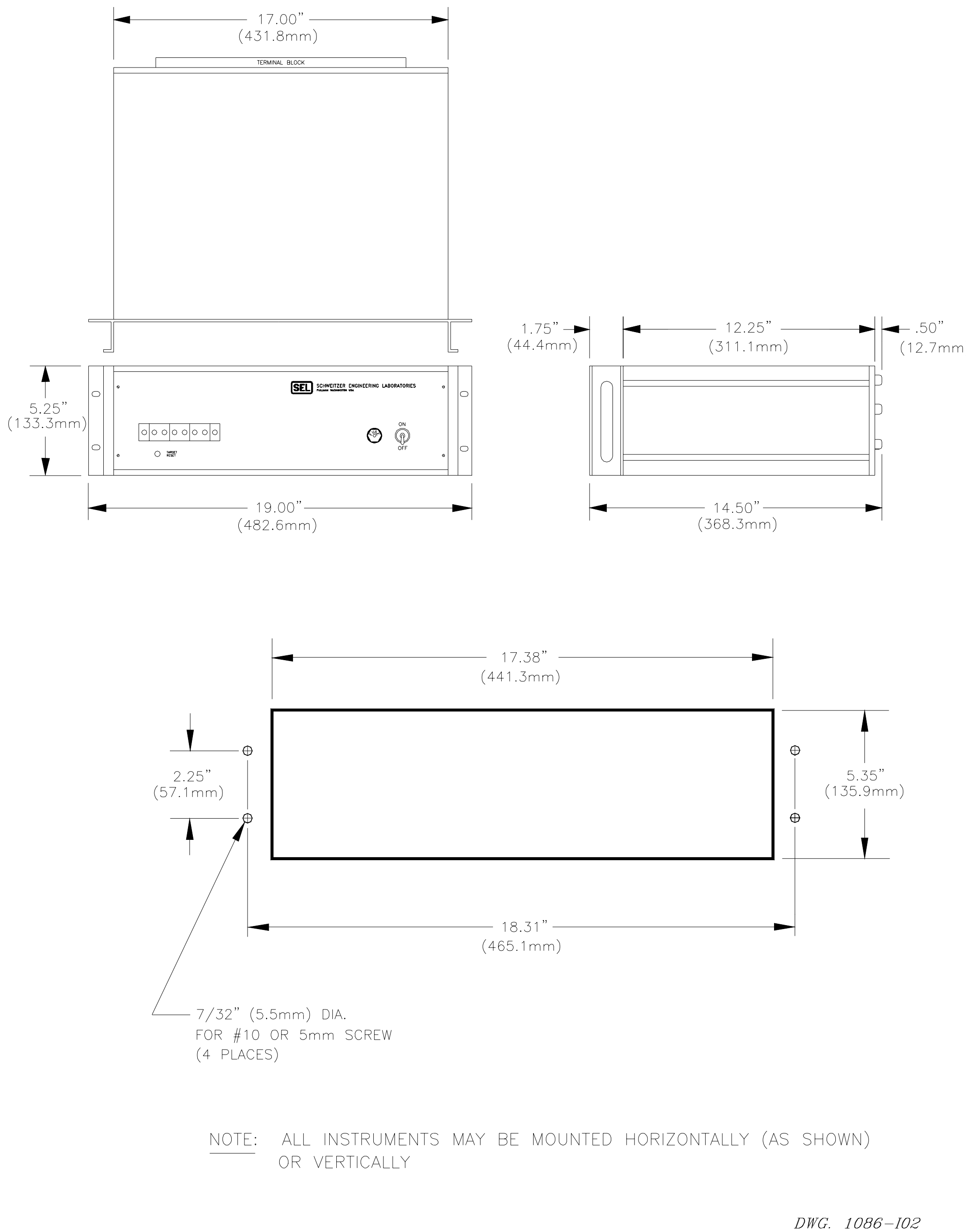


Figure C.4: Relay Dimensions, Panel Cutout, and Drill Plan

SEL-2BFR, -2/BFR COMMAND SUMMARY

Level 0

ACCESS	Answer with password (if password protection is enabled) to gain access to Level 1. Third unsuccessful attempt pulses ALARM relay.

Level 1

2ACCESS	Answer with password (if password protection enabled) to gain access to Level 2. This command always pulses the ALARM relay.
DATE m/d/y	Without arguments, relay displays date; **DATE 6/15/91 <ENTER>** sets the date to June 15, 1991. IRIG-B synchronization overrides month and day settings.
EVENT n l	Shows record for event number n, l signifies long version: **EVENT 1 l <ENTER>** shows the long form of the latest event. **EVENT 100 <ENTER>** shows the short form of the oldest event.
HEAT n	Shows internal energy of 3 close and 3 open resistors n times.
HISTORY	Shows DATE, TIME, TYPE, ENERGY, IV-TIME, and 52A-TIME for the 100 most recent events.
IRIG	Forces immediate execution of IRIG-B time code synchronization.
METER n	Shows primary current, voltage, real and reactive power n times. METER runs once; METER n runs n times (n = 1 to 255).
QUIT	Returns to Access Level 0.
SHOWSET	Displays settings without affecting them.
STATUS	Shows self-test status and ALARM history.
TARGET n	Shows data and set target lights as follows: TAR 0: Relay Targets — TAR 1: Relay Word Row 1 TAR 2: Relay Word Row 2 — TAR 3: Relay Word Row 3 TAR 4: Relay Word Row 4 — TAR 5: Relay Word Row 5 TAR 6: Relay Outputs — TAR 7: Relay Inputs TAR R: Clear Targets and return to TAR 0.
TIME h/m/s	Shows or sets time. TIME 13/32/00 sets clock to 1:32:00 PM. IRIG-B synchronization overrides this setting.
TRACE n	Traces voltage and current inputs, Relay Word bits, relay inputs and outputs n times.
TRIGGER	Triggers event report generation (event type is INT).

Level 2

LOGIC n	Shows or sets logic masks M86T, MA1, MA2, MA3, MA4, MA5. Command pulses ALARM contact closed and clears event buffers when new settings are stored.
OUT n	Closes designated output contacts if jumper JMP104 is in place (n = T, 1, 2, 3, 4, 5, or A).
PASSWORD	Shows or changes passwords: **PASSWORD 1 OTTER <ENTER>** changes Level 1 password to OTTER. **PASSWORD 2 TAIL <ENTER>** changes Level 2 password to TAIL.
SET n	Initiates setting procedure. Optional n directs relay to begin procedure at that setting. SET 50LD starts procedure at 50LD setting. SET initiates procedure at beginning. ALARM relay closes while relay computes new settings and clears long event data.

Use space, comma, semicolon, or slash to separate commands and parameters from one another. Only the first three letters of commands are significant.

SEL-2BFR, -2/BFR COMMAND SUMMARY

Level 0

ACCESS	Answer with password (if password protection is enabled) to gain access to Level 1. Third unsuccessful attempt pulses ALARM relay.

Level 1

2ACCESS	Answer with password (if password protection enabled) to gain access to Level 2. This command always pulses the ALARM relay.
DATE m/d/y	Without arguments, relay displays date; **DATE 6/15/91 <ENTER>** sets the date to June 15, 1991. IRIG-B synchronization overrides month and day settings.
EVENT n l	Shows record for event number n, l signifies long version: **EVENT 1 l <ENTER>** shows the long form of the latest event. **EVENT 100 <ENTER>** shows the short form of the oldest event.
HEAT n	Shows internal energy of 3 close and 3 open resistors n times.
HISTORY	Shows DATE, TIME, TYPE, ENERGY, IV-TIME, and 52A-TIME for the 100 most recent events.
IRIG	Forces immediate execution of IRIG-B time code synchronization.
METER n	Shows primary current, voltage, real and reactive power n times. METER runs once; METER n runs n times (n = 1 to 255).
QUIT	Returns to Access Level 0.
SHOWSET	Displays settings without affecting them.
STATUS	Shows self-test status and ALARM history.
TARGET n	Shows data and set target lights as follows: TAR 0: Relay Targets — TAR 1: Relay Word Row 1 TAR 2: Relay Word Row 2 — TAR 3: Relay Word Row 3 TAR 4: Relay Word Row 4 — TAR 5: Relay Word Row 5 TAR 6: Relay Outputs — TAR 7: Relay Inputs TAR R: Clear Targets and return to TAR 0.
TIME h/m/s	Shows or sets time. TIME 13/32/00 sets clock to 1:32:00 PM. IRIG-B synchronization overrides this setting.
TRACE n	Traces voltage and current inputs, Relay Word bits, relay inputs and outputs n times.
TRIGGER	Triggers event report generation (event type is INT).

Level 2

LOGIC n	Shows or sets logic masks M86T, MA1, MA2, MA3, MA4, MA5. Command pulses ALARM contact closed and clears event buffers when new settings are stored.
OUT n	Closes designated output contacts if jumper JMP104 is in place (n = T, 1, 2, 3, 4, 5, or A).
PASSWORD	Shows or changes passwords: **PASSWORD 1 OTTER <ENTER>** changes Level 1 password to OTTER. **PASSWORD 2 TAIL <ENTER>** changes Level 2 password to TAIL.
SET n	Initiates setting procedure. Optional n directs relay to begin procedure at that setting. SET 50LD starts procedure at 50LD setting. SET initiates procedure at beginning. ALARM relay closes while relay computes new settings and clears long event data.

Use space, comma, semicolon, or slash to separate commands and parameters from one another. Only the first three letters of commands are significant.