ABB Power T&D Company Inc.
Relay Division
Coral Springs, FL 33065

Instruction Leaflet
I.L. 41-775.2A

Type SLB-1
Breaker Pole Failure Relay
10 Amp Continuous Rating

Effective: June 1984
Supersedes I.L 41-775.2 Dated april 1984

✪ Denotes Changed Since Previous Issue

CAUTION

It is recommended that the user of this equipment become acquainted with the information in this instruciton leaflet before energizing the equipment. Failure to observe this precaution may result in damage to the equipment. Printed circuit modules should not be removed or inserted while the relay is energized unless specific instruction elsewhere in this instruction leaflet states that such action is permissible. Failure to observe this precaution can result in an undesired tripping output and cause component damage.

APPLICATION

The SLB-1 relay is used to detect circuit breaker pole disagreement. It complements other breaker-failure detecting devices that sense failure consequent to fault clearing.

Pole disagreement results from such things as: pole flashover due to lightning, faulty mechanical linkage, failure of one pole mechanism of a breaker equipped with independent pole operator or flashover of an interruptor due to low air or gas pressure.

The relay compares currents in the three poles of the breaker and if one is zero or very low and one of the others is high, this is identified as "pole disagreement" after a short time delay. The relay trips adjacent breakers through a separate lockout relay to isolate the faulty breaker.

The SLB-1 is intended for use in breaker-and-a-half or ring-bus configuration. With low magnitude load current flowing through the bus, odd phase current combinations result from unequal phase impedances and multiple paths for current flow through the bus. Unequal phase currents flowing through an individual breaker can give the false appearance of pole disagreement.

The SLB-1 contains a zero sequence voltage comparison circuit that alows this low current difference to be ignored, while permitting tripping when a hazardous pole disagreement actually exists. For higher current differences tripping can take place without the requirement that zero sequence voltage be present (or different on the two sides of the breaker).

All possible contingencies which may arise during installation, operation or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding this particular installation, operation or maintenance of this equipment, the local ABB Power T&D Company Inc. representative should be contacted.

Printed in U.S.A.

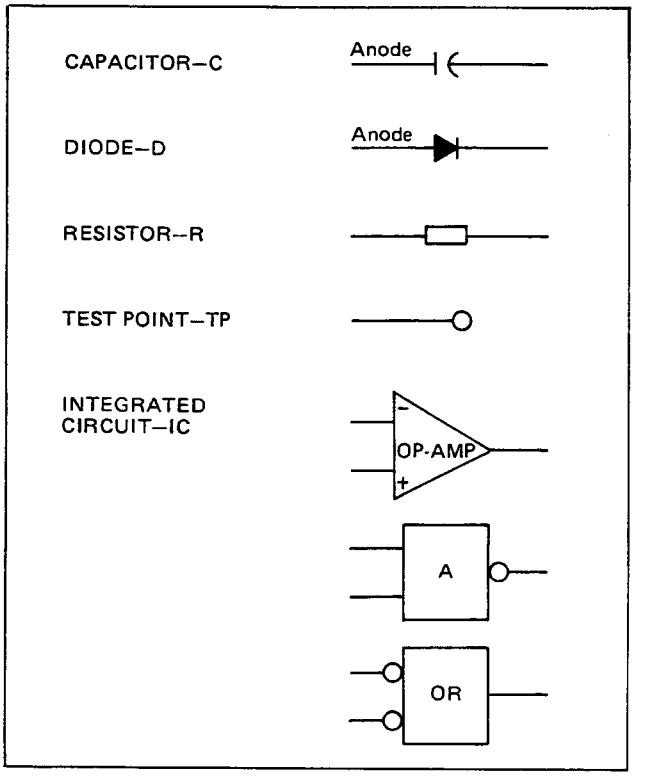
Since ground faults produce zero sequence voltage and unbalanced currents, distinction between this and pole failure must be made if very short timer settings are to be used. This is accomplished by using ΔV_o, the difference of the zero sequence voltage on the two side of the protected breaker. With all poles of the breaker closed, zero sequence voltage will always be equal on the two sides of the breaker, and $\Delta V_o = 0$. With one pole open they will not, unless the two sides of the breaker are electrically tied together through another path. In general, an open pole with ΔV_o is very hazardous and an open pole without ΔV_o is less hazardous.

CONSTRUCTION

The type SLB-1 relay is a solid state package mounted in an FT-42 case (see I.L.41-076). Referring to Fig. 3a, the circuitry consists of three current to voltage transformers, two voltage transformers, four printed circuit board assemblies, and two telephone type relays for contact output.

All the solid state circuitry for the SLB-1 relay is contained on four 5-7/8" x 4-7/8" printed circuit boards which plug into 19 pin connectors. Trimpots on the circuit boards are used for relay calibration and relay settings. The SLB-1 contains two timers for time delay applications, directly settable by two front panel mounted potentiometers with time calibrated dials. The power supply for the SLB-1 is isolated from the user's dc source through the use of an on-board DC to DC converter.

The printed circuit board assemblies, figures 5, 6, 7, and 8 show the location of all the resistors, capacitors, diodes, transistors, and integrated circuits used to perform the functions of current disagreements. Components on each PC board are identified by a letter followed by a number so that every component has a unique identification. Resistors are identified by the letter R followed by a number starting with 1. Similarly, all the other components are identified by letters and symbols as shown in the following:



NOTE

In description of the integrated circuits, the number in parentheses following the IC number will refer to the output pin of one of the two operational amplifiers contained in the linear IC package, e.g. IC1(12) refers to the op. amp. in IC1 whose output pin is 12. Digital IC'a will be identified in the same manner.

OPERATION

All the SLB-1 logic is contained on 4 circuit boards. Referring to Fig. 3a, the outputs of the 3 current to voltage transformers T1, T2, and T3 are applied to 3 identical circuite on the Signal Conditioner circuit board. Each circuit consists of a voltage limiting back-to-back zener diode, an active bandpass filter, and an absolute-value full-wave rectifier. Taking one circuit as an example, back-to-back zener diode Z1 is used to limit the transformer secondary voltage to a safe level. The bandpass filter consists of operational amplifier IC1 (12), resistors R3, R4, and P1, capacitors C1 and C2. It is designed to pass 60 hertz. P1 is a trimpot used for dc offset adjustment. The fullwave rectifier circuit consists of two operational amplifiers (IC3), one diode (D1), and four resistors (R5), (R6), (R7), and (R8). The rectifier circuit is basically a voltage follower IC3 (pins 6,7,10) and an inverting amplifier IC3 (12) whose input at the (+) terminal (pin 6) is positive regardless of the polarity of the signal at TP1.

The three rectifier outputs and the "OR" of the three outputs, through voltage follower IC2 (10), are fed to the Level Detector circuit board. This board contains four identically constructed level sensing circuits. Three are connected to the individual outputs of the Signal Conditioner board, while the fourth receives the "OR" output. Each of the level sensing circuits consists of a non-inverting variable gain amplifier, an RC filter, and a level detector. For example, one sensing circuit consists of IC6 (12) and IC8 (12) with their associated resistors, capacitors, and trimpots. The full-wave signal (proportional to I_A) at TP2 on the Signal Conditioner board is amplified by IC6 (12). P4 is used to vary the gain of the amplifier and therefore, the level of input current (I_L) at which pickup occurs. P5 is used to reduce the amplifier's dc offset to zero.

An RC filter circuit following the amplifier output produces a ripple voltage proportional to the amplitude of the input. The maximum ripple voltage is determined by the charge of capacitor C8 through diode D7 and resistor R29 while the low voltage of the ripple is controlled by C8 discharging through the resistance R28 and P6. The discharge rate is made adjustable with potentiometer P6 so as to more accurately set the pickup/dropout ratio.

A level detector, IC8 (12), is used to detect the level of this ripple voltage. When the peak of the ripple at pin 1, IC8 (12), is below the operate point of the level detector, the output of IC8 (12) will be high (+15Vdc) and the voltage at pin 2 of IC8 (12) will be approximately 9.5 volts due to the voltage divider effect of resistors R30, with R31 and R32 in parallel. Under this condition TP10 will be a logic "1". If the input current is increased to such a level that causes the peak of the ripple voltage at IC8, pin 1, to exceed the 9.5 volts at pin 2, then the level detector will switch, causing pin 12 to become "0". This logic "0" will also appear at the output, TP10, indicating pickup operation. Once the level detector switches, this causes resistors R30 and R32 to be in parallel and the voltage divider relationship

between this parallel combination and R31 causes the IC8, pin 2, voltage to become approximately 5.0 volts. This voltage is greater than the minimum level of the ripple voltage thereby allowing the level detector to remain switched. However, when the input current obtains a value 95% of pickup, this will cause the minimum ripple level to become approximately 5.0 volts which causes the level detector to switch back to a logic "1" output indicating dropout. During normal relay operation in the absense of $3V_o$, the output at TP10 is at logic "0" (the picked-up state). This keeps the AND gate IC11 (6) disabled.

As indicated before, the operation of the low set (I_L) level detectors for I_B and I_C and for the high set (I_H) "OR"ed quantity at TP7 is the same as just described for I_A. The output of the "OR"ed level detector at TP19 is first time delayed 15 ms through the circuit consisting of IC10 (12), R54, R55, R56, R57, R58, and C12 and then "AND"ed with the outputs (TP10, TP13, TP16) of the three current level detectors at IC11 (6), IC11 (8), and IC12 (8). The 15 ms delay at TP20 avoids undesired tripping due to normal breaker unsymmetries.

The outputs of the three "AND" gates IC11 (6), IC11 (8), and IC12 (8) are connected to an "OR" gate, IC12 (6) which is used to drive an output telephone type relay (TR2) through an adjustable timer, IC20 (12) on the timer board. During normal SLB-1 operation in the absence of $3V_o$, the output of the "OR" gate at TP21 is at logic "0" which keeps the timer and TR2 from operating. This occurs when all three input currents I_A, I_B, and I_C are above the I_L (low set) and I_H (high set) settings which produce logic "0"s at TP10, TP13, TP16 and logic "1" at TP20. A trip condition occurs when at least one input current drops below its I_L setting, changing one of the logic "0"s to a logic "1" and one of the currents is above the I_H setting which produces a logic "1" at TP20. The two logic "1"s enable one of the "AND" gates on the Level Detector board producing a logic "1" at the TP21, the output of "OR" gate IC12 (6). This starts the timer, IC20 (12) which, after the selected time delay causes the TR2 relay to pick up.

The operation of timer IC20 (12) is the same as described for the level detectors except the switching from logic "1" to logic "0" is determined by the charge voltage on C21 and the RC time constant of R89, C21, and P25 in series. Switching occurs when the charge on C21 overcomes the reference voltage at pin 2 of IC20 produced by the voltage divider resistors R90 and R91. This occurs in one time constant which is variable depending the setting of P25. P5 is a front panel mounted potentiometer with a dial marked 0.2 to 4.0 seconds.

The SLB-1 relay includes circuitry for supervising the detection logic with $3E_o$ ($3V_o$) measured on both sides of the breaker in breaker-and-a-half and ring bus applications. Circuits for detecting the magnitude of $3V_o$ on each side of the breaker, both individually and differentially (ΔV_o), are provided on the $3V_o$ Logic board. Each $3V_o$ quantity appearing at transformers T4 and

T5 is sensed by individual level detectors similar to those in the current circuits less the 60 Hz filters. Links 1, 2, and 3 at the inputs to the level detectors permit selection of either individual $3V_o$ or $\Delta 3V_o$ operation. For $\Delta 3V_o$, all three links should be in Position 1. This connects the secondaries of T4 and T5 in opposition and the result is applied to one level detector circuit, IC13 (10), IC16(12), IC16 (10), and IC14(10). Individual $3V_o$ detection is obtained with all three links in Position 2.

In addition to the two $3V_o$ level detecting circuits, a I_M (medium set) level detector, IC13(12) and IC14(12), is included on the $3V_o$ Logic board. The configuration of this detector is identical to the I_H (high set) detector. The outputs of the two $3V_o$ detectors at pin 10 of IC 14 and pin 10 of IC17 are "OR"ed in IC19(8) and then "AND"ed with the I_M (medium set) detector in IC19(3). The output of this "AND" gate at TP32 is time delayed 15 ms by the IC10 (12) circuit on the Level Detector board before being "AND"ed with the I_L (low set) detectors for operation of the timer associated with the TR2 output relay.

The $3V_o$ "OR"ed output at pin 8 of IC19 is also "AND"ed with the I_L (low set) output at TP21 in IC18 (6) to provide an operate signal to a second adjustable timer, IC20(10), which controls the TR1 output relay. This timer is identical to that controlling TR2 except with one-fourth the range (0.05 to 1.0 seconds) adjustable through front panel mounted P26. An additional input to the IC(18) "AND" gate provides an inhibit signal to inhibit the operation of the TR1 timer when single or selective pole tripping is used.

The inhibit circuit consists of an input buffer (R77, R78, R79, R80, Z5, Z6, and C15), optical isolator IC15, and a 5 ms "ON" 500 ms "OFF" timer IC17(12). The operation of this timer is the same previously described. The diodes D20, D21, D22, D23 are used to control the charge and discharge paths for C17.

All the level detectors adjustments for the SLB-1 relay consist of setting two potentiometers (one for pickup and one for dropout) as shown in Table 1. Though the level detectors are preset at the factory to the recommended values of I_L = 20 mA, I_M = 65 mA, I_H = 300 mA, and $3V_o$ = 6 volts, they can be adjusted for other values if required for the application.

Detector	Pickup Pot.	Dropout Pot.
A Phase I_L	P4	P6
B Phase I_L	P7	P9
C Phase I_L	P10	P12
High Set I_H	P13	P15
Medium Set I_M	P16	P18
$3V_{o1}$	P19	P21
$3V_{o2}$	P27	P29

The dc power supply for the SLB-1 contains a DC-to-DC converter on the Timer board which isolates the user's dc source from the relay's electronic circuits. The telephone relays, TR1 and TR2, are powered directly from the external source through current limiting resistors RDC3 and RDC4. However, the timers which drive the telephone relays are isolated from the external source by means of Optical Isolators, IC22 and IC23.

CHARACTERISTICS

A. Current Rating

Continuous	10 Amperes per phase
One Second	200 Amperes per phase

B. Operating Time

Time Equal to Timer Settings

C. Current Burden Per Phase

1A	.025VA

D. DC Burden

0.25 Amps continuous

E. Pickup Ranges

I_L - variable from 15 to 100 mA
I_M - variable from 50 to 200 mA
I_H - variable from 100 to 500 mA
$3V_{o1}$ - variable from 6 to 20 volts
$3V_{o2}$ - variable from 6 to 20 volts

Dropout

94 to 98% of all pickup values

F. Tripping Condition

1. For $3V_o$ or $\Delta 3V_o$ equal to less than 6 volts, at least one phase conducting greater than the I_H setting while at least one phase is conducting less than the I_L setting.

2. For $3V_o$ or $\Delta 3V_o$ equal to 6 or more volts, at least one phase conducting greater than the I_M setting while at least one phase is conducting less than the I_L setting.

G. Restraining Conditions

1. For $3V_o$ or $\Delta 3V_o$ equal to less than 6 volts, sudden increase of current from 0.0 ampere to any value greater than the I_H setting in all phases, whether balanced or not.

2. For $3V_o$ or $\Delta 3V_o$ equal to 6 to 20 volts, any sudden change in current, increase or decrease, balanced or not, as long as the minimum current is greater than the I_M setting in all three phases.

3. Simultaneous interruption of three currents, balanced or not.

H. Timer Delay Range and Voltage Rating

Time Delay Range (Seconds)	Voltage (Volts dc)
.05 - 1.0	48
.05 - 1.0	125
.05 - 1.0	250
0.2 - 4.0	48
0.2 - 4.0	125
0.2 - 4.0	250

Timer Reset Time

TR drop-out time = .01 sec. or less.

I. Frequency - 50/60 Hz

SETTINGS

Setting are required for I_L, I_M, I_H, $3V_{o1}$ and $3V_{o2}$. Link selection is required for $3V_o$ and $\Delta 3V_o$.

I_L

I_L, the low-set overcurrent unit, is adjustable between 15 and 100 mA. When used in a 2 breaker per line section, bus arrangement (breaker-and-a-half, ring bus, etc), the setting must be sufficiently high to override any back-feed effect to the ct of the protected breaker that could cause incorrect sensing of breaker condition. No load condition, for while pole disagreement detection is required, should produce a current greater than I_L in the low phase, with zero current in the ct primary. With high quality ct's, used on full tap, a setting of 20 mA will usually suffice.

I_M

I_M is the medium-set current detector. It is adjustable from 50 to 200 mA and functions with the zero sequence voltage detector and I_L to detect pole-disagreement. If a faulty breaker feeds an unloaded line, the "sound" phases will have current equal to line charging current. The I_M setting dictates the minimum line length for which pole disagreement can be detected at no load. It therefore, should be set quite low. To determine the maximum setting, I_M (max) = 1.2 I_C/R_C is used, where I_C is the total line charging current per phase. R_C is the ct ratio and 1.2 is a margin factor. Higher settings may be used, but pole disagreement detection based on line charging current will not be possible.

I_H

The I_H high-set overcurrent unit will respond irrespective of $3V_o$ level. It must be set with sufficient margin above I_L, that load unbalance can never cause I_H to operate and I_L to be reset. Experience indicates that a 300 mA setting is adequate. Setting over the range of 100 to 500 mA is possible by adjusting potentiometer P13.

$3V_o$

The $3V_o$ setting has a different meaning depending on the link position selection on the "$3V_o$ Sensing Logic" PC board. In link position 1 (3 links), the level sensing device has $\Delta 3V_o$ (the difference between the two zero sequence voltage inputs) applied to it. With all poles of the breaker closed, this will be zero. A difference indicates one or more poles are open and that a system neutral shift has occurred. The minimum 6 volt setting of P19 should normally be suitable, but a setting as high as 20 volts may be used. The position of P27 is of no significance when using link position 1.

When link position 2 is used the two $3V_o$ units operate as individual level detectors. The operation of either satisfies the logic. A 6 volt setting of potentiometers P19 and P27 may be used, but note that any nearby ground fault may satisfy the $3V_o$, I_M, I_L logic and therefore it may be desired to set timer T_1 much longer for this link position. Link position 1 is normally recommended.

T_1

This timer may be set for the minimum 50 ms on left dial P26

when link position 1 is used for $\Delta 3V_o$. When link position 2 is used, either a time sufficiently long to allow all normal clearing must be allowed; possibly 0.5 second, or possible overtripping at no load must be permitted consequent to a ground fault.

Where single pole tripping is used, an inhibitor input from the tripping relays prevents tripping through the short timer T_1 . This prevents undesired tripping during the period when one pole of the breaker deenergizes a line to ground fault.

T_2

T_2 timer causes tripping for those cases where zero sequence voltage is not present across the protected breaker. Since $3V_o$ is a significant indicator of breaker hazard, T_2 may be set much longer than the 50 ms setting of T_1 . 0.5 seconds for retrip of the protected breaker and alarm is a recommended time. T_2 adjustments over the range of 0.2 to 4.0 seconds are made with Right Dial P25.

Where link position 2 is used for $3V_o$, T_2 may be set for 1.0 second, to energize the lockout relay and trip adjacent breakers.

INDICATING CONTACTOR SWITCH (ICS)

The only setting required on the ICS unit is the selection of the 0.2 or 2.0 ampere tap. This selection is made by connecting the lead located in front of the tap block to the desired setting by means of the connecting screw. The tap should be chosen to be compatible with the trip current that will flow through the coil The ICS unit contacts will close and the operation indicator target will drop for any current above tap value.

EXTERNAL CONNECTIONS

Fig. 4 shows the external connections for the type SLB-1 relays.

RECEIVING ACCEPTANCE

Make a visual inspection to make sure that there are no loose connections, broken resistors, or broken resistor wires.

RELAY CHECK

A. Refer to figure 3.

B. Connect per test figure 10 and apply rated dc voltage.

C. Apply I_A = 15mA, I_B = I_C = 400mA, $3V_o$ = 0 volts. A logic "1" (greater than 8 volts) should be observed at terminal 14 or TP21 of the Level Detector circuit board, and telephone relay TR2 should operate.

Apply I_B = 15mA, I_A = I_C = 400mA, $3V_o$ = 0 and check relay output per step C.

Apply I_C = 15mA, I_A = I_B = 400mA, $3V_o$ = 0 and check relay output per part C.

D. Apply I_A = 15mA, I_B = I_C = 100mA, $3V_o$ = 10 volts rms. A logic "1" (greater than 8 volts) should be observed at terminal 14 (TP21) of the Level Detector circuit board and at terminal 17 (TP31) of the $3V_o$ Logic circuit board.

Telephone relays TR1 and TR2 should operate.

Apply I_B = 15mA, I_A = I_C = 100mA, $3V_o$ = 10 volts and check relay output per step C.

Apply I_C = 15mA, I_A = I_B = 100mA, $3V_o$ = 10 volts and check relay output per part C.

TIMING CHECK

SLB-1 timers and their dials are calibrated and set at the factory and should not be disturbed in the field. However, the maximum calibration point on the timer dial(s) may be checked to insure that the timers are operating properly.

The recommended test circuit for this check is shown in figure 9. To check the TR1 timer, block the TR2 telephone relay operate contacts with a piece of insulation material. To check the TR2 timer, the TR1 relay operate contacts should be blocked.

A. Connect per test figure 9 and apply rated dc voltage. Switch (S1) should be in the closed position.

B. Set I_A , I_B , & I_C = 1.0 amperes and $3V_o$ = 10 volts. Reset the electronic timer to zero.

C. Set SLB-1 timer dial at the maximum calibration mark and open switch (S1). The electronic timer should display the time set on the SLB timer dial to within + 3%.

D. Return setting to value desired for the application and unblock telephone relay contacts.

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. Mount the relay vertically by means of the rear mounting stud or studs for the type FT projection case or by means of the four mounting holes on the flange for the semi-flush type FT case. Either the stud or the mounting screws may be utilized for grounding the relay. External toothed washers are provided for use in the locations shown on the outline and drilling plan to facilitate making a good electrical connection between the relay case, its mounting screws or studs, and the relay panel. Ground wires are affixed to the mounting screws or studs as required for poorly grounded or insulating panels. Other electrical connections may be made directly to the terminals by means of screws for steel panel mounting or to the terminal stud furnished with the relay for thick panel mounting. The terminal stud may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench.

For detail information on the FT case refer to I.L. 41-076.

ROUTINE MAINTENANCE

All relays should be checked at least once every year at such time intervals as may be dictated by experience to be suitable to the particular application.

CALIBRATION

Use the following procedure for calibrating the relay if the relay adjustments have been changed or disturbed. This procedure should not be used unless it is apparent the relay is not in proper working order.

The SLB-1 relay can best be calibrated in the chassis using a board extender, style S#644B315 G03.

Using the test setup in figure 10 and referring to the internal schematic diagram, figure 3a, the following procedure should be used in the calibration of the SLB-1 relay. (All voltages are referred to common unless otherwise notes).

A. DC Offset Adjustments

1. Remove the Signal Conditioner board and insert the board extender in its place. Next, plug the Signal Conditioner board into the board extender. Using the millivolt DC range of a DVM:

   a. Connect a jumper from terminal 14 to terminal 8 and adjust P1 so that the voltage at TP1 is 0.0 ± 5.0 mv DC.

   b. Connect a jumper from terminal 16 to terminal 11 and adjust P2 so that the voltage at TP3 is 0.0 ± 5.0 mv DC.

   c. Connect a jumper from terminal 3 to terminal 9 and adjust P3 so that the voltage at TP5 is 0.0 ± 5.0 mv DC.

   d. Replace the Signal Conditioner board in the relay chassis.

2. Remove the Level Detector board and insert the board extender in its place and plug the Detector board into the board extender.

   a. Connect a jumper from terminal 2 to terminal 10 and adjust P5 so that the voltage at TP8 is 0.0 ± 5.0 mv DC.

   b. Connect a jumper from terminal 4 to terminal 10 and adjust P8 so that the voltage at TP11 is 0.0 ± 5.0 mv DC.

   c. Connect a jumper from terminal 5 to terminal 10 and adjust P11 so that the voltage at TP14 is 0.0 ± 5.0 mv DC.

   d. Connect a jumper from terminal 12 to terminal 10 and adjust P14 so that the voltage at TP17 is 0.0 ± 5.0 mv DC.

   e. Replace the Level Detector board in the relay chassis.

3. With the $3V_o$ Logic board in the board extender, put links 1, 2 and 3 in position 2.

   a. Connect a jumper from terminal 18 to terminal 9 and adjust P20 so that the voltage at TP24 is 0.0 ± 5.0 mv DC.

b. Connect a jumper from terminal 11 to terminal 13 and adjust P28 so that the voltage at TP28 is 0.0 ± 5.0 mv DC.

c. Connect a jumper from terminal 12 to terminal 10 and adjust P17 so that the voltage at TP22 is 0.0 ± 5.0 mv DC.

d. Remove the jumper and replace the 3Vo Logic circuit board in the relay chassis.

B. I_H Level Detector (Refer to Fig. 6). Note: All the pickup and dropout adjustment potentiometers are located on the front edges of the circuit boards.

1. Connect per test diagram Fig. 10 and apply rated dc voltage. Place the Level Detector Module on the extender card and turn P6, P9, P12 and P15 full clockwise.

2. Apply I_A = 300 mA, I_B = I_C = 0, $3V_O$ = 0.

3. With an oscilloscope, monitor terminal 14 or TP21 on the Level Detector board, and adjust P13 until a logic "1" (greater than 8 volts) just appears at terminal 14.

4. Reduce I_A to about 290 mA and adjust the dropout potentiometer P15 until a logic "0" (less than 2 volts) just appears at terminal 14.

5. Increase I_A and logic "1" output should be observed as current reaches 300 mA.

6. Reduce I_A and recheck per step 4. Dropout should occur within the 300 to 290 mA range.

C. I_M Level Detector (Refer to Fig. 8).

1. Connect per test diagram Fig. 10 and apply rated dc voltage. Connect a jumper from TP27 to term. 10 on the $3V_O$ module.

2. Apply I_A = 65 mA, I_B = I_C = 0.

3. Monitor terminal 14 or TP21 on the Level Detector board, and adjust the pickup potentiometer P16 on the $3V_O$ Module until a logic "1" appear at terminal 14.

4. Reduce I_A to about 63 mA and adjust the dropout potentiometer P18 on the $3V_O$ Module until a logic "0" appears at term. 14.

5. Increase I_A and logic "1" output should be observed as current reaches 65 mA.

6. Reduce I_A and recheck per step 4.

7. Remove the jumper from TP27.

D. $3V_O$ Level Detector (Refer to Fig. 8).

1. Connect per test diagram Fig. 10 and apply rated voltage. Turn P18, P21, and P29 full clockwise.

2. Apply I_A = 100 mA, I_B = I_C = 0, $3V_O$ = 6 volts.

3. Monitor terminal 14 or TP21 on the Level Detector board, and adjust P19 on the $3V_O$ Logic board until a logic "1" appears at terminal 14.

4. Reduce $3V_O$ to 5.8 volts and adjust P21 on the 3V Logic board until a logic "0" appears at terminal 14 on the Level Detector board.

5. Recheck steps 3 and 4.

6. Next apply $3V_O$ = 6 volts to relay terminals 18 and 19 and repeat steps 2 through 5 while adjusting P27 for pickup and P29 for dropout.

E. I_L Current Level Detector (Refer to Fig. 6).

1. Connect per test diagram Fig. 10 and apply rated dc voltage.

2. Apply I_A 20 mA, I_B = I_C = 1.0 Amp, $3V_O$ = 0.

3. Monitor terminal 14 or TP21 on the Level Detector board and adjust P4 until a logic "0" (less than 2 volts) appears at terminal 14.

4. Reduce I_A to 19 mA and adjust P6 until a logic "1" appears at terminal 14 on the Level Detector Module.

5. Recheck steps 3 and 4.

6. Adjust P7 and P9 per steps 3, 4, and 5 with I_B = 20 mA, I_A = I_C = 1.0 Amp.

7. Adjust P10 and P12 per steps 3, 4, and 5 with I_C = mA, I_A = I_B = 1.0 Amp.

8. Replace the Level Detector Module in the chassis.

F. Fast Timer Inhibit Check (Refer to Fig. 8).

1. Connect per test diagram Fig. 10 and apply rated dc voltage. Place $3V_O$ Module on the Extender Card.

2. Apply I_A = 0, I_B = I_C = 1.0 Amp, $3V_O$ = 10 volts.

3. Monitor terminal 17 or TP31 on the 3 V_O Logic board. Terminal 17 should be at logic "1" and telephone relays TR1 and TR2 should be picked up.

4. Apply rated dc voltage to Inhibit relay terminals 11 and 12 (+). Terminal 17 should switch to logic "0" and telephone relay TR1 should drop out.

5. Replace the $3V_O$ Module in the chassis.

G. Timing Check

Check timers using procedure given under RECEIVING ACCEPTANCE.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data.

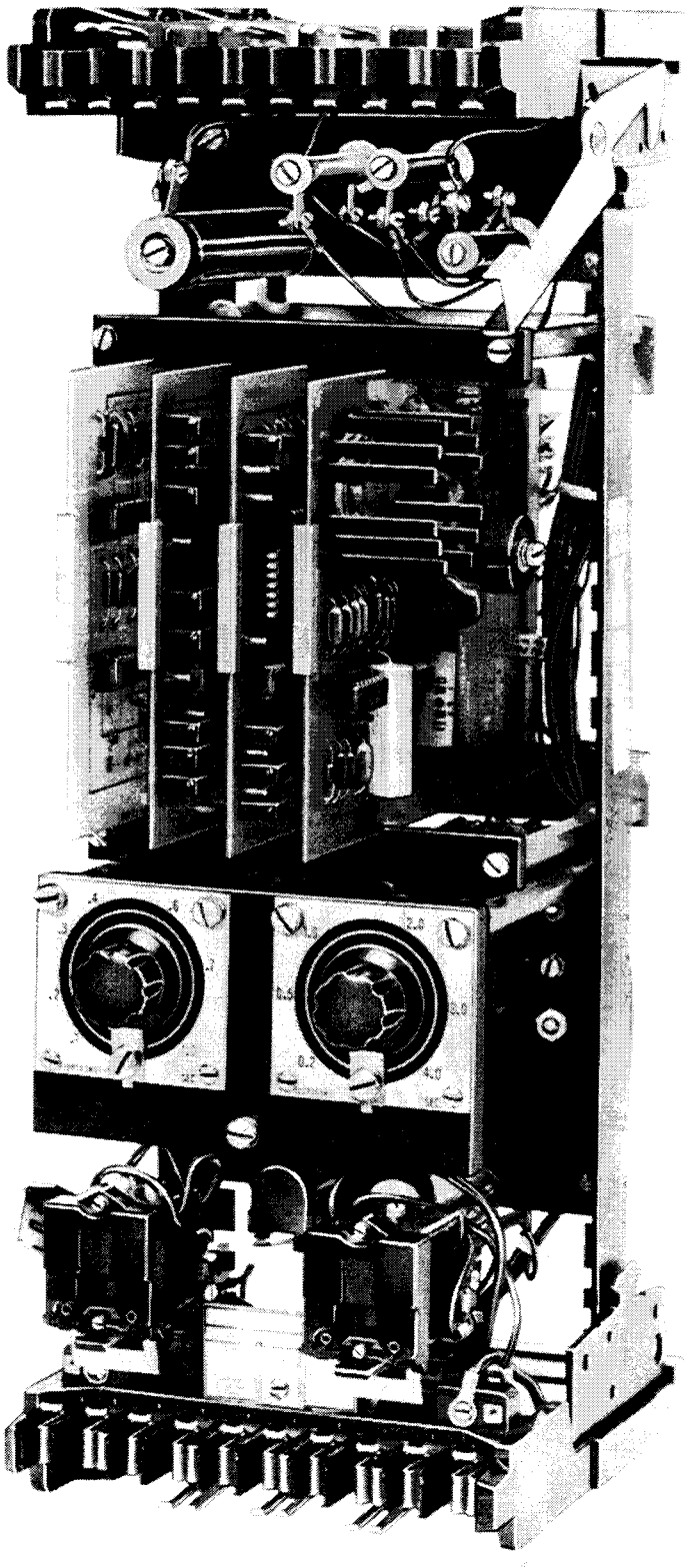


Fig. 1. Type SLB-1 Relay Chassis

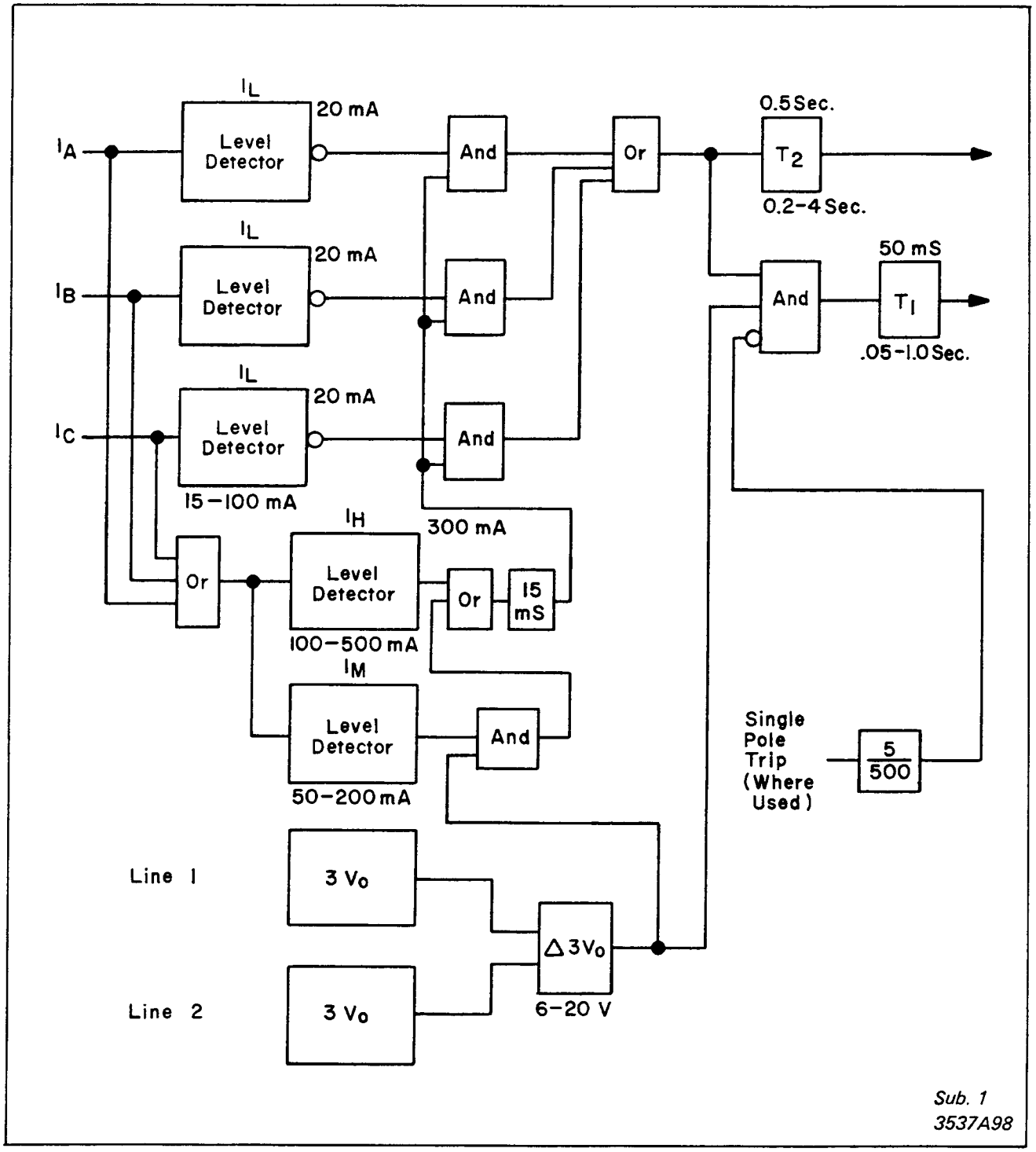
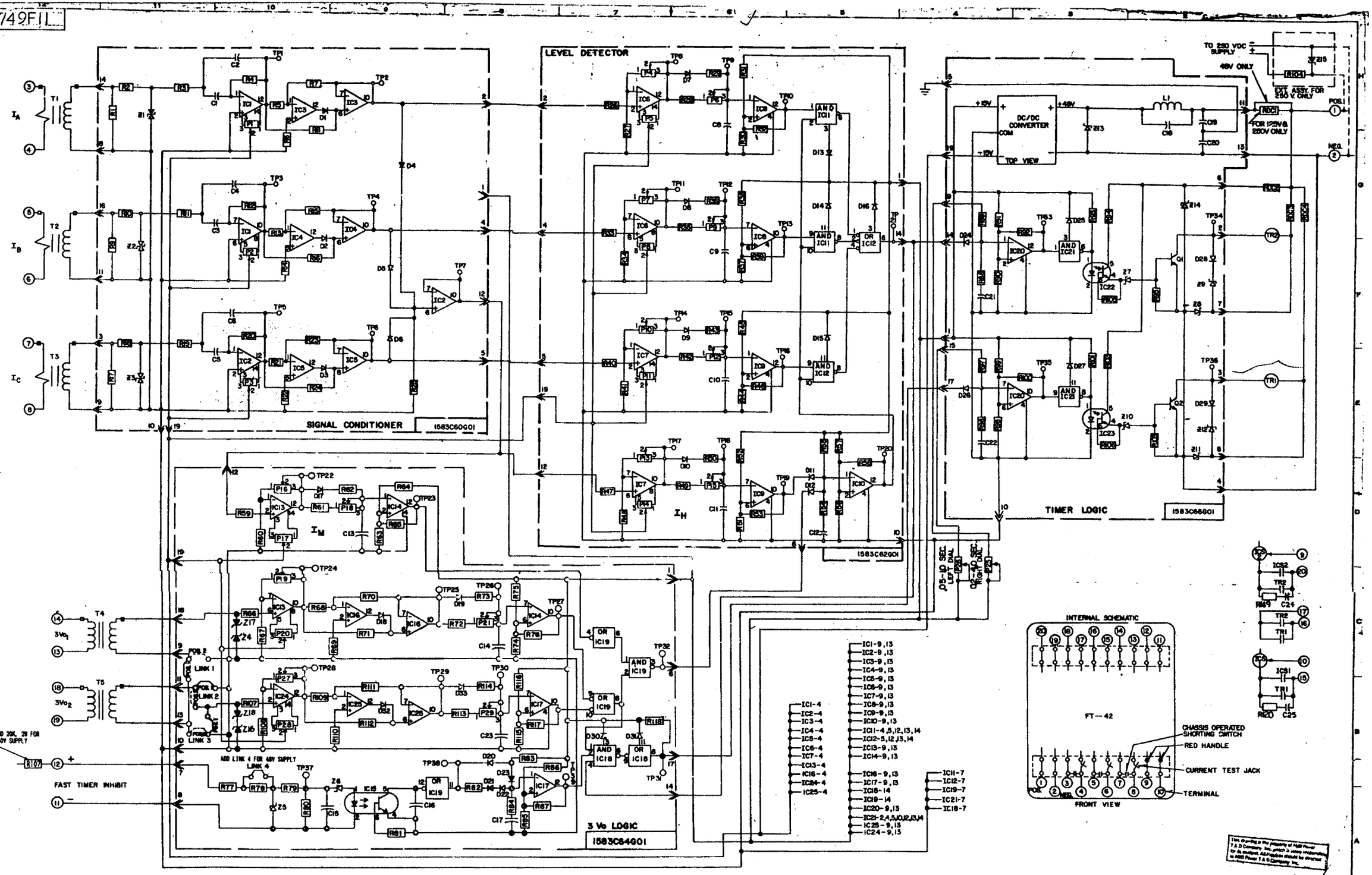


Fig. 2. Logic for SLB-1 Relay

J749F1L


LEVEL DETECTOR
SIGNAL CONDITIONER
1583C60G01
1583C62G01
TIMER LOGIC
1583C66G01
3 Vo LOGIC
1583C64G01
DC/DC CONVERTER
TOP VIEW
TO 220 VDC SUPPLY
48V ONLY
EXT. ASSY FOR 250 V ONLY
FOR 125V & 220V ONLY
POS.
NEG.
0.5-10 SEC. LEFT DIAL
0.5-10 SEC. RIGHT DIAL
FAST TIMER INHIBIT
ADD 20K, 2W FOR 250V SUPPLY
ADD LINK 4 FOR 48V SUPPLY
INTERNAL SCHEMATIC
FT-42
FRONT VIEW
CHASSIS OPERATED SHORTING SWITCH
RED HANDLE
CURRENT TEST JACK
TERMINAL

1749F11

C1	CAPACITOR	2.0 MFD 50V	3531A88H02
C2	CAPACITOR	.047 MFD 100V	353HA68H07
C3	CAPACITOR	2.0MFD 50V	3531A88H02
C4	CAPACITOR	.047 MFD 100V	353HA68H07
C5	CAPACITOR	2.0 MFD 50V	3531A88H02
C6	CAPACITOR	.047 MFD 100V	353HA68H07
C7	CAPACITOR	0.1 MFD 100V	3500A69H05
C8	CAPACITOR	0.47 MFD 200V	876A409H17
C9	CAPACITOR	0.47 MFD 200V	876A409H17
C10	CAPACITOR	0.47 MFD 200V	876A409H17
C11	CAPACITOR	0.47 MFD 200V	876A409H17
C12	CAPACITOR	1.0 MFD 35V	837A244H15
C13	CAPACITOR	0.47 MFD 200V	876A409H17
C14	CAPACITOR	0.47 MFD 200V	876A409H17
C15	CAPACITOR	0.05 MFD 100V	184A663H02
C16	CAPACITOR	500 PF 500V	837A200H02
C17	CAPACITOR	1.0 MFD 35V	837A244H15
C18	CAPACITOR	.047 MFD 200V	3502A86H03
C19	CAPACITOR	.01 MFD 3000V	3536A32H02
C20	CAPACITOR	.01 MFD 3000V	3536A32H02
C21	CAPACITOR	8.0 MFD 50V	3531A88H04
C22	CAPACITOR	4.0 MFD 50V	3531A88H03
C23	"	0.47 MFD 200V	876A409H17
C24,25	CAPACITOR	.018 MFD 100V	CE1003F1A1
D1	DIODE	IN645A	837A692H03
D2	DIODE	IN645A	837A692H03
D3	DIODE	IN645A	837A692H03
D4	DIODE	IN645A	837A692H03
D5	DIODE	IN645A	837A692H03
D6	DIODE	IN645A	837A692H03
D7	DIODE	IN645A	837A692H03
D8	DIODE	IN645A	837A692H03
D9	DIODE	IN645A	837A692H03
D10	DIODE	IN645A	837A692H03
D11	DIODE	IN645A	837A692H03
D12	DIODE	IN645A	837A692H03
D13	DIODE	IN645A	837A692H03
D14	DIODE	IN645A	837A692H03
D15	DIODE	IN645A	837A692H03
D16	DIODE	IN645A	837A692H03
D17	DIODE	IN645A	837A692H03
D18	DIODE	IN645A	837A692H03
D19	DIODE	IN645A	837A692H03
D20	DIODE	IN645A	837A692H03
D21	DIODE	IN645A	837A692H03
D22	DIODE	IN645A	837A692H03
D23	DIODE	IN645A	837A692H03
D24	DIODE	IN645A	837A692H03
D25	DIODE	IN645A	837A692H03
D26	DIODE	IN645A	837A692H03
D27	DIODE	IN645A	837A692H03
D28	DIODE	IN4818	788A342H06
D29	DIODE	IN4818	788A342H06
D30	DIODE	IN645A	837A692H03
D31	DIODE	IN645A	837A692H03
IC1	INT. CKT.	747DM	1443C52H01
IC2	INT. CKT.	747DM	1443C52H01
IC3	INT. CKT.	747DM	1443C52H01
IC4	INT. CKT.	747DM	1443C52H01
IC5	INT. CKT.	747DM	1443C52H01
IC6	INT. CKT.	747DM	1443C52H01
IC7	INT. CKT.	747DM	1443C52H01
IC8	INT. CKT.	747DM	1443C52H01
D32	DIODE	IN645A	837A692H03
D33	"	"	"

IC24	INT. CKT.	747DM	1443C52H01
IC25	INT. CKT.	747DM	1443C52H01
IC9	INT. CKT.	747DM	1443C52H01
IC10	INT. CKT.	747DM	1443C52H01
IC11	INT. CKT.	MC679L	6296D58H02
IC12	INT. CKT.	MC679L	6296D58H02
IC13	INT. CKT.	747DM	1443C52H01
IC14	INT. CKT.	747DM	1443C52H01
IC15	INT. CKT.	4N35	7748936H01
IC16	INT. CKT.	747DM	1443C52H01
IC17	INT. CKT.	747DM	1443C52H01
IC18	INT. CKT.	MC679L	6296D58H02
IC19	INT. CKT.	MC868L	6296D58H05
IC20	INT. CKT.	747DM	1443C52H01
IC21	INT. CKT.	MC679L	6296D58H02
IC22	INT. CKT.	4N35	7748936H01
IC23	INT. CKT.	4N35	7748936H01
Q1	TRANSISTOR	2N3590	837A617H03
Q2	TRANSISTOR	2N3590	837A617H03
T1	TRANSFORMER		1582C88902
T2	TRANSFORMER		1582C88902
T3	TRANSFORMER		1582C88902
T4	TRANSFORMER		1582C88901
T5	TRANSFORMER		1582C88901
R1	RESISTOR	100Ω, 3W, 5%	763AI27H20
R2	RESISTOR	1.0K, 3W, 5%	763AI27H02
R3	RESISTOR	1.3K, .5W, 1%	848A819H59
R4	RESISTOR	53.6K, .5W, 1%	848A821H16
R5	RESISTOR	20K, .5W, 1%	848A820H74
R6	RESISTOR	10K, .5W, 1%	848A820H45
R7	RESISTOR	20K, .5W, 1%	848A820H74
R8	RESISTOR	10K, .5W, 1%	848A820H45
R9	RESISTOR	100Ω, 3W, 5%	763AI27H20
R10	RESISTOR	1.0K, 3W, 5%	763AI27H02
R11	RESISTOR	1.3K, .5W, 1%	848A819H59
R12	RESISTOR	53.6K, .5W, 1%	848A821H16
R13	RESISTOR	20K, .5W, 1%	848A820H74
R14	RESISTOR	10K, .5W, 1%	848A820H45
R15	RESISTOR	20K, .5W, 1%	848A820H74
R16	RESISTOR	10K, .5W, 1%	848A820H45
R17	RESISTOR	100Ω, 3W, 5%	763AI27H20
R18	RESISTOR	1.0K, 3W, 5%	763AI27H02
R19	RESISTOR	1.3K, .5W, 1%	848A819H59
R20	RESISTOR	53.6K, .5W, 1%	848A821H16
R21	RESISTOR	20K, .5W, 1%	848A820H74
R22	RESISTOR	10K, .5W, 1%	848A820H45
R23	RESISTOR	20K, .5W, 1%	848A820H74
R24	RESISTOR	10K, .5W, 1%	848A820H45
R25	RESISTOR	10K, .5W, 1%	848A820H45
R26	RESISTOR	619Ω, .5W, 1%	848A819H28
R27	RESISTOR	619Ω, .5W, 1%	848A819H28
R28	RESISTOR	3.01K, .5W, 1%	848A819H94
R29	RESISTOR	1.0 K, .5W, 1%	848A819H48
R30	RESISTOR	10K, .5W, 1%	848A820H45
R31	RESISTOR	10K, .5W, 1%	848A820H45
R32	RESISTOR	10K, .5W, 1%	848A820H45
R33	RESISTOR	619Ω, .5W, 1%	848A819H28
R34	RESISTOR	619Ω, .5W, 1%	848A819H28
R35	RESISTOR	3.01K, .5W, 1%	848A819H94
R36	RESISTOR	1.0 K, .5W, 1%	848A819H48
R37	RESISTOR	10K, .5W, 1%	848A820H45
R38	RESISTOR	10K, .5W, 1%	848A820H45
R107		10K, .5W, 1%	848A819H48
R108		" " "	"
R109		20K, .5W, 1%	848A820H74
R110		10K, .5W, 1%	848A820H45
R111		20K, .5W, 1%	848A820H74
R118		15K, .5W, 1%	848A820H62

R39	RESISTOR	10K, .5W, 1%	848A820H45
R40	RESISTOR	619Ω, .5W, 1%	848A819H28
R41	RESISTOR	619Ω, .5W, 1%	848A819H28
R42	RESISTOR	3.01K, .5W, 1%	848A819H94
R43	RESISTOR	1.0 K, .5W, 1%	848A819H48
R44	RESISTOR	10K, .5W, 1%	848A820H45
R45	RESISTOR	10K, .5W, 1%	848A820H45
R46	RESISTOR	10K, .5W, 1%	848A820H45
R47	RESISTOR	619Ω, .5W, 1%	848A819H28
R48	RESISTOR	619Ω, .5W, 1%	848A819H28
R49	RESISTOR	3.01K, .5W, 1%	848A819H94
R50	RESISTOR	1.0 K, .5W, 1%	848A819H48
R51	RESISTOR	10K, .5W, 1%	848A820H45
R52	RESISTOR	10K, .5W, 1%	848A820H45
R53	RESISTOR	10K, .5W, 1%	848A820H45
R54	RESISTOR	100Ω, .5W, 1%	848A818H51
R55	RESISTOR	15.0K, .5W, 1%	848A820H62
R56	RESISTOR	10K, .5W, 1%	848A820H45
R57	RESISTOR	10K, .5W, 1%	848A820H45
R58	RESISTOR	10K, .5W, 1%	848A820H45
R59	RESISTOR	1.0 K, .5W, 1%	848A819H48
R60	RESISTOR	453Ω, .5W, 1%	848A819H15
R61	RESISTOR	3.01K, .5W, 1%	848A819H94
R62	RESISTOR	1.0 K, .5W, 1%	848A819H48
R63	RESISTOR	10K, .5W, 1%	848A820H45
R64	RESISTOR	10K, .5W, 1%	848A820H45
R65	RESISTOR	10K, .5W, 1%	848A820H45
R66	RESISTOR	1.0 K, .5W, 1%	848A819H48
R67	RESISTOR	1.0 K, .5W, 1%	848A819H48
R68	RESISTOR	20K, .5W, 1%	848A820H74
R69	RESISTOR	10K, .5W, 1%	848A820H45
R70	RESISTOR	20K, .5W, 1%	848A820H74
R71	RESISTOR	10K, .5W, 1%	848A820H45
R72	RESISTOR	3.01K, .5W, 1%	848A819H94
R73	RESISTOR	1.0 K, .5W, 1%	848A819H48
R74	RESISTOR	10K, .5W, 1%	848A820H45
R75	RESISTOR	10K, .5W, 1%	848A820H45
R76	RESISTOR	10K, .5W, 1%	848A820H45
R77	RESISTOR	5K, 3W, .5%	763AI27H04
R78	RESISTOR	15K, 2W, .5%	185A207H55
R79	RESISTOR	470Ω, .5W, 2%	629A531H24
R80	RESISTOR	8.2K, .5W, 2%	629A531H54
R81	RESISTOR	1.0M, .5W, 1%	848A822H39
R82	RESISTOR	499K, .5W, 1%	848A822H10
R83	RESISTOR	4.99K, .5W, 1%	848A820H16
R84	RESISTOR	100Ω, .5W, 1%	848A818H51
R85	RESISTOR	15K, .5W, 1%	848A820H62
R86	RESISTOR	15K, .5W, 1%	848A820H62
R87	RESISTOR	22.1K, .5W, 1%	848A820H78
R88	RESISTOR	100Ω, .5W, 1%	848A818H51
R89	RESISTOR	20K, .5W, 1%	848A820H74
R90	RESISTOR	10K, .5W, 1%	848A820H45
R91	RESISTOR	10K, .5W, 1%	848A820H45
R92	RESISTOR	10K, .5W, 1%	848A820H45
R93	RESISTOR	68Ω, .5W, 1%	848A819H32
R94	RESISTOR	10K, .5W, 1%	848A820H45
R95	RESISTOR	10K, .5W, 1%	848A820H45
R96	RESISTOR	100Ω, .5W, 1%	848A818H51
R97	RESISTOR	2.49K, .5W, 1%	848A819H86
R98	RESISTOR	10K, .5W, 1%	848A820H45
R99	RESISTOR	10K, .5W, 1%	848A820H45
R112		" " "	"
R113		3.01K, .5W, 1%	848A819H94
R114		1.0K, .5W, 1%	848A819H48
R115		10.K, .5W, 1%	848A820H45
R116		" " "	"
R117		" " "	"

R100	RESISTOR	10K, .5W, 1%	848A820H45
R101	RESISTOR	68Ω, .5W, 1%	848A819H32
R102	RESISTOR	4.99K, .5W, 1%	848A820H16
R103	RESISTOR	4.99K, .5W, 1%	848A820H16
R104	RESISTOR	2×400Ω, .40W	RW4000JJ06
R105	RESISTOR	1.0M, .25W, 1%	848A822H39
R106	RESISTOR	1.0M, .25W, 1%	848A822H39
■R107	RESISTOR	20K, 2W, 5% CARBON	RC2002J279
P1	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P2	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P3	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P4	TRIM POTENTIOMETER	20K, .5W	3531A86H02
P5	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P6	TRIM POTENTIOMETER	10K, .5W	3531A86H01
P7	TRIM POTENTIOMETER	20K, .5W	3531A86H02
P8	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P9	TRIM POTENTIOMETER	10K, .5W	3531A86H01
P10	TRIM POTENTIOMETER	20K, .5W	3531A86H02
P11	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P12	TRIM POTENTIOMETER	10K, .5W	3531A86H01
P13	TRIM POTENTIOMETER	10K, .5W	3531A86H01
P14	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P15	TRIM POTENTIOMETER	10K, .5W	3531A86H01
P16	TRIM POTENTIOMETER	10K, .5W	3531A86H01
P17	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P18	TRIM POTENTIOMETER	20K, .5W	3531A86H02
P19	TRIM POTENTIOMETER	20K, .5W	3531A86H02
P20	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P21	TRIM POTENTIOMETER	10K, .5W	3531A86H01
P22	TRIM POTENTIOMETER	20K, .5W	3531A86H02
P23	TRIM POTENTIOMETER	10K, .5W	3523A42H01
P24	TRIM POTENTIOMETER	10K, .5W	3531A86H01
P25	POTENTIOMETER	500K, 2W	3531A87H02
P26	POTENTIOMETER	250K, 2W	3531A87H01
P27	TRIM POT.	20K, .5W	3531A86H02
P28	TRIM POT.	10K, .5W	3523A42H01
P29	TRIM POT	10K, .5W	3531A86H01
Z1	ZENER DIODE	IN4836, 15V	3531A92H01
Z2	ZENER DIODE	IN4836, 15V	3531A92H01
Z3	ZENER DIODE	IN4836, 15V	3531A92H01
Z4	ZENER DIODE	IN960B	186A797H10
Z5	ZENER DIODE	IN3686B, 20V	185A212H06
Z6	ZENER DIODE	IN752A, 5.6V	186A797H12
Z7	ZENER DIODE	IN748A, 3.6V	837A398H08
Z8	ZENER DIODE	IN3049B, 160V	187A936H13
Z9	ZENER DIODE	IN3049B, 160V	187A936H13
Z10	ZENER DIODE	IN748A, 3.6V	837A398H08
Z11	ZENER DIODE	IN3049B, 160V	187A936H13
Z12	ZENER DIODE	IN3049B, 160V	187A936H13
Z13	ZENER DIODE	IN2832B, 56V	184A854H84
Z14	ZENER DIODE	IN5352B, 15V	862A288H04
Z15	ZENER DIODE	IN3344RA, 130V	762A631H16
Z16	ZENER DIODE	IN960B	186A797H10
Z17	ZENER DIODE	IN960B	186A797H10
Z18	ZENER DIODE	IN960B	186A797H10
● RDC1	RESISTOR	560Ω, 40W	1336I73
✱ RDC2	RESISTOR	3.3K, 10 W	184A856H06
● RDC2	RESISTOR	8.0K, 10 W	3502A39H02
✱ RDC3	RESISTOR	600Ω, 10W	3502A39H01
● RDC3	RESISTOR	2 K, 10 W	184A856H08
✱ RDC4	RESISTOR	600Ω, 10 W	3502A39H01
● RDC4	RESISTOR	2K, 10W	184A856H06
R107(●)	RESISTOR	1.0MEG, .25W, 1%	RN1044F1M0
TR1	TELEPHONE RELAY		541D514H37
TR2	TELEPHONE RELAY		541D514H37
L1	CHOKE		2928096G04
R19	RESISTOR 1.0M 25W 1%		RN1004F1M0
R120	RESISTOR 1.0M 25W 1%		RN1004F1M0

● FOR 125V & 250V ONLY
✱ FOR 48V ONLY

■ FOR 250V ONLY

NOTE:

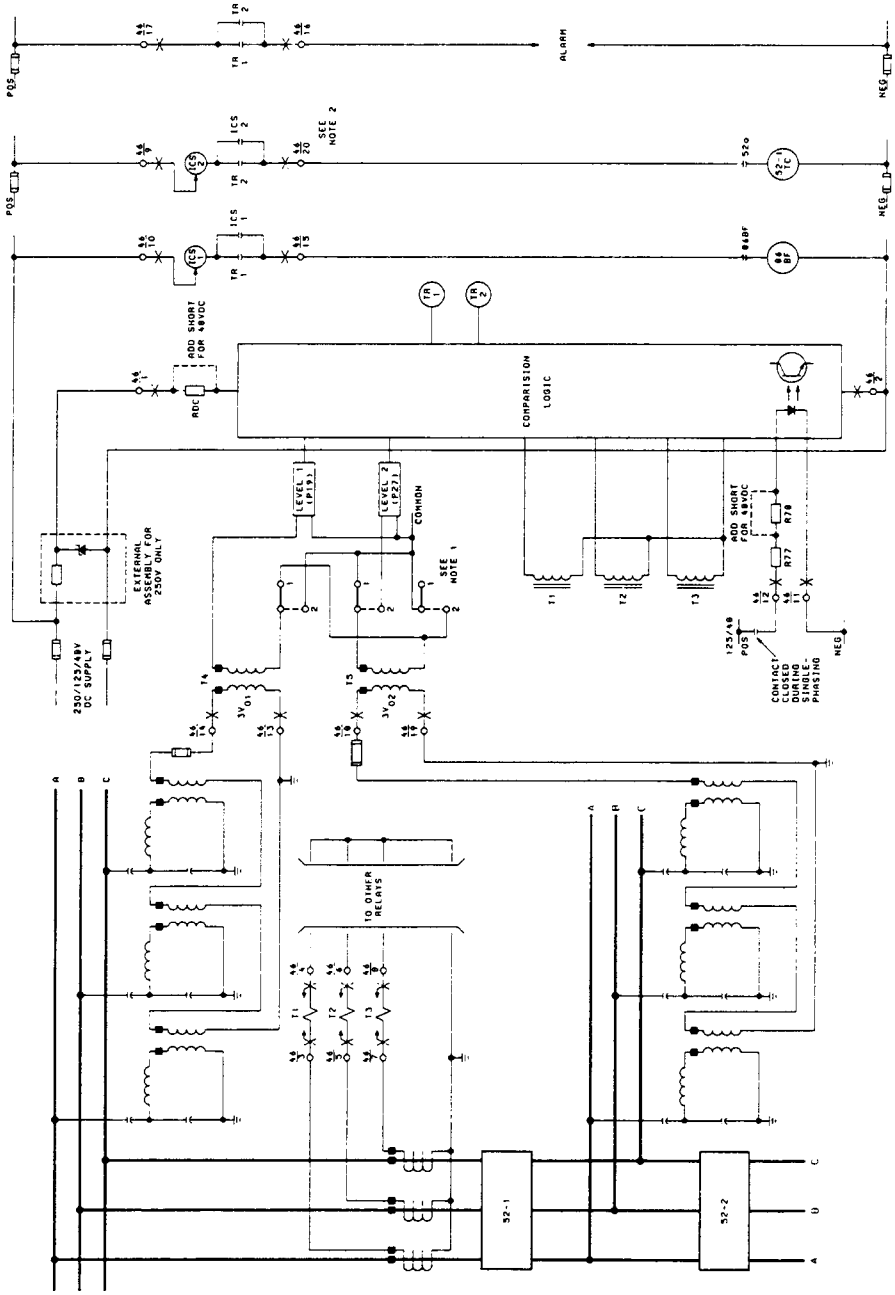
1. USE LINK POSITION 1 FOR $\Delta 3\ V_0$ SENSING.

   USE LINK POSITION 2 FOR INDEPENDENT V_{01} AND V_{02} SENSING.

2. CONNECTIONS SHOWN FOR TR-2 ASSUME LINK POSITION 1 IN USE AND RETRIP OF PROTECTED BREAKER IS DESIRED WHEN $\Delta 3\ V_0$ IS LOW. FOR LINK POSITION 2, 86BF TRIPPING BY TR-2 MAY BE DESIRED.

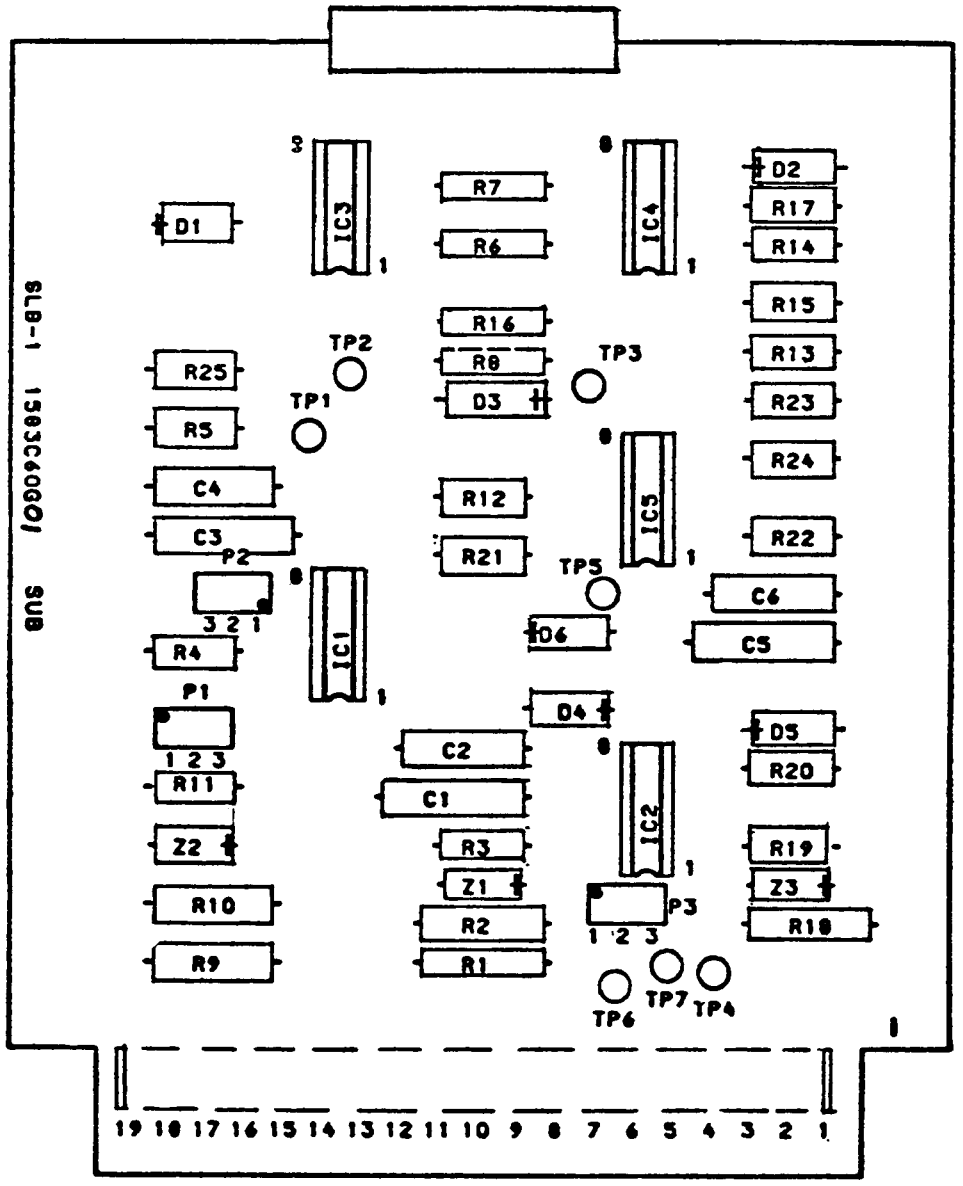
DEVICE NUMBER CHART

46 – SLB-1 POLE DISAGREEMENT RELAY
52 – CIRCUIT BREAKER
86BF – BREAKER FAILURE LOCKOUT RELAY



Sub. 2
Dwg. 2052D90

Fig. 4. External Connection Diagram



Sub. 2
Dwg. 1486B43

Fig. 5. Component Location (Signal Conditioner)

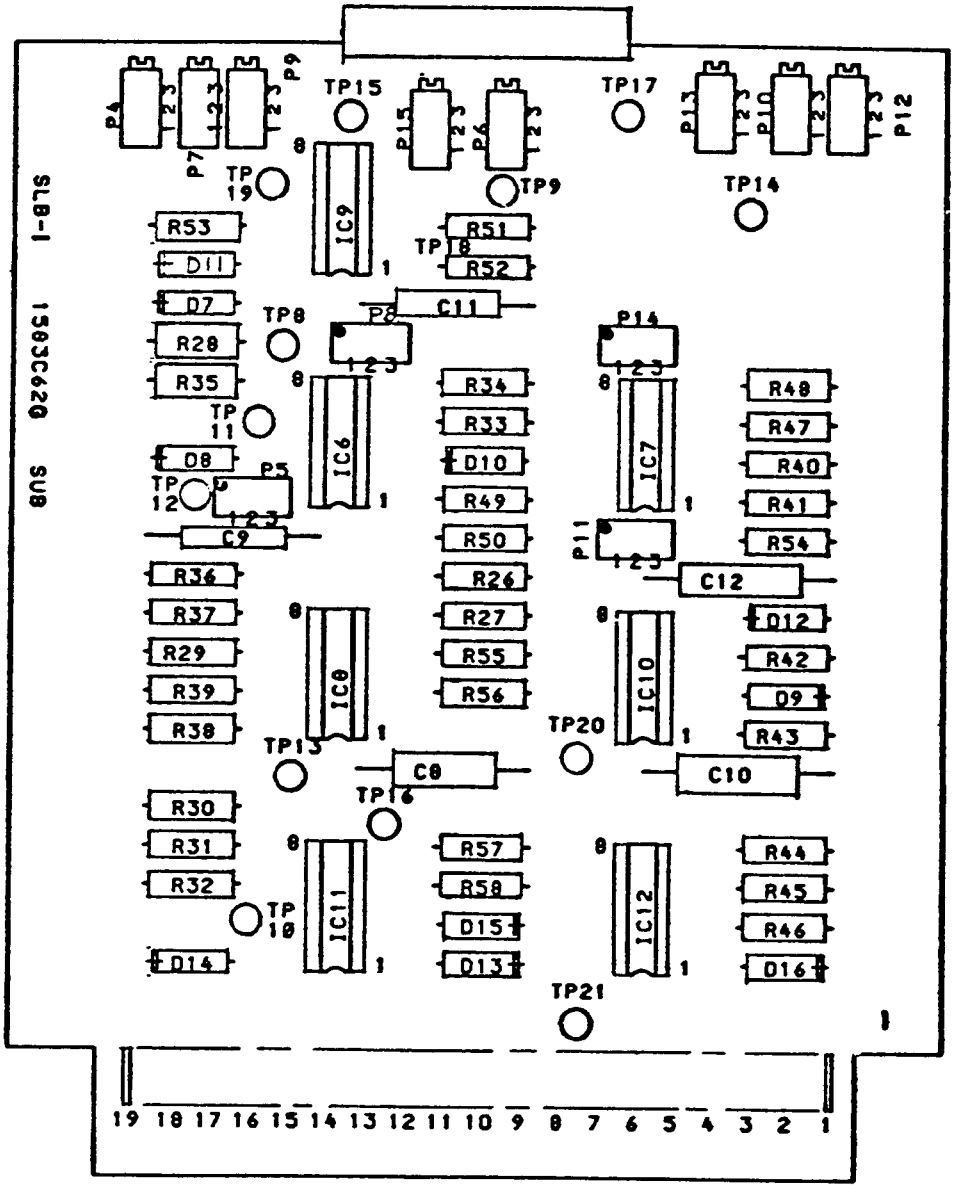


Fig. 6. Component Location (Level Detector)

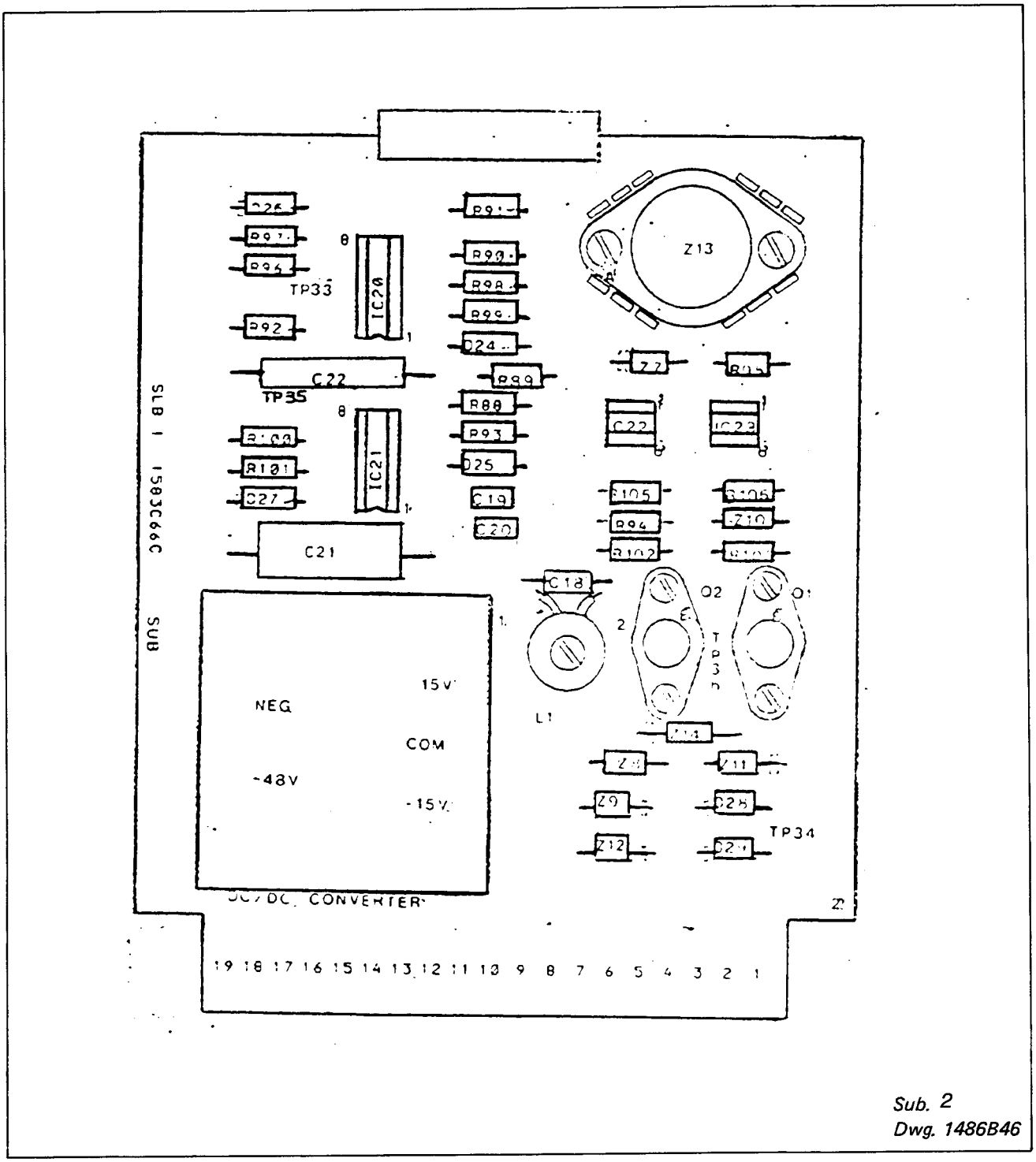
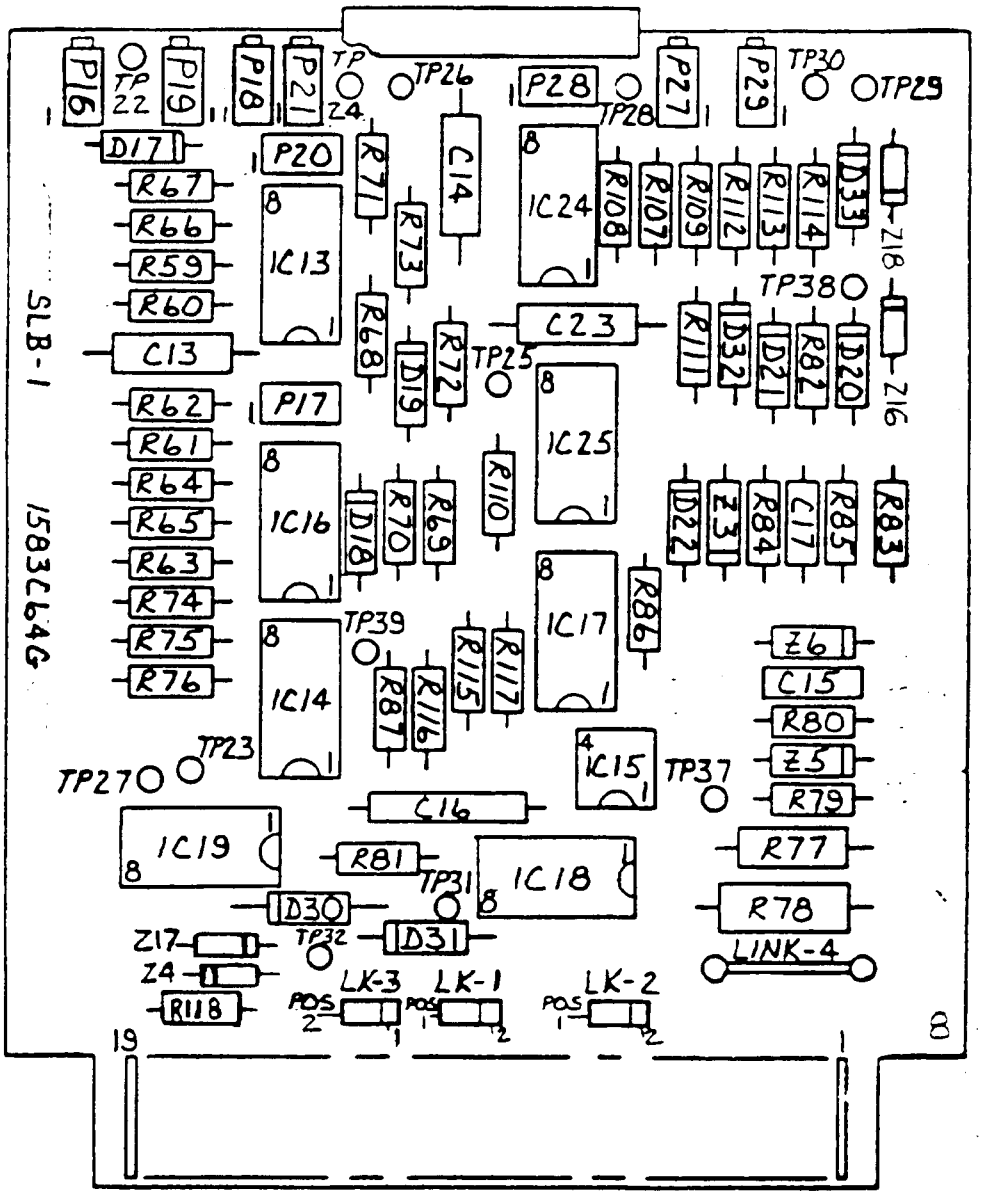


Fig. 7. Component Location (Timer)



Sub. 7
Dwg. 1486B45

Fig. 8. Component Location (3 V_0 Logic)

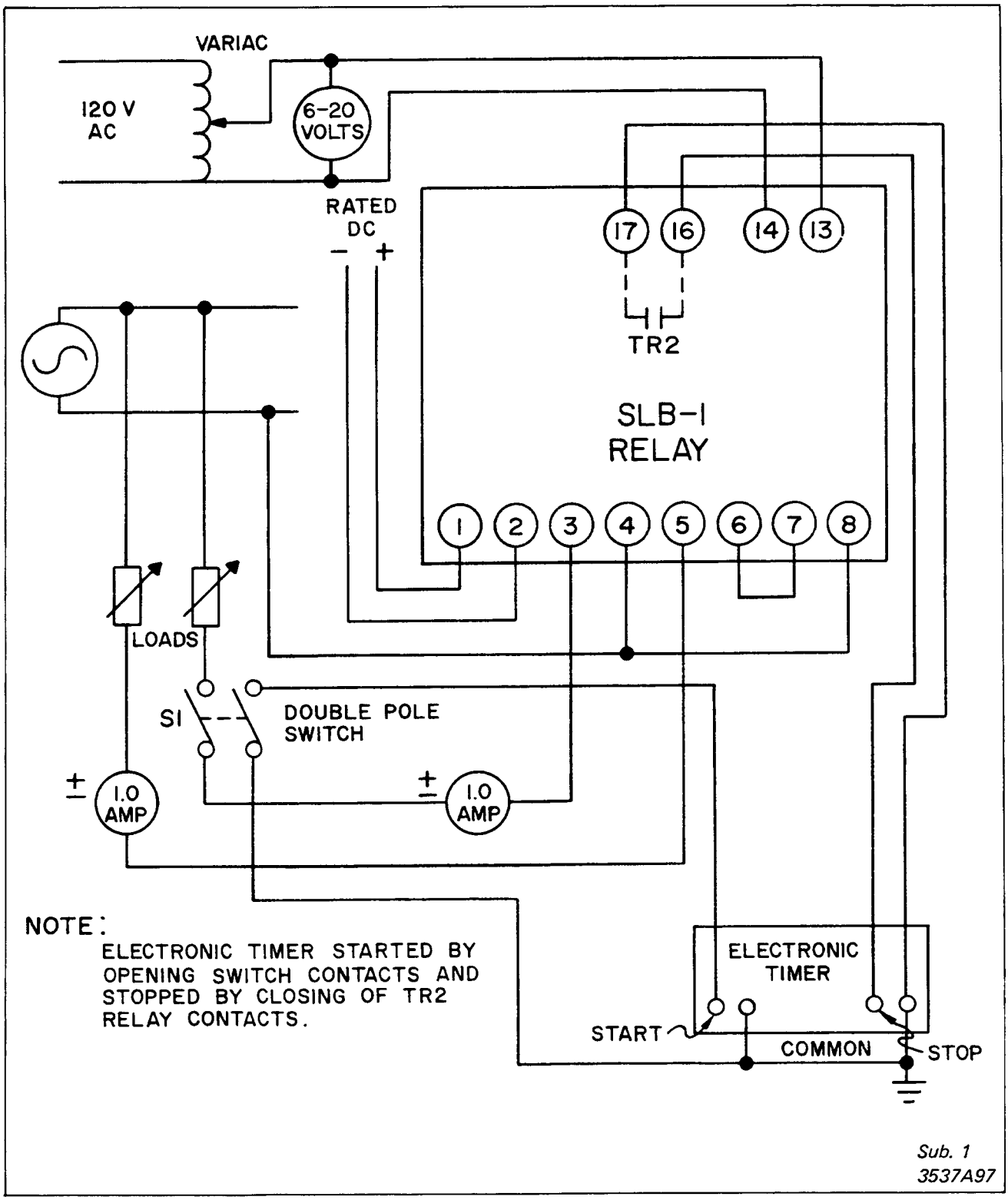


Fig. 9. Timer Test Circuit

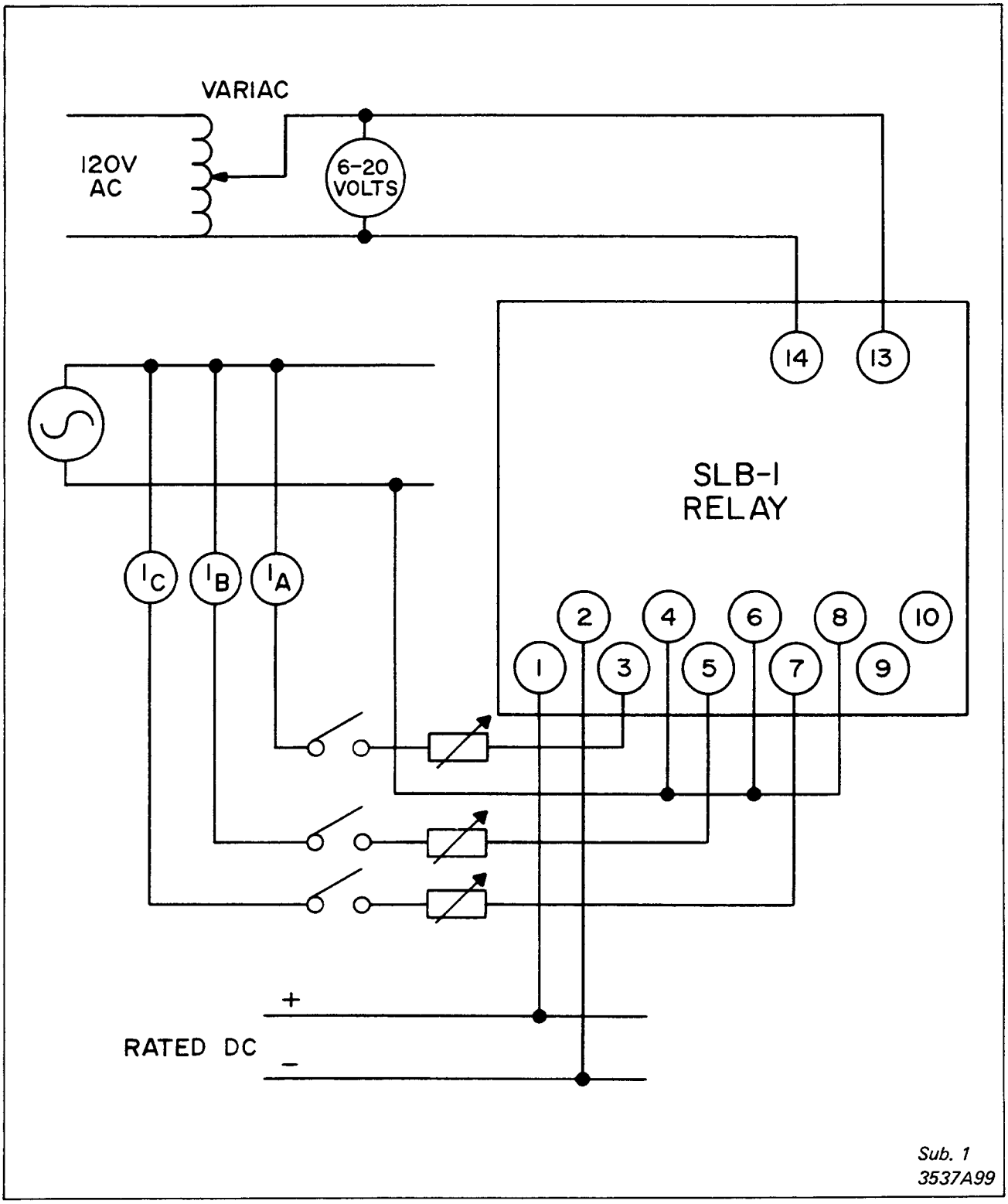


Fig. 10. SLB-1 Relay Test Circuit

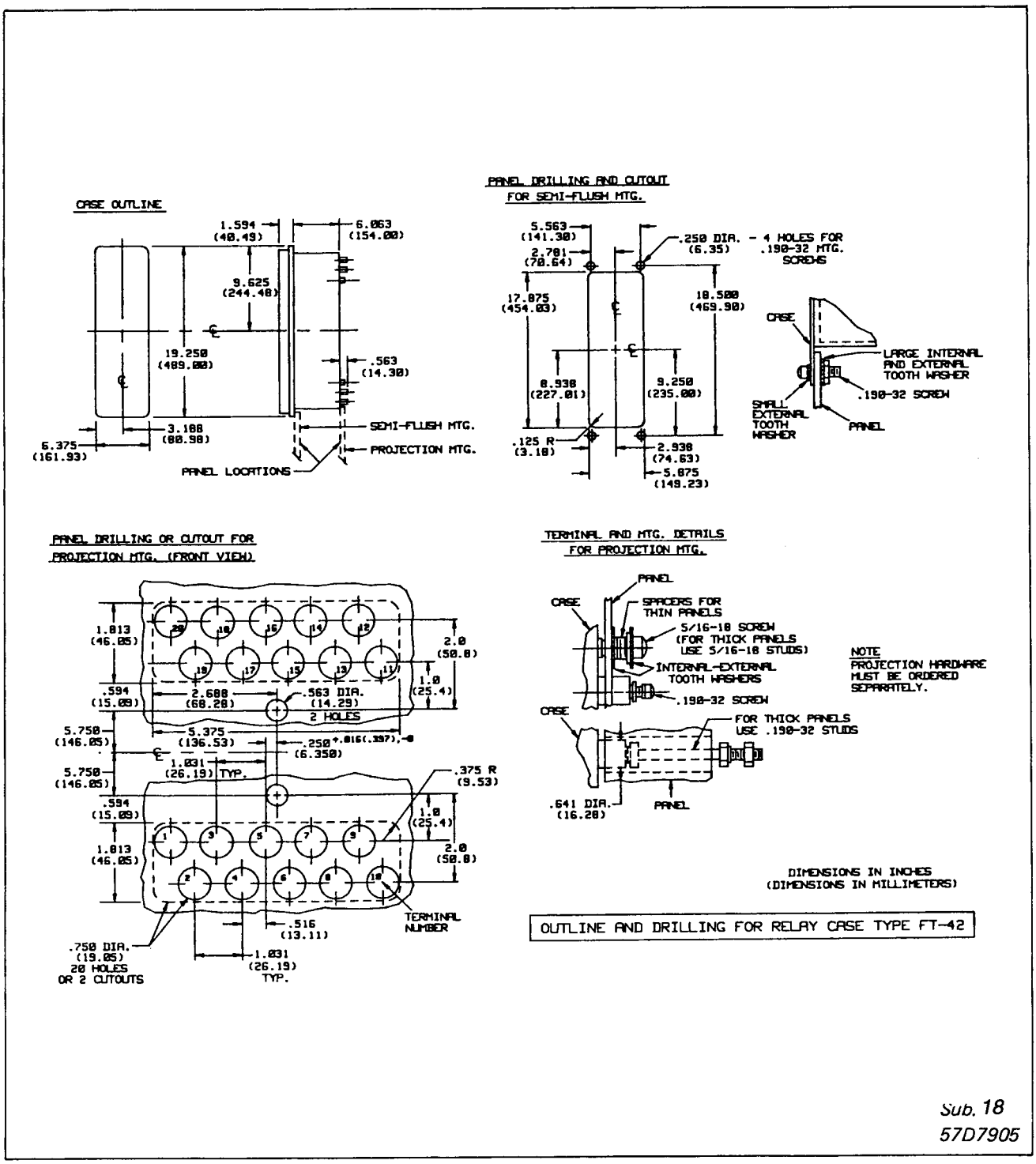


Fig. 11. Outline and Drilling Plan for Type SLB-1 Relay in Type FT-42 Case

ABB Power T&D Company Inc.
Relay Division
Coral Springs, FL 33065

Addendum to
I.L. 41-775.2A

Type SLB-1
Breaker Pole Failure Relay
10 Amp Continuous Rating

Effective: November 1991
This Addendum Supersedes
All Previous Addenda

A - Add New Information • **C** - Change Existing Information • **D** - Delete Information

C

Page 3

Under "OPERATION", paragraph 1. The last sentence beginning "The rectifier circuit is basically a voltage follower IC3....." should be changed to read as follows:

"The rectifier circuit is basicaly a voltage follower IC3 (pins 6, 7, 10) and an inverting amplifier IC3 (12) where the input to the (+) terminal (pin 6) of the voltage follower is positive regardless of the polarity of the signal at TP1".

C

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Under "CALIBRATION", paragraph 2. "..... style S#644B315 G03." should read as follows: ".....style S#644B315 G02."

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