INSTALLATION • OPERATION • MAINTENANCE

INSTRUCTIONS

TYPE SDF-1 SOLID STATE UNDERFREQUENCY RELAY FOR CLASS 1E APPLICATIONS

CAUTION

It is recommended that the user of this equipment become acquainted with the information in this instruction leaflet before energizing the equipment. Failure to observe this precaution may result in damage to the equipment.

Printed circuit modules should not be removed or inserted while the relay is energized unless specific instructions elsewhere in this instruction leaflet state that such action is permissible. Failure to observe this precaution can result in an undesired tripping output, and cause component damage.

APPLICATION

The SDF-1 Relay (Figures 1 and 2) is a solid state, single-frequency setting, high-accuracy under-frequency relay for use in automatic load-saving schemes. (See setting section page 5 for further application data.)

"Class 1E" is the safety classification of the electric equipment and systems in nuclear power generating stations that are essential to emergency shutdown of the reactor, containment isolation, cooling of the reactor, and heat removal from the containment and reactor, or otherwise are essential in preventing significant release of radioactive material to the environment.

These relays have been specially designed and tested to establish their suitability for Class 1E applications. Materials have been selected and tested to insure that the relays will perform their intended function for their design life when operated in a normal environment as defined by ANSI standard C37.90-1978, when exposed to radiation levels up to 10^4 rads, and when subjected to seismic events producing a Shock Response Spectrum within the limits of the relay rating.

CONSTRUCTION & OPERATION

The type SDF-1 Underfrequency Relay is composed of (1) an isolation transformer, (2) a zero crossing voltage detector, and synchronizer printed circuit module, (3) a main clock and four bit binary counter printed circuit module, (4) a twelve bit binary counter printed circuit module, (5) a trip control circuit and delay timer printed circuit module, (6) a power supply printed circuit module, (7) a front panel mounted digital underfrequency trip-point setting assembly, (8) an indicating contactor switch unit (ICS), and (9) an input/output trip relay module.

All components are identified on the internal schematic in Figure 3.

ISOLATING TRANSFORMER

The isolation transformer is a 1:1 transformer which provides dc isolation.

ZERO CROSSING, VOLTAGE DETECTOR, AND SYNCHRONIZER PRINTED CIRCUIT MODULE

The zero crossing, voltage detector, and synchronizer printed circuit module contains a two-

All possible contingencies which may arise during installation, operation, or maintenance, and all details and variations of this equipment do not purport to be covered by these instructions. If further information is desired by purchaser regarding his particular installation, operation or maintenance of his equipment, the local Westinghouse Electric Corporation representative should be contacted.

cell symmetrical low pass filter to provide transient and high frequency noise suppression, a zero crossing detector that generates a low voltage square wave signal having the same frequency as the fundamental of the input signal, and a synchronizer for the synchronization of the output signals from the zero-crossing detector with the main clock signals. Also contained on this module are the two power supply voltage detectors to prevent spurious tripping at the time of power turn-on, and an undervoltage detector which provides an inhibiting signal to avoid incorrect operation of the relay if the input line voltage drops below the minimum prescribed value (25 to 45 volts). Refer to Figure 5 for component location and board layout.

MAIN CLOCK AND FOUR BIT BINARY COUNTER PRINTED CIRCUIT MODULE

The main clock and four bit binary counter printed circuit module contains the main clock and the first four bits of the binary counter. The main clock, consisting of a crystal controlled oscillator to provide the reference frequency and a driving state, supplies clock pulses to the main counter and to the synchronizer. The first four bits of the 16-bit binary counter are also contained on this module. Refer to Figure 6 for component location and board layout.

TWELVE BUT BINARY COUNTER PRINTED CIRCUIT MODULE

The twelve bit binary counter printed circuit module contains the last 12 bits of the 16 bit binary counter and the timing control circuit. The timing control circuit accomplishes the generation of the proper signals required by the trip control circuit to perform the specified trip enabling or inhibiting sequences as well as generation of the reset signal for the binary counter. Refer to Figure 7 for component location and board layout.

TRIP CONTROL CIRCUIT AND DELAY TIMER PRINTED CIRCUIT MODULE

The trip control circuit and delay timer printed circuit module contains the coincidence output circuit, a trip control, a trip timer, and a trip output circuit. The coincidence output circuit generates a signal that is stored by the trip control circuit when the period set on the underfrequency trippoint setting is exceeded. The trip control circuit stores the information whether or not a trip condition occurred during the actual cycle and before the reset signal initiates the next period timing. This circuit also steps up on one of the required counting sequences of three consecutive trip cycles for tripping or two consecutive no-trip cycles required for reset. The trip timer starts after the first trip cycle is recognized. Before three consecutive trip cycles have occurred it is reset by the first no-trip cycle; after three consecutive trip cycles have occurred it is reset only if two consecutive no-trip cycles occur. The timer energizes the trip output circuit after the delay time is expired. The delay time, after the first trip cycle is recognized, can be set from 1 to 99 cycles (60 Hz base) with the front panel decade switches; the prescribed range however goes from a minimum of 2 cycles, since three consecutive trip cycles are required by the trip control circuit for a trip condition, to a maximum of 99 cycles. The trip output circuit provides the required signal characteristics in order to drive the trip relay. The trip output circuit is set in the trip condition by the completion of the trip delay time and is reset by either a low voltage inhibit signal or the trip control circuitry. Refer to Figure 8 for component location and board layout.

POWER SUPPLY PRINTED CIRCUIT MODULE

The power supply printed circuit module contains a dual voltage regulated switching power supply with an 18 volt dc output for most relay functions and a 5 volt dc output for the integrated circuit functions. The main supply is of the switching regulator design giving high efficiency and relative insensitivity to input voltage. Refer to Figure 9 for component location and board layout.

DIGITAL UNDERFREQUENCY TRIP-POINT SETTING ASSEMBLY

The digital underfrequency trip-point setting assembly is where the frequency trip-point is set as maximum allowed period. The setting corresponds to the binary coded number of main clock pulses that can be counted during the maximum period

duration. If the actual period exceeds the set value, the coincidence generates a signal to the trip control circuit.

The two trip delay timer decade setting switches are located on the underfrequency trip-point setting assembly and can be set in any combination yielding from 2 to 99 cycles of time delay (60 Hz base).

INPUT/OUTPUT TRIP RELAY MODULE

The operation of the trip relay is controlled by the trip output circuit on the trip control circuit and delay timer printed circuit module. The trip relay, when energized, allows the indicating contractor switch unit to operate. A capacitive protection scheme is used to make the SDF-1 less susceptible to transients and noise.

Indicating Contactor Switch Unit (ICS)

The indicating contactor switch is a small dc operated clapper type device. A magnetic armature, to which leaf-spring mounted contacts are attached, is attracted to the magnetic core upon energization of the switch. When the switch closes, the moving contacts bridge two stationary contacts, completing the trip circuit. Also during this operation two fingers on the armature deflect a spring located on the front of the switch which allows the operation indicator target to drop. The target is reset from the outside of the case by a push rod located at the bottom of the cover.

UNDERFREQUENCY TEST MODULE 1469C14G01 (Optional)

The underfrequency test module consists of a printed circuit module with an 11 bit binary keyboard mounted on the front module panel. The complete circuit diagram is shown in Figure 11. To obtain a desired test frequency, the corresponding binary code (Table I) is set on the keyboard. Diodes D1 through D11 operate as a coincidence detector for the main counter bits connected to the closed switches on the test module. Refer to Figure 12 for component location and board layout.

THEORY OF OPERATION

Operation of the SDF-1 underfrequency relay will be described with the aid of Figure 3 internal schematic drawing 1725F14, and Figure 4 external schematic and logic diagram drawing 719B252.

The SDF-1 underfrequency relay utilizes the period of the alternating waveform being monitored for underfrequency measurement. The input signal is isolated, filtered to remove transients and high frequency noise, checked for undervoltage, and fed into the zero-crossing detector, where positive-going zero-crossing signals are generated to define the period of the waveform. The positive-going zero-crossing signals are brought into synchronization with the main clock signal of 1.966080 megahertz and are used to reset the binary counter at each synchronized positive-going zero-crossing.

The main clock increments the binary counter at a 1.966080 megahertz rate so that bit [15] of the counter changes to a logic "1" signal in 16.6667 milliseconds, the period of a 60 hertz waveform. The underfrequency trip point setting corresponds to the binary coded number of main clock pulses that can be counted after bit [15] goes to "1", or period in excess of the 16.6667 millisecond (60 hertz period). The binary settings for frequencies from 60.00 to 54.00 Hz in .05 Hz steps are given in Table 1.

If the actual period exceeds this set value (underfrequency condition), the coincidence circuit generates a signal to the trip control circuity where it is stored. The trip control circuit stores the information whether or not a trip condition occurred during the actual cycle and before the reset signal which initiates the next period timing. The trip timer starts *after* the first trip cycle is recognized. Before the required counting sequence of three consecutive trip cycles for a trip condition is completed, the trip control circuit can be reset by the first no-trip cycle; after three consecutive trip cycles have occurred it is reset only if two consecutive non-trip cycles occur. The timer energizes

the trip output circuitry to energize the trip relay after the delay time set is expired. The delay time can be set from the minimum 2 cycles to 99 cycles (60 Hz base). The trip output circuit to the trip relay is reset by either a low voltage inhibit signal or the trip control circuitry.

A more detailed look at the underfrequency measurement circuitry of the SDF-1 relay is as follows (refer to Figures 1 and 3):

The period of the alternating waveform is measured by circuitry on the zero crossing, voltage detectors, and synchronizer printed circuit module. The voltage being monitored is supplied through 1:1 isolation transformer to the low pass filter which removes transient and high frequency noise from the ac signal. It is then clipped by diodes D5 and D6 to limit the differential range to a nominal $\pm$ .7 volts being fed into the input stage of the zero-crossing detector. Positive going zero-crossings are detected by differential amplifier Q4D, Q4E, and Q4F and transistors Q6 and Q7. When the input signal on the base of Q4E is more positive than the base Q4D, corresponding to Q4E on and Q4D, Q6, and Q7 off, the voltage at pin 10 of NAND gate B is high resulting in a "0" output on pin 8 of gate B, which is the synchronizer. When the input signal on the base of Q4D is more positive than the base of Q4E, corresponding to Q4E off and Q4D, Q6 and Q7 on, the voltage at pin 10 of NAND gate B is low resulting in a "1" output on pin 8 of gate B for the zero-crossing input into the synchronizer. The zero-crossing of the voltage waveform being monitored are thus converted into either a "0" or a "1" zero-crossing "D" signal which is fed into the synchronizer for synchronization with the signals from the main clock. The positive-going zero crossings are then used to propagate the reset pulse (RES) from the timing control circuit located on the twelve bit binary counter printed circuit module to reset the 16 bits of the binary counter to zero at the end of each period.

The clock signal to the binary counter is provided on the main clock and 4 bit binary counter printed circuit module by a stable crystal oscillator which uses the parallel resonance of the crystal CL-1 in the circuitry associated with field-effect transistor Q8 to produce a 1.966080 megahertz clock signal, CPO.

The 16 bit binary counter is located on the main clock and four bit binary counter printed circuit module (bits [0], [1], [2], and [3],) and the twelve bit binary counter printed circuit module (bits [4] through [15]). With a 1.966080 MHz clock frequency (CPO), bit [15] changes status every 16.6667 milliseconds. Since all the bits of the counter are reset to Zero at the beginning of each period [15] goes to "1" only if the actual period is longer than the 60 Hz. period. For frequencies ranging from 60 to 54 Hz the actual period ranges from 16.6667 to 18.5185 milliseconds. When [15] goes to "1" all bits from [0] to [14] go to ZERO. During the 1.8518 ms corresponding to the difference between 54 and 60 Hz periods there are 1821 CP1 clock pulses. (Bit [0] is used as a scaling stage to obtain a CP1 output at half the frequency of CPO). With the condition [15] = ONE, only the first 11 bits must be then decoded to detect if the input frequency falls below a present value from 60.00 Hz to 54.00 Hz set on the digital underfrequency trip-point setting assembly per Table 1. This is accomplished by the coincidence circuit generating a signal to the trip control circuitry where it is stored and utilized in a manner previously described.

CHARACTERISTICS

FREQUENCY RANGE (HZ)

The SDF-1 relay can be set at values from 54.00 to 60.00 Hz in increments of 0.05 Hz, with an accuracy of $\pm$0.007 Hz from the set point. The repeatability is thus $\pm$0.007 Hz.

(See Table I)

Increments of less than 0.05 Hz can be obtained if needed for unusual applications.

DC CONTROL VOLTAGE

The SDF-1 relay is designed to operate on either 48 or 125 volts dc by selecting jumper combination on dc power supply.

ENERGY REQUIREMENTS

AC Burden 7.3 Volt-Amperes at 120VAC 60 Hz.
DC Burden 14 Watts at 48 VDC Control Voltage
16 Watts at 125VDC Control Voltage

TIME DELAY RANGE

2 to 99 cycles in 1-cycle setting increments with a tolerance of better than ±5%. The total minimum operating time of the relay is 4 cycles −3 cycles of underfrequency detection and 1 cycle operating time for the trip relay. The timer will start *after* the first detected underfrequency cycle and, if set for 2 cycles of delay, will time out at the same time that tripping is enabled by the trip control logic.

OPERATING TIME

The operating time for the SDF-1 relay, taken from the first positive-going zero crossing of the ac potential wave after the underfrequency set-point is crossed, is equal to the time delay set on the front panel decade switches plus 2 cycles. This is because one cycle is used by the period-checking circuitry to determine that an underfrequency condition exists before the timer can be started; also, the tripping relay requires one cycle to pick up after the time delay expires. Trip control logic will not allow tripping to take place until at least 3 underfrequency cycles have been detected, regardless of a lower time delay setting; the minimum total operating time is thus 4 cycles if trip relay pickup time is included.

Examples of SDF-1 timing are illustrated in the figures. Refer to figure 14. Note that the relay senses frequency by measuring the time between positive going zero crossings. If the frequency is initially above the trip setting and then declines fairly linearly, as will occur in service, the relay will measure the *average* frequency over each cycle. Thus, it will detect the underfrequency condition during a given cycle only if the trip setting is crossed before that cycle is half-completed. Otherwise, detection will occur during the *following* cycle. The resultant timing variation is less than ±½ cycle. In the example of figure 14, the relay has a delay setting of 6 cycles on the front panel decade switches. The total time from underfrequency set-point crossing to trip contact closure will be between 7.5 and 8.5 cycles, depending on the position of the ac wave when the frequency setting is crossed.

Now refer to figure 15. Suppose that ac is suddenly applied at a frequency below the trip setting, as might occur during bench testing of the relay, or possibly in the midst of a frequency disturbance. In this case there will be a delay of up to, but less than, one cycle before the SDF-1 starts to measure the underfrequency condition. This variable time is in addition to the trip delay setting plus 2 cycles. In the example, the time from energization to contact closure will be between 8 and 9 cycles.

TRIP CIRCUIT

The main contacts will close 30 amperes at 250 volts dc and the seal-in contacts of the indicating contactor switch will safely carry this current long enough to trip a circuit breaker. Seismic ICS units are available in 0.2, 1.0, and 2.0 ampere (fixed rating) sizes.

TEMPERATURE RANGE

The SDF-1 is designed to operate over a temperature range from −30°C to + 70°C.

SETTINGS

UNDERFREQUENCY TRIP POINT

The SDF-1 relay is set for underfrequency trip by the tap screws in the underfrequency trip point setting assembly on the front panel of the relay. The binary settings for frequencies from 60.00 to 54.00 Hz in 0.05 Hz steps are given in Table I. When the tap screw is in the "1" upper position it contributes to the frequency setting as in the following weighting table.

TABLE II

Underfrequency Set Point Position Weights											
Binary Code Position	A	B	C	D	E	F	G	H	J	K	L
Weight ("1" Position)	1	2	4	8	16	32	64	128	256	512	1024

When the tap screw is in the "0" lower position it contributes 0 to the weight. The tap screws must be firmly tightened by hand in either of the two positions. *Note:* a screwdriver may be used to tighten the tap screws but caution should be exercised not to exert too much pressure on the screws.

An illustrative example is the assumption that a tripping point of 59.50 Hz is desired. The tap screws should be fastened in the following combination according to Table I.

	A	B	C	D	E	F	G	H	J	K	L
1		X		X				X			
0	X		X		X	X	X		X	X	X

Settings in increments as fine as the accuracy of the relay are possible, if needed for an unusual application. A request for the binary setting for a frequency not listed in Table I (but between 54.0 and 60.0 Hz) can be made through the nearest Westinghouse sales office.

Selecting a Frequency Setting

For load-shedding, the frequency is normally set as high as possible without approaching the region of normal system frequency swings (usually set 59.5 Hz or below). High settings, combined with short time delay, will provide greatest protection from severe system overload (see "Selecting a Time Delay" in the following section). A number of relays may be set in successively lower steps for more selective load-saving.

Trip Time Delay Setting

The trip time relay is set in 1-cycle increments with the decade switches on the front panel from the minimum of 2 cycles to 99 cycles (60 Hz base). The delay settings of the two controls are additive. A delay of less than 2 cycles is not possible because of trip control logic (as explained in "Theory of Operation"); setting below 2 cycles will be of no benefit. The timer will start *after* the first underfrequency cycle is recognized; the combined presence of outputs from the timer and from the trip control logic (indicating 3 consecutive underfrequency cycles) will enable tripping. The closing of the trip relay contact will require one additional cycle after the time delay has elapsed.

Note that the cycle calibrations assume a 60 Hz reference (i.e., one cycle equals 16.67 ms). The time delay is an analog function, unrelated to the ac input cycles.

Selecting a Time Delay

When a system overload occurs, underfrequency relays must disconnect load to arrest frequency decline. The output of generating plants may be impared below 57-57.5 Hz, so shedding must be completed before this level is reached. Shortest possible time delay is usually advantangeous. Note that, due to the frequency-checking technique of the SDF-1 relay, no intentional time delay is required to avoid misoperation for transients of short duration (such as phase-single shifts due to fault inception or clearing). However, time delay may be used to prevent response to misleading inputs (such as line excitation by a slowing motor load); or, in some schemes, to coordinate a number of relays set to the same frequency.

Fig. 13 shows the effect of time delay on the actual frequency at which tripping takes place under declining frequency conditions. The curves show how the frequency continues to drop in the time interval required for the relay to operate after its frequency set-point is crossed.

For example, suppose that for a system of inertia constant H = 2, it is required that the frequency not dip below 57.5 Hz for any overload up to 46%. Assume the relay is set to trip at 59.20 Hz. The scale at the bottom of figure 13 indicates that a 46% overload will cause a 6 Hz/sec rate of decline. According to Figure 13, the SDF-1 relay with 15 cycles of delay setting will close its trip contact when the frequency has dropped 1.7 Hz below the set point, or 57.5 Hz, for this overload condition. Thus, 15 cycles is the maximum acceptable time delay setting to obtain the desired protection.

Now suppose the relay trips a 5-cycle breaker. Since load must actually be disconnected to arrest frequency decline, the breaker operating time has the same effect as additional time delay setting.

Because 15 cycles is the longest tolerable delay, the relay should not have more than 10 cycles of delay setting.

The curves in Figure 13 have been plotted to include the effect of the delay setting, as labeled on each curve, along with two additional cycles for initial underfrequency detection and telephone relay operation. Thus, the curve corresponding to 2 cycles of delay setting is plotted for 4 cycles total SDF-1 operating time, etc. Use the curve whose label corresponds to the actual setting of the decade switches.

INSTALLATION

The relays should be mounted on switchboard panels or their equivalent in a location free from dirt, moisture, excessive vibration and heat. Mount the relay vertically by means of the mounting stud for the type FT projection case or by means of the four mounting holes on the flange for the semi-flush type FT case. Either the stud or the mounting screws may be utilized for grounding the relay. The electrical connections may be made directly to the terminals by means of screws for steel panel mounting or to the terminal stud furnished with the relay for thick panel mounting. The terminal stud may be easily removed or inserted by locking two nuts on the stud and then turning the proper nut with a wrench. See Fig. 16 for Outline and Drilling plan.

For detailed information on the FT case, refer to I.L. 41-076.

ADJUSTMENTS & MAINTENANCE

The proper adjustments to insure correct operation of this relay have been made at the factory. Upon receipt of the relay no customer adjustments, other then those covered under "SETTINGS" should be required.

ACCEPTANCE CHECK

It is recommended that an acceptance check be applied to the SDF-1 relay to verify that the circuits are functioning properly.

The following procedure can be used for this purpose.

NOTE

The relay is wired for 125 Vdc, when it is shipped from the factory. For 48 Vac application, change the jumper positions shown on the internal schematic drawing.

1. **Settings**

   Check front panel settings; they should be as follows:

   a. Underfrequency trip point desired set on the underfrequency trip point setting assembly as per Table I.

   b. Trip time delay set for the desired cycles delay on the trip time delay decade setting knobs.

2. **Indicating Contactor Switch**

   Close the trip relay contacts and pass sufficient dc current through the trip circuit (Relay terminals 1 and 10) to close the contacts of the ICS. This value of current should not be greater than the particular ICS value being used. The indicator target should drop freely.

3. **Underfrequency Trip Point Setting**

   Connect SDF-1 Relay per test diagram Figure 10. Using a variable frequency source apply 120 volts at set tripping frequency. Relay should trip within + .007 Hz of set trip frequency in the time set on the digital trip time setting plus 16 milliseconds operating time of the trip relay. Raise frequency of source above the trip point setting (.007 Hz. or higher) and the trip relay should drop out after approximately two cycles delay.

4. **Undervoltage Detector**

   Lower frequency of source so relay once again trips; lower voltage of source below 25 volts, and the trip relay should drop out.

5. **Test Module 1469C14G01 (Optional)**

Test module 1469C14G01 may be utilized to test the underfrequency trip setting of the SDF-1 relay. Disconnect AC to relay terminals 8 and 9 when using this test module. When inserted into its relay connector and test points T8 and T9 on module 1469C14G01 are connected together, underfrequency trip point settings may be checked by switching the same binary number on the test module that is set on the underfrequency trip point setting assembly to trip the relay. Likewise, dropping the test module setting down by a weight of one or greater (see Table II), corresponding to a higher frequency, will allow the relay to reset.

ROUTINE MAINTENANCE

All relays should be checked at least once every year or at such other intervals as may be dictated by experience to be suitable to the particular application.

CALIBRATION

Use the following procedures for calibrating the relay if the relay has been taken apart for repairs or the adjustments have been disturbed. This procedure should not be used unless it is apparent that the relay is not in proper working order. (See "Acceptance Check").

INDICATING CONTACTOR SWITCH (ICS)

Close the trip relay contacts and pass sufficient dc current through the trip circuit (Relay terminals 1 and 10) to close the contacts of the ICS. This value of current should not be greater than the particular ICS value being used. The indicator target should drop freely.

The contact gap should be approximately .047" between the bridging moving contact and the adjustable stationary contact. The bridging moving contact should touch both stationary contact simultaneously.

DC REGULATED SUPPLIES

The 5 Vdc supply is adjustable and can be adjusted by potentiometer P1 on power supply module 1600C95G01. The 18 Vdc supply is referenced to the 5 volt supply and needs no adjustment. Both dc supplies should be maintained within ±5% for the dc power supply between 90 V and 140 V or 42 V and 56 V for the supply voltage of 125 Vdc or 48 Vdc respectively.

MAIN CLOCK ADJUSTMENT

Inductor L-1 should be adjusted to obtain the correct clock signal CPO at TP2 on module 1469C15G01. The correct signal is 1.966080 MHz. with a tolerance range of 1.965980 MHz. to 1.966180 MHz.

UNDERFREQUENCY TRIP TEST

Connect the SDF-1 Relay per test diagram Figure 10. Using a variable frequency source apply 120 volts at set tripping frequency. Relay should trip within ±0.007 Hz. of set trip frequency in the time set on the trip time delay setting plus 16 milliseconds operating time of the trip relay. Raise frequency of source 0.007 Hz or higher above the trip point setting and the trip relay should drop out after approximately two cycles delay.

TRIP CONTROL CIRCUIT AND DELAY TIMER ADJUSTMENT

Potentiometer R46 on module 1469C17G01 must be adjusted to bring the 99 cycle delay setting to 99 cycles (60 Hz base), i.e., 1.650 seconds. Remember that the total operating time is equal to the delay setting plus 2 additional cycles. Thus, at 99 cycles delay setting the potentiometer R46 should be set so that the total operating time is 101 cycles or 1.683 seconds. The delay timer should be tested at each position on the selector switch. (Note: Delay settings for 1 to 2 cycles will give the minimum delay of 2 cycles and can only be checked at a higher setting: i.e. 1 cycle has to be checked at 11 cycles delay setting, or 21, 31, etc.).

TEST MODULE 1469C14G01 (Optional)

Test module 1469C14G01 may be utilized to test the underfrequency trip setting of the SDF-1 relay. Disconnect AC to relay terminals 8 and 9 when using this test module. When inserted into its relay connector and test points T8 and T9 on

module 1469C16G01 are connected together, underfrequency trip point settings (Table I) may be checked by switching the same binary number on the test module that is set on the underfrequency trip point setting assembly to trip the relay. Likewise, dropping the test module setting down by a weight of one or greater (see Table II), corresponding to a higher frequency, will allow the relay to reset.

RENEWAL PARTS

Repair work can be done most satisfactorily at the factory. However, interchangeable parts can be furnished to the customers who are equipped for doing repair work. When ordering parts, always give the complete nameplate data.

TABLE I

FREQ. (HZ)	PERIOD (MS)	UNDERFREQUENCY TRIP POINT SETTING										
		A	B	C	D	E	F	G	H	J	K	L
60.00	16.6667	0	0	0	0	0	0	0	0	0	0	0
59.95	16.6806	0	1	1	1	0	0	0	0	0	0	0
59.90	16.6945	1	1	0	1	1	0	0	0	0	0	0
59.85	16.7084	1	0	0	1	0	1	0	0	0	0	0
59.80	16.7224	1	1	1	0	1	1	0	0	0	0	0
59.75	16.7364	1	0	1	0	0	0	1	0	0	0	0
59.70	16.7504	0	1	0	0	1	0	1	0	0	0	0
59.65	17.7645	0	0	0	0	0	1	1	0	0	0	0
59.60	16.7785	0	1	1	1	0	1	1	0	0	0	0
59.55	16.7926	0	0	1	1	1	1	1	0	0	0	0
59.50	16.8067	0	1	0	1	0	0	0	1	0	0	0
59.45	16.8209	0	0	0	1	1	0	0	1	0	0	0
59.40	16.8350	1	0	1	0	0	1	0	1	0	0	0
59.35	16.8492	1	1	0	0	1	1	0	1	0	0	0
59.30	16.8634	1	0	0	0	0	0	1	1	0	0	0
59.25	16.8776	1	1	1	1	0	0	1	1	0	0	0
59.20	16.8919	1	0	1	1	1	0	1	1	0	0	0
59.15	16.9062	1	1	0	1	0	1	1	1	0	0	0
59.10	16.9205	0	1	0	1	1	1	1	1	0	0	0
59.05	16.9348	0	0	0	1	0	0	0	0	1	0	0
59.00	16.9492	0	1	1	0	1	0	0	0	1	0	0
58.95	16.9635	0	0	1	0	0	1	0	0	1	0	0
58.90	16.9779	0	1	0	0	1	1	0	0	1	0	0
58.85	16.9924	0	0	0	0	0	0	1	0	1	0	0
58.80	17.0068	0	1	1	1	0	0	1	0	1	0	0
58.75	17.0213	1	0	1	1	1	0	1	0	1	0	0
58.70	17.0358	1	1	0	1	0	1	1	0	1	0	0
58.65	17.0503	1	0	0	1	1	1	1	0	1	0	0
58.60	17.0648	1	1	1	0	0	0	0	1	1	0	0
58.55	17.0794	0	1	1	0	1	0	0	1	1	0	0
58.50	17.0940	0	0	1	0	0	1	0	1	1	0	0
58.45	17.1086	0	1	0	0	1	1	0	1	1	0	0
58.40	17.1233	1	0	0	0	0	0	1	1	1	0	0
58.35	17.1380	1	1	1	1	0	0	1	1	1	0	0
58.30	17.1527	0	1	1	1	1	0	1	1	1	0	0
58.25	17.1674	0	0	1	1	0	1	1	1	1	0	0
58.20	17.1821	1	1	0	1	1	1	1	1	1	0	0
58.15	17.1969	1	0	0	1	0	0	0	0	0	1	0
58.10	17.2117	0	0	0	1	1	0	0	0	0	1	0
58.05	17.2265	0	1	1	0	0	1	0	0	0	1	0
58.00	17.2414	1	0	1	0	1	1	0	0	0	1	0
57.95	17.2563	0	0	1	0	0	0	1	0	0	1	0
57.90	17.2712	0	1	0	0	1	0	1	0	0	1	0
57.85	17.2861	1	0	0	0	0	1	1	0	0	1	0
57.80	17.3010	0	0	0	0	1	1	1	0	0	1	0
57.75	17.3160	0	1	1	1	1	1	1	0	0	1	0
57.70	17.3310	1	0	1	1	0	0	0	1	0	1	0
57.65	17.3461	0	0	1	1	1	0	0	1	0	1	0
57.60	17.3611	1	1	0	1	0	1	0	1	0	1	0
57.55	17.3762	1	0	0	1	1	1	0	1	0	1	0
57.50	17.3913	0	0	0	1	0	0	1	1	0	1	0
57.45	17.4064	1	1	1	0	1	0	1	1	0	1	0
57.40	17.4216	0	1	1	0	0	1	1	1	0	1	0
57.35	17.4368	1	0	1	0	1	1	1	1	0	1	0
57.30	17.4520	0	0	1	0	0	0	0	0	1	1	0
57.25	17.4672	1	1	0	0	1	0	0	0	1	1	0
57.20	17.4825	0	1	0	0	0	1	0	0	1	1	0
57.15	17.4978	1	0	0	0	1	1	0	0	1	1	0
57.10	17.5131	0	0	0	0	0	0	1	0	1	1	0
57.05	17.5285	1	1	1	1	0	0	1	0	1	1	0

TABLE I (Cont.)

FREQ. (HZ)	PERIOD (MS)	UNDERFREQUENCY TRIP POINT SETTING										
		A	B	C	D	E	F	G	H	J	K	L
57.00	17.5439	0	1	1	1	1	0	1	0	1	1	0
56.95	17.5593	1	0	1	1	0	1	1	0	1	1	0
56.90	17.5747	1	0	1	1	1	1	1	0	1	1	0
56.85	17.5901	0	0	1	1	0	0	0	1	1	1	0
56.80	17.6056	1	1	0	1	1	0	0	1	1	1	0
56.75	17.6211	0	1	0	1	0	1	0	1	1	1	0
56.70	17.6367	0	1	0	1	1	1	0	1	1	1	0
56.65	17.6523	1	0	0	1	0	0	1	1	1	1	0
56.60	17.6678	0	0	0	1	1	0	1	1	1	1	0
56.55	17.6835	0	0	0	1	0	1	1	1	1	1	0
56.50	17.6991	1	1	1	0	1	1	1	1	1	1	0
56.45	17.7148	0	1	1	0	0	0	0	0	0	0	1
56.40	17.7305	0	1	1	0	1	0	0	0	0	0	1
56.35	17.7462	1	0	1	0	0	1	0	0	0	0	1
56.30	17.7620	1	0	1	0	1	1	0	0	0	0	1
56.25	17.7778	0	0	1	0	0	0	1	0	0	0	1
56.20	17.7936	0	0	1	0	1	0	1	0	0	0	1
56.15	17.8094	1	1	0	0	0	1	1	0	0	0	1
56.10	17.8253	1	1	0	0	1	1	1	0	0	0	1
56.05	17.8412	1	1	0	0	0	0	0	1	0	0	1
56.00	17.8571	0	1	0	0	1	0	0	1	0	0	1
55.95	17.8731	0	1	0	0	0	1	0	1	0	0	1
55.90	17.8891	0	1	0	0	1	1	0	1	0	0	1
55.85	17.9051	1	0	0	0	0	0	1	1	0	0	1
55.80	17.9211	1	0	0	0	1	0	1	1	0	0	1
55.75	17.9372	1	0	0	0	0	1	1	1	0	0	1
55.70	17.9533	1	0	0	0	1	1	1	1	0	0	1
55.65	17.9695	1	0	0	0	0	0	0	0	1	0	1
55.60	17.9856	1	0	0	0	1	0	0	0	1	0	1
55.55	18.0018	0	0	0	0	0	1	0	0	1	0	1
55.50	18.0180	0	0	0	0	1	1	0	0	1	0	1
55.45	18.0343	0	0	0	0	0	0	1	0	1	0	1
55.40	18.0505	0	0	0	0	1	0	1	0	1	0	1
55.35	18.0668	0	0	0	0	0	1	1	0	1	0	1
55.30	18.0832	0	0	0	0	1	1	1	0	1	0	1
55.25	18.0995	1	0	0	0	0	0	0	1	1	0	1
55.20	18.1159	1	0	0	0	1	0	0	1	1	0	1
55.15	18.1324	1	0	0	0	0	1	0	1	1	0	1
55.10	18.1488	1	0	0	0	1	1	0	1	1	0	1
55.05	18.1653	1	0	0	0	0	0	1	1	1	0	1
55.00	18.1818	1	0	0	0	1	0	1	1	1	0	1
54.95	18.1984	0	1	0	0	0	1	1	1	1	0	1
54.90	18.2149	0	1	0	0	1	1	1	1	1	0	1
54.85	18.2315	0	1	0	0	0	0	0	0	0	1	1
54.80	18.2482	1	1	0	0	1	0	0	0	0	1	1
54.75	18.2648	1	1	0	0	0	1	0	0	0	1	1
54.70	18.2815	1	1	0	0	1	1	0	0	0	1	1
54.65	18.2983	0	0	1	0	0	0	1	0	0	1	1
54.60	18.3150	0	0	1	0	1	0	1	0	0	1	1
54.55	18.3318	1	0	1	0	0	1	1	0	0	1	1
54.50	18.3486	1	0	1	0	1	1	1	0	0	1	1
54.45	18.3655	0	1	1	0	0	0	0	1	0	1	1
54.40	18.3824	1	1	1	0	1	0	0	1	0	1	1
54.35	18.3993	1	1	1	0	0	1	0	1	0	1	1
54.30	18.4162	0	0	0	1	1	1	0	1	0	1	1
54.25	18.4332	1	0	0	1	0	0	1	1	0	1	1
54.20	18.4502	1	0	0	1	1	0	1	1	0	1	1
54.15	18.4672	0	1	0	1	0	1	1	1	0	1	1
54.10	18.4843	1	1	0	1	1	1	1	1	0	1	1
54.05	18.5014	0	0	1	1	0	0	0	0	1	1	1
54.00	18.5185	0	0	1	1	1	0	0	0	1	1	1

ELECTRICAL PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
RESISTORS		
R1	68 K Ohm 5% 1/2W	184A763H71
R2	4.3 K Ohm 5% 1/2W	184A763H42
R3, R4, R7, R30, R32, R41	3 K Ohm 5% 1/2W	184A763H38
R5	5.1 K Ohm 5% 1/2W	184A763H44
R6, R33	1.8 K Ohm 5% 1/2W	184A763H33
R8	3.3 K Ohm 5% 1/2W	184A763H39
R9	3.57 K Ohm 1% 1/2W	862A376H54
R10	1.78 K Ohm 1% 1/2W	862A376H25
R11, R13	2.43 K Ohm 1% 1/2W	862A376H38
R12	15 K Ohm 5% 1/2W	184A763H55
R14	1.1 K Ohm 1% 1/2W	862A376H05
R15, R54, R55	10 K Ohm 1% 1/2W	862A377H30
R17	9.1 K Ohm 5% 1/2W	184A763H50
R18	1.5 K Ohm 5% 1/2W	184A763H31
R19, R20	22.1 K Ohm 1% 1/2W	862A377H34
R21, R22, R23, R24	2 K Ohm 1% 1/2W	763A126H18
R25	2.7 K Ohm 5% 1/2W	184A763H37
R26, R27	1.2 K Ohm 5% 1/2W	184A763H29
R28	56 K Ohm 5% 1/2W	184A763H69
R29, R39	5.6 K Ohm 5% 1/2W	184A763H45
R31, R38	2.4 K Ohm 5% 1/2W	184A763H36
R34, R37	330 K Ohm 5% 1/2W	184A763H15
R35, R36	300 K Ohm 5% 1/2W	184A763H86
R40	2.2 K Ohm 5% 1/2W	184A763H35
R42	120 Ohm 5% 1/2W	184A763H05
R43	75 K Ohm 5% 1/2W	184A763H72
R45	11 K Ohm 1% 1/2W	862A377H05
R46	2 K Ohm 10% 1/2W	862A406H01
R47	1.87 K Ohm 1% 1/2W	862A376H27
R50	49.9 Ohm 1% 1/2W	862A374H68
R51, R56, R58	3 K Ohm 5% 1/2W	184A763H38
R52	39 K Ohm 5% 1/2W	184A763H65
R57, R16	10 K Ohm 5% 1/2W	184A763H51
R59	10 Ohm 5% 25W	04D1297H27
R53	100 K Ohm 5% 1/2W	184A763H75
R90, R91, R92, R93, R94, R97, R98	1.21 K Ohm 1% 1/2W	848A829H56
R100, 101, 102, 103, 104, 105, 106, 107, 108	1.21 K Ohm 1% 1/2W	848A820H53
R200	47 Ohm 5% 1/2W	187A290H17
CAPACITORS		
C1, C16, C20, C30, C33, C36, C39	.47 MFD 50V 20%	762A680H04
C2, C8, C11, C40	.1 MFD 100V 10%	836A620H03
C3, C5	.47 MFD 200V 10%	188A669H01
C4	100 PFD 200V 10%	836A620H01
C6, C7	50 PFP 500V 2%	762A757H25
C9	10 PFD 200V	879A989H01

ELECTRICAL PARTS LIST (Contd.)

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
CAPACITORS (Contd.)		
C10	.018 MFD 100V 10%	836A620H04
C12	500 PFD 500V	184A663H05
C13	51 PFD 500V 2%	763A209H18
C14	250 PFD 500V 2%	861A46H11
C15, C17, C19	100 PFD 1000V 2%	184A663H06
C18	8 MFD 30V 5%	862A177H07
C32, C38	1.0 MFD 200V 20%	876A409H10
C34	4.7 MFD 35V ±10%	184A661H12
C35	5.6 PFD 200V ±10%	880A403H05
DIODES		
D1, D2, D7, D8, D10, D12, D13, D14, D15 D28, A, B, C, D, E, F, G, H, J, K, L	1N4148	836A928H06
D3, D4, D5, D6	1N645	837A692H03
D9, D11	1N457A	184A855H07
ZENER DIODES		
Z1, Z7	1N747A	837A398H08
Z2	1N965B	186A797H08
Z3	1N962B	837A398H09
Z4	1N753A	862A606H01
INPUT/OUTPUT MODULE		
R1A, R2A	150 Ohm 1/2W	1724641
D1A	1.5 KE68	878A619H02
C1A, C3A, C4A	.022 MFD	1544921
C2A	.05 MFD	1728695
C6A, C7A, C9A, C10A, C14A, C15A	.01 MFD	3516A36H03
C5A, C8A, C11A, C13A, C16A	.004 MFD	879A911H12
C17A	.01 MFD	879A911H12
Telephone Relay		407C733H04
TRANSISTORS		
Q1, Q2, Q3, Q5, Q7, Q9, Q11, Q12, Q13, Q15	2N2905A	762A672H11
Q4, Q6, Q10, Q16, Q29	2N2905A	762A672H10
Q8	2N4222	878A577H01
Q14	D13T1	878A289H01
Q27	2N3055	187A673H08
Q28	DTSD410	187A673H09

ELECTRICAL PARTS LIST (Contd.)

CIRCUIT SYMBOL	DESCRIPTION	WESTINGHOUSE STYLE NUMBER
INTEGRATED CIRCUITS		
IQ4	CA3026	717B205H01
A, Q, V, W	U6A993059X	204C328H04
B, K, L, R, S, T, U	U6A994659X	204C328H03
C, D, E, F, I, J, P	U6A993259X	204C328H01
G, H	U6A993659X	204C328H02
COUNTER BITS 0-1, 2-3, 4-5, 6-7, 8-9, 10-11, 12-13, 14-15		
TRIP 1-2	U6A909959X	204C331H01
TRANSFORMERS-INDUCTORS		
T1	Input Isolation Transformer	878A574H01
L1	Inductor	878A654H01
L3, L4	Inductor	3500A27H02
MISCELLANEOUS		
TR	Trip Relay	541D514H36
CL1 (60HZ)	Crystal	187A857H23
TEST MODULE 1469C14G01 (Optional)		
R1	120 Ohm 1/2W 5%	184A763H05
C1	.47 MFD 35V 10%	187A508H05
C2	100 PFD 200V 10%	836A620H01
C3	.1 MFD 100V 10%	836A620H03
D1 to D11	1N4148	878A469H01
A	U6A993059X	204C328H04
B	U6A994659X	204C328H03
C	U6A993259X	204C328H01
Switch	(11 Req'd)	878A645H01

POWER SUPPLY MODULE – STYLE 1600C95G01

COMP	PART NAME	DESCRIPTION	STYLE NO.
C01	Capacitor	.001 MF 20% 3000V Cer	3536A32H01
C04	Capacitor	.1 MFD ±5% 500V	184A663H14
C05	Capacitor	.1 MFD ±5% 500V	184A663H14
C06	Capacitor	5 MFD +75/-10% 25V	186A341H07
C07	Capacitor	.1 MFD ±5% 500V	184A663H14
C08	Capacitor	210 MFD 250V 2-5/8x1	3529A07H01
C09	Capacitor	1000 PF 1KV ±10% Cer	762A680H02
C10	Capacitor	.47 MFD ±5% 200V Mylar	876A409H17

ELECTRICAL PARTS LIST (Contd.)

POWER SUPPLY MODULE – STYLE 1600C95G01			
COMP	**PART NAME**	**DESCRIPTION**	**STYLE NO.**
C11	Capacitor	470 PF 1KV ±10% Cer	879A911H10
C12	Capacitor	470 PF 1KV ±10% Cer	879A911H10
C13	Capacitor	100 MFD +100/-10% 50V EL	3535A92H01
C14	Capacitor	1500 PF ±10% 1KV Cer	762A680H05
C15	Capacitor	1000 PF 1KV ±10% Cer	762A680H02
C16	Capacitor	1500 PF ±10% 1KV Cer	762A680H05
C17	Capacitor	100 UF 50V +100/-10% EL	9641A08H02
C18	Capacitor	1000 PF 1KV ±10% Cer	762A680H05
C19	Capacitor	100 UF 20V +100/-10% EL	9641A08H01
C20	Capacitor	270 PF 500V ±2% Mica	762A757H12
C21	Capacitor	.1 MFD 100V ±20% Cer	762A680H14
C22	Capacitor	.22 MFD 100V ±20% Cer	3512A08H02
C23	Capacitor	.1 MFD 100V ±20% Cer	762A680H14
C24	Capacitor	.1 MFD 100V ±20% Cer	762A680H14
C25	Capacitor	.01 MFD 200V ±5% Met-Poly Carb	3534A68H03
C26	Capacitor	100 MFD +75/-10% 25V EL	186A341H02
C27	Capacitor	.027 MFD ±10%	188A669H14
C28	Capacitor	.01 MFD 100V +20% Cer	184A663H01
D01	Zener	1.5KE200 200V 10% 5W 1.5KW SG	878A619H01
D02	Diode	1N4936 400V 1A	836A928H10
D03	Diode	1N645A 225V .2 Amp	837A692H03
D04	Diode	1N645A 225V .2 Amp	837A692H03
D05	Diode	1N4148 100V	836A928H06
D06	Diode	MR851 100V 3A Rectifier	3535A29H03
D07	Diode	MR851 100V 3A Rectifier	3535A29H03
D08	Diode	MR851 100V 3A Rectifier	3535A29H03
D09	Diode	MR851 100V 3A Rectifier	3535A29H03
D10	Diode	1N645A 225V .2 Amp	837A692H03
D11	Diode	1N4148 100V	836A928H06
Z01	Zener	1N5352B 15V 5% 5W	862A288H04
Z03	Zener	1N966B 16V 5% 400MW	862A288H05
Z04	Zener	1N3050B 180V 5% 1W	187A936H17
Z05	Zener	UZ5240 400V 10% 5W	837A693H17
Z08	Zener	1N959 8.2V 20% 400MW	837A398H12
Z09	Zener	1N957B 6.8V 5% 400MW	186A797H06
Q01	Transistor	2N2222A NPN	762A672H15
Q02	Transistor	2N2907A PNP	762A672H17
Q03	Transistor	IRF720 400V 3A	9641A07H01
Q04	Transistor	2N2222A NPN	762A672H15
Q05	Transistor	2N2222A NPN	762A672H15
Q06	Transistor	2N2222A NPN	762A672H15
Q07	Transistor	2N2222A NPN	762A672H15
Q08	Transistor	2N2222A NPN	762A672H15

ELECTRICAL PARTS LIST (Contd.)

POWER SUPPLY MODULE – STYLE 1600C95G01			
COMP	**PART NAME**	**DESCRIPTION**	**STYLE NO.**
IC01	Int Ckt	UA741C	6277D61H08
IC02	Int Ckt	SG1524 Pulse Width Modulator	3534A92H01
IC03	Int Ckt	MC14011 Bal Quad-2 Input Nand	3527A09H02
IC04	Int Ckt	MC14011 Bal Quad-2 Input Nand	3527A09H02
T01	Core		1492B01G01
L01	Car Coil	1.28MH	3535A63G01
L02	Car Coil	1.28MH	3535A63G01
P02	Pot	2K 10% .5W Pot (Top Adjust)	3523A42H03
P03	Pot	Var 1K Ohm 1DT (Top Adjust)	3523A42H03
J01	Jumper	Bluechip Jumper	3532A54H01
J02	Jumper	Bluechip Jumper	3532A54H01
J03	Jumper	Bluechip Jumper	3532A54H01
J04	Jumper	Bluechip Jumper	3532A54H01
J05	Jumper	Bluechip Jumper	3532A54H01
J01	Connector	3 Position	9640A47H01
J02	Connector	3 Position	9640A47H01
J03	Connector	3 Position	9640A47H01
J04	Connector	3 Position	9640A47H01
J05	Connector	3 Position	9640A47H01
R01	Resistor	10 Ohm 5W 3%	629A923H15
R02	Resistor	10K 3W 5% W.W.	763A127H15
R03	Resistor	2000 Ohm 2W 5%	185A207H34
R04	Resistor	0 Ohm	862A478H01
R05	Resistor	30.1 Ohm 1/4W 1% Metal Film	848A818H01
R06	Resistor	1 Ohm .50W 5% W.W.	863A164H01
R07	Resistor	1 Ohm .50W 5% W.W.	863A164H01
R08	Resistor	250 Ohm 1% 5W Min. Wire Wound	3529A28H01
R09	Resistor	20K Ohm .5W 2% M.G.	629A531H63
R10	Resistor	1K 1% .25W	863A174H01
R11	Resistor	2K 1% .25W	863A174H30
R12	Resistor	10K 1% .25W	863A175H01
R13	Resistor	10K 1% .25W	863A175H01
R14	Resistor	2K 2% 1/2W M.G.	629A531H39
R15	Resistor	100K 1% .25W	863A175H97
R16	Resistor	16.K .50W ±2%	629A531H37
R17	Resistor	100 Ohm .5W 2%	629A531H08
R18	Resistor	1K 1% .25W	863A174H01
R19	Resistor	100 Ohm .5W 2%	629A531H08
R20	Resistor	20K 1% .25W	863A175H30
R21	Resistor	20K 1% .25W	863A175H30
R22	Resistor	3.01K .25W 1% Metal Film	848A819H94
R23	Resistor	10K 2% 1/2W M.G.	629A531H56
R24	Resistor	30.1K 1% .25W	863A175H47
R25	Resistor	51.1K 1% .25W	863A175H69
R26	Resistor	100 Ohm .5W 2%	629A531H08

✪ ELECTRICAL PARTS LIST (Contd.)

POWER SUPPLY MODULE – STYLE 1600C95G01			
COMP	PART NAME	DESCRIPTION	STYLE NO.
R27	Resistor	100 Ohm .5W 2%	629A531H08
R28	Resistor	150 Ohm 1% .25W	863A173H18
R29	Resistor	1K 1% .25W	863A174H01
R30	Resistor	750 Ohm 1% .25W	863A173H85
R31	Resistor	2K 1% .25W	863A174H30
R32	Resistor	20K 1% .25W	863A175H30
R33	Resistor	5.11K 1% .25W	863A174H69
R34	Resistor	5.11K 1% .25W	863A174H69
R35	Resistor	5.11K 1% .25W	863A174H69
R36	Resistor	1K 1% .25W	863A174H01
R37	Resistor	4.75K Ohm 1% .125W	863A174H66
R38	Resistor	32.4K 1% .25W	863A175H50
R39	Resistor	4.75K Ohm 1% .125W	863A174H66
R40	Resistor	100 Ohm 5W 1% W.W.	763A130H03
R41	Resistor	13.0K Ohm .125W 1% M.F.	863A175H12
R42	Resistor	5.11K 1% .25W	863A174H69
R43	Resistor	2K 1% .25W	863A174H30
R44	Resistor	10K 1% .25W	863A175H01
R45	Resistor	2 Ohm 1W 5% Molded Comp	629A371H23
R46	Resistor	383 Ohm 3W 1%	763A531H01
R47	Resistor	51.1K 1/4W 1% Metal Film	848A821H14

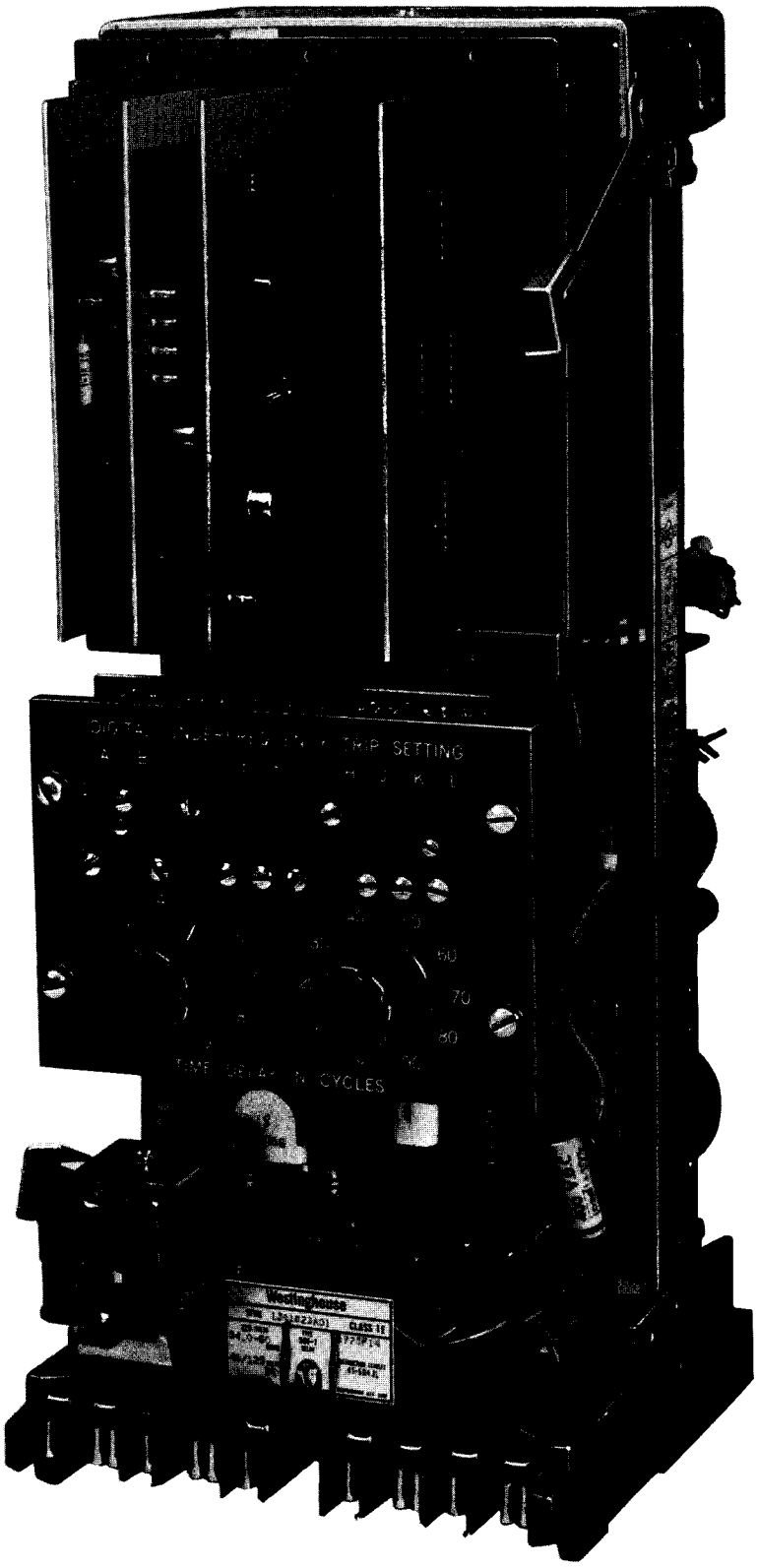


Fig. 1. Type 1E SDF-1 Underfrequency Relay Front View (Without Case)

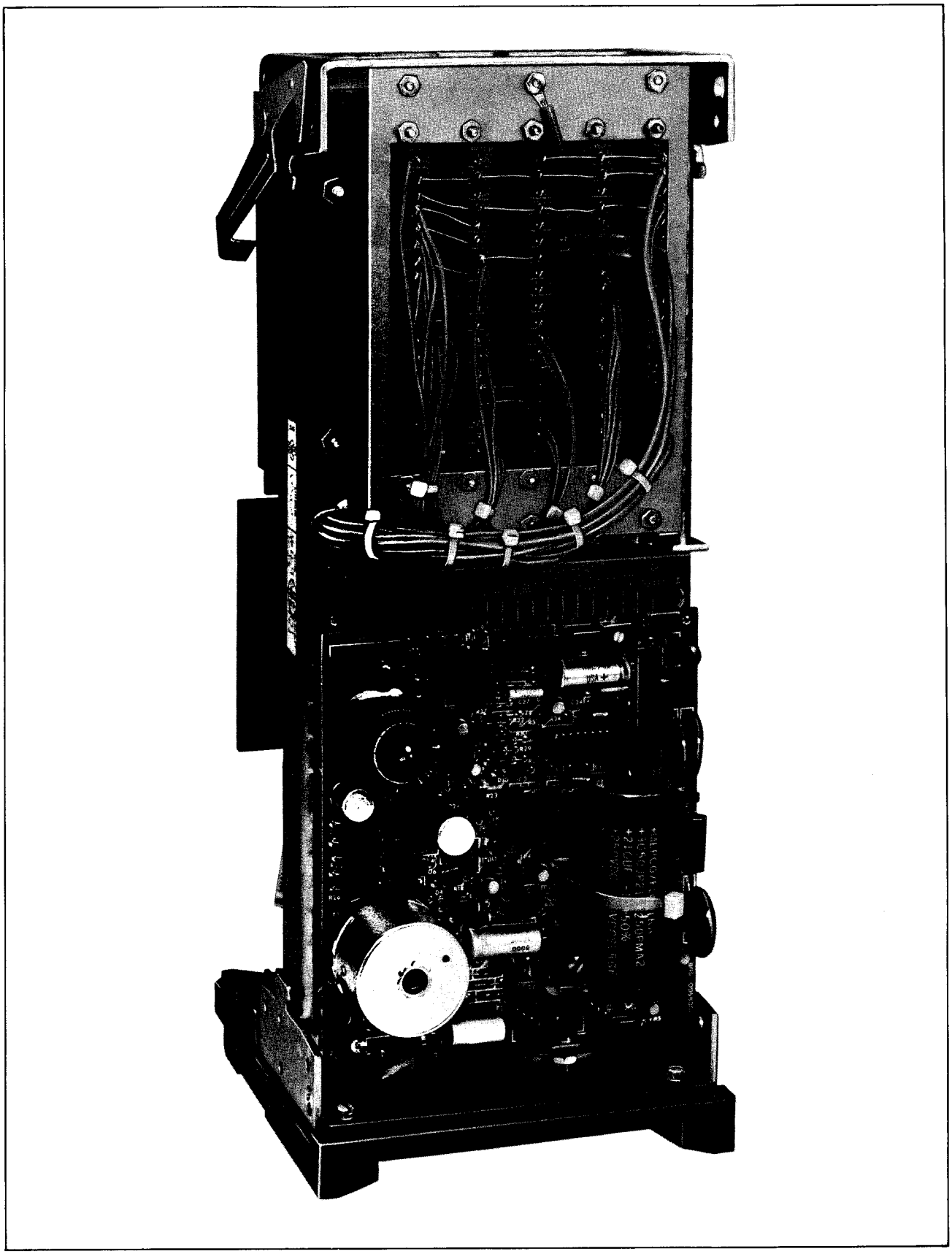


Fig. 2. Type 1E SDF-1 Underfrequency Relay Rear View (Without Case)

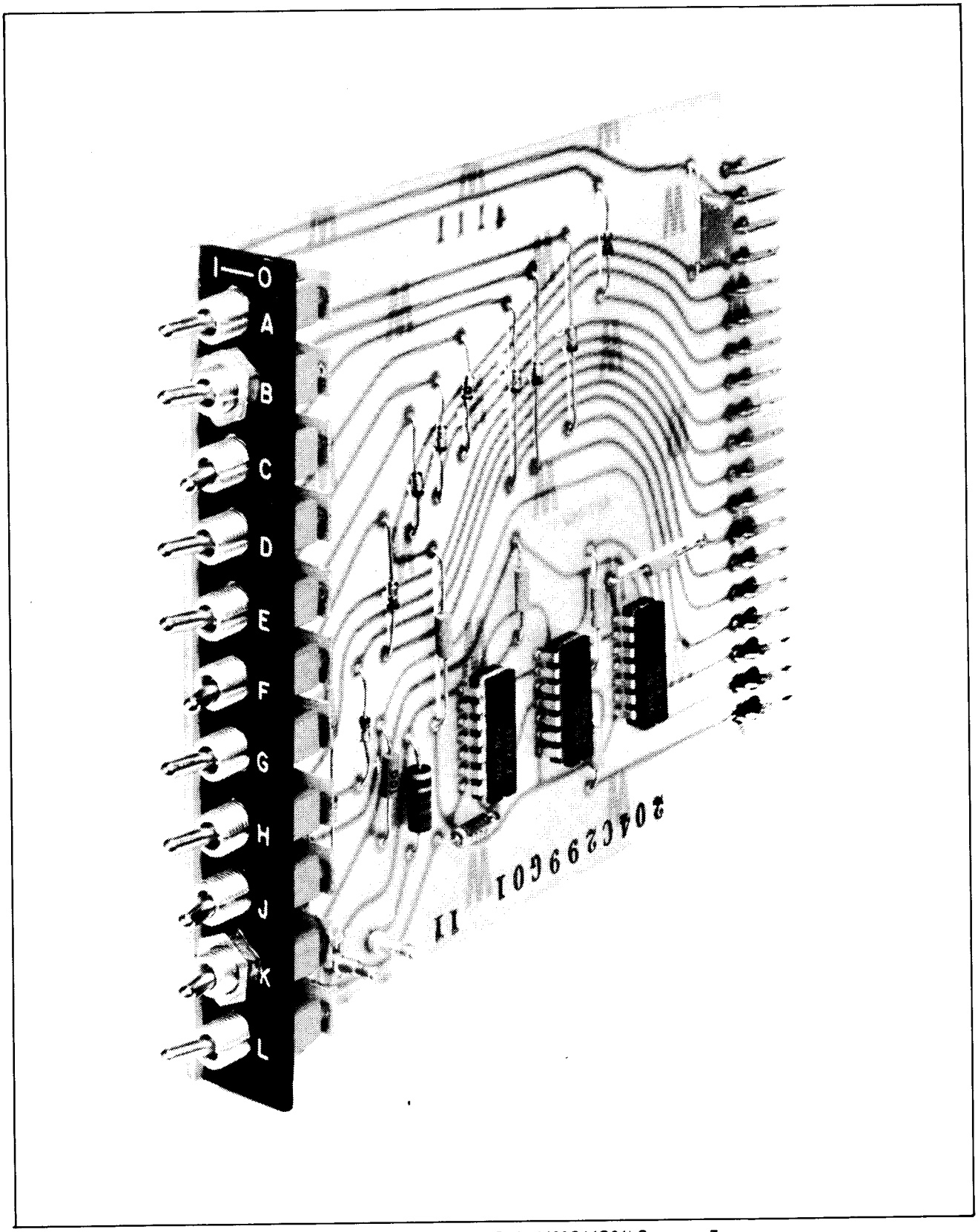


Fig. 2A. Optional Test Module (Style 1469C14G01) See page 7.

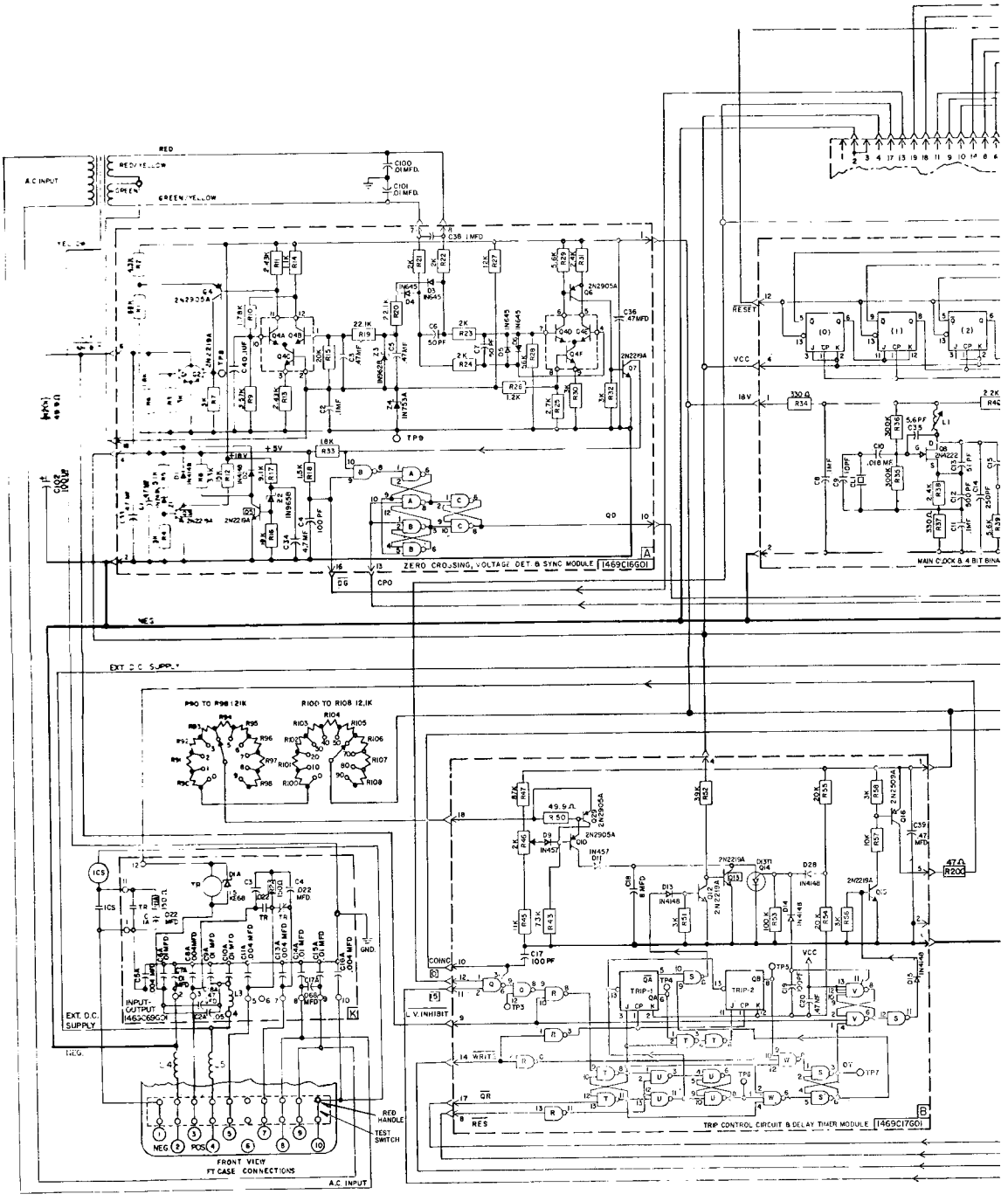
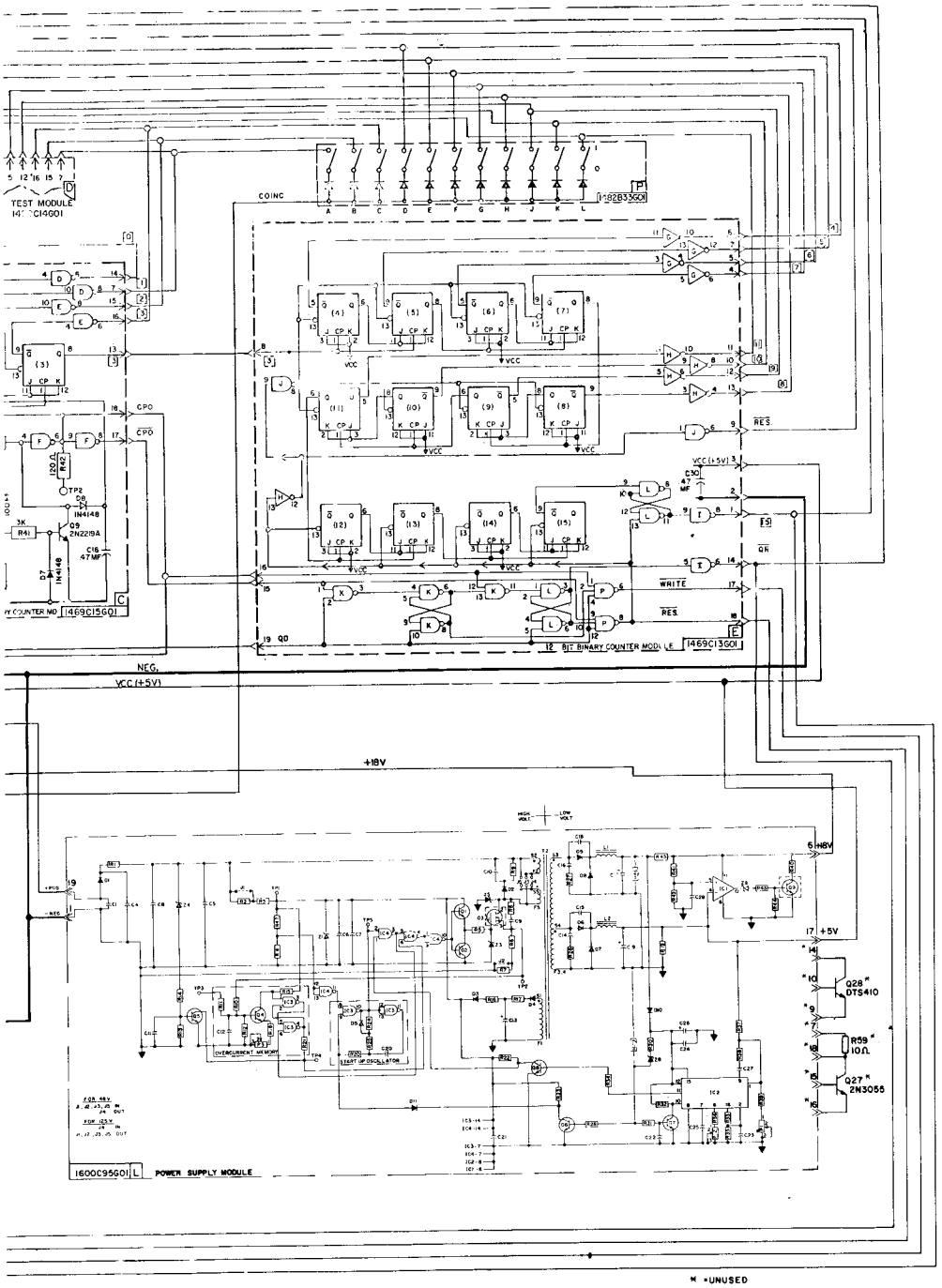


Fig. 3. Internal Schem



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atic Drawing.

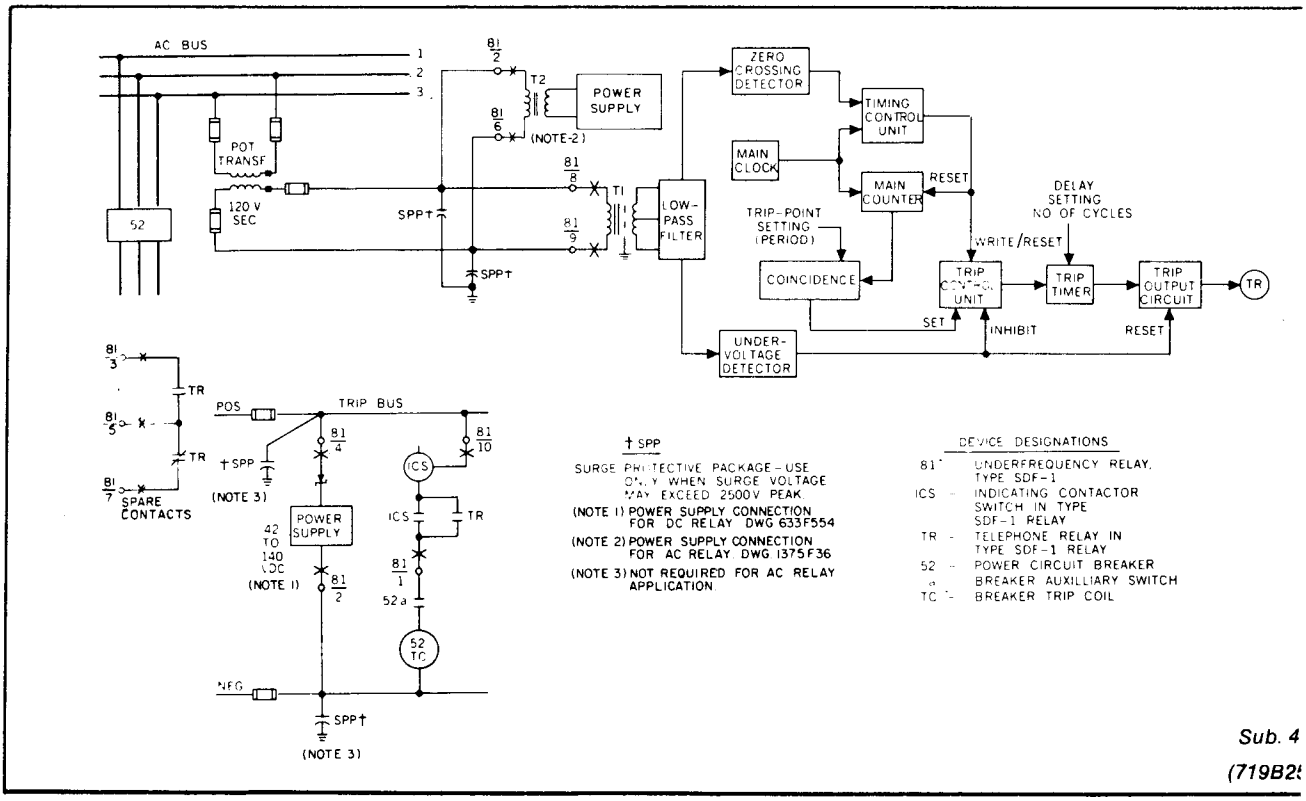

Fig. 4. External Schematic and Logic Diagram.

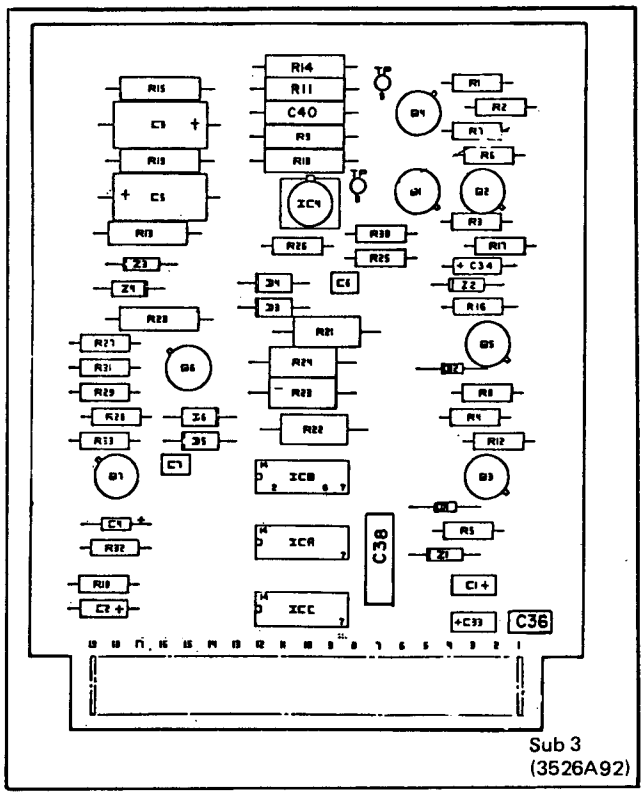

Fig. 5. Zero Crossing, Voltage Detectors, and Synchronizer Printed Circuit Module Component Location.

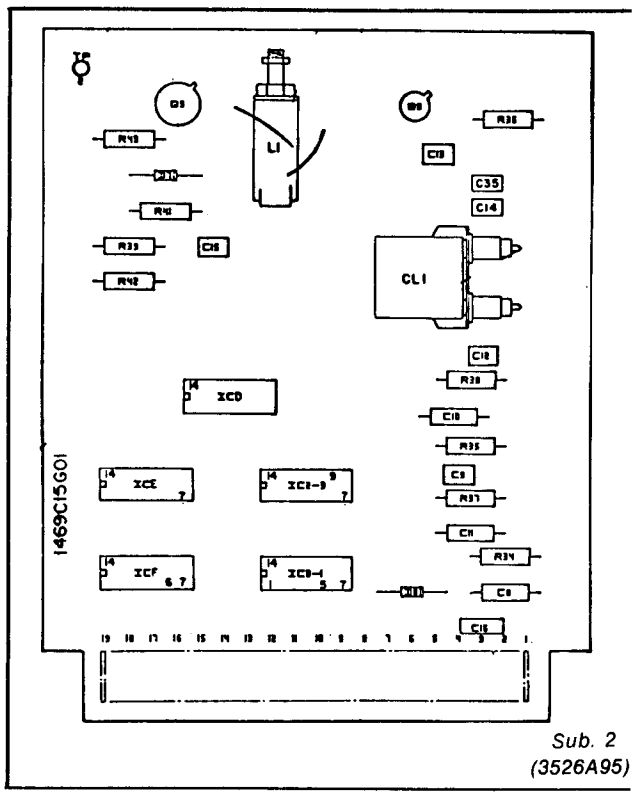

Fig. 6. Main Clock and Four Bit Binary Counter Printed Circuit Module Component Location.

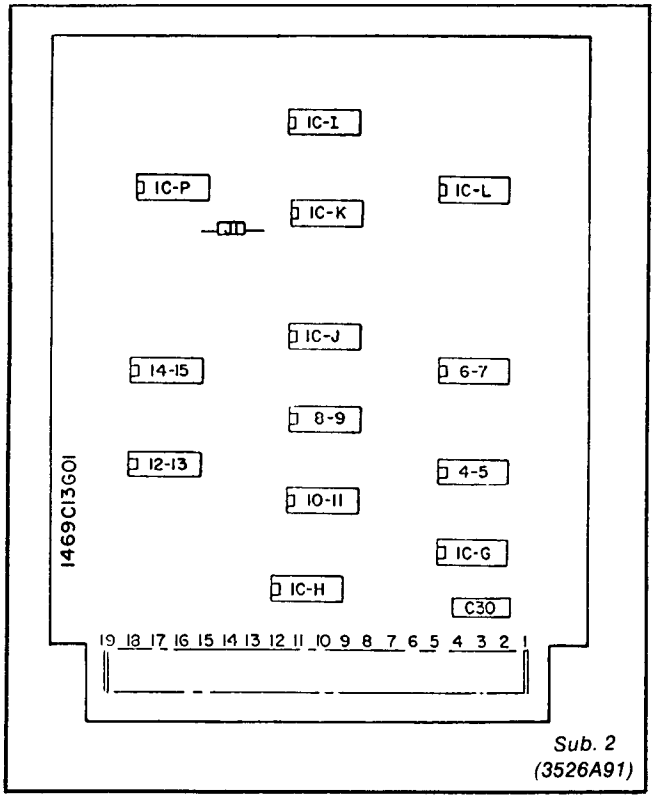

Fig. 7. Twelve Bit Binary Counter Printed Circuit Module Component Location.

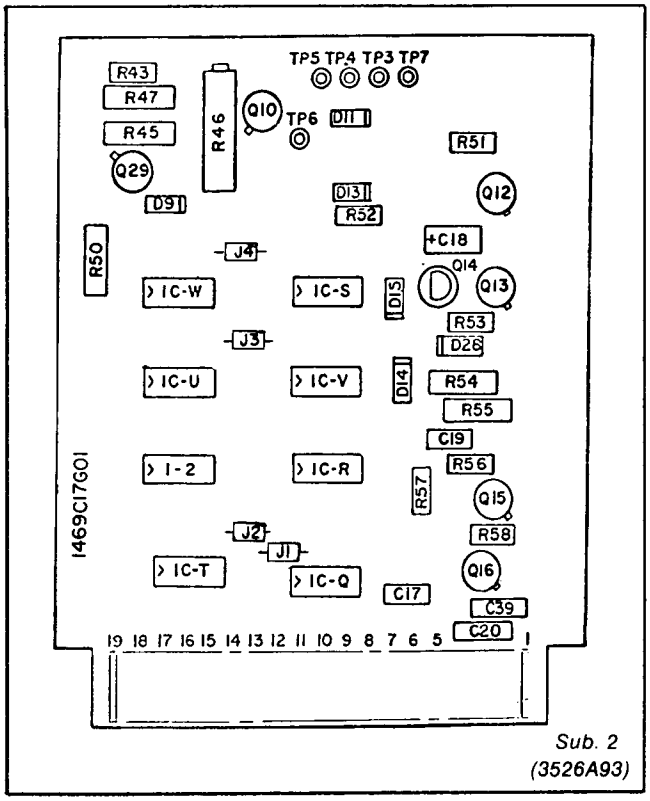

Fig. 8. Trip Control Circuit and Delay Timer Printed Circuit Module Component Location.

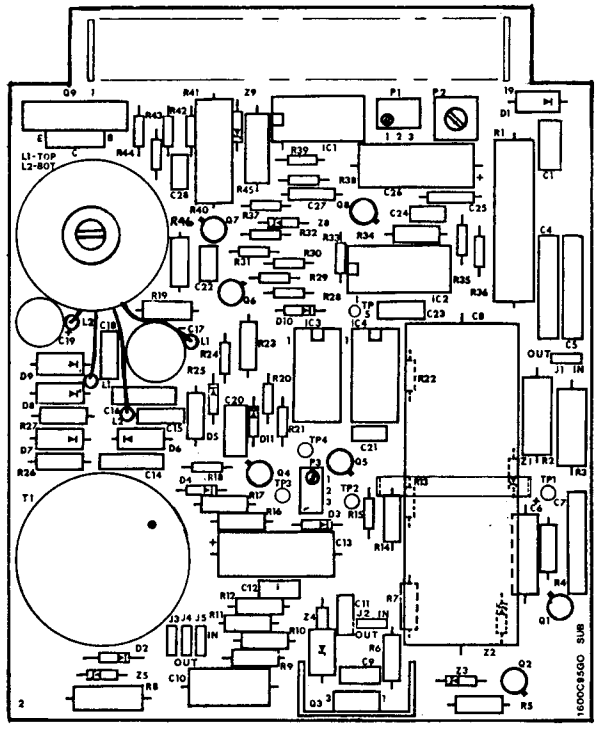

Fig. 9. Power Supply Printed Circuit Module Component Location.

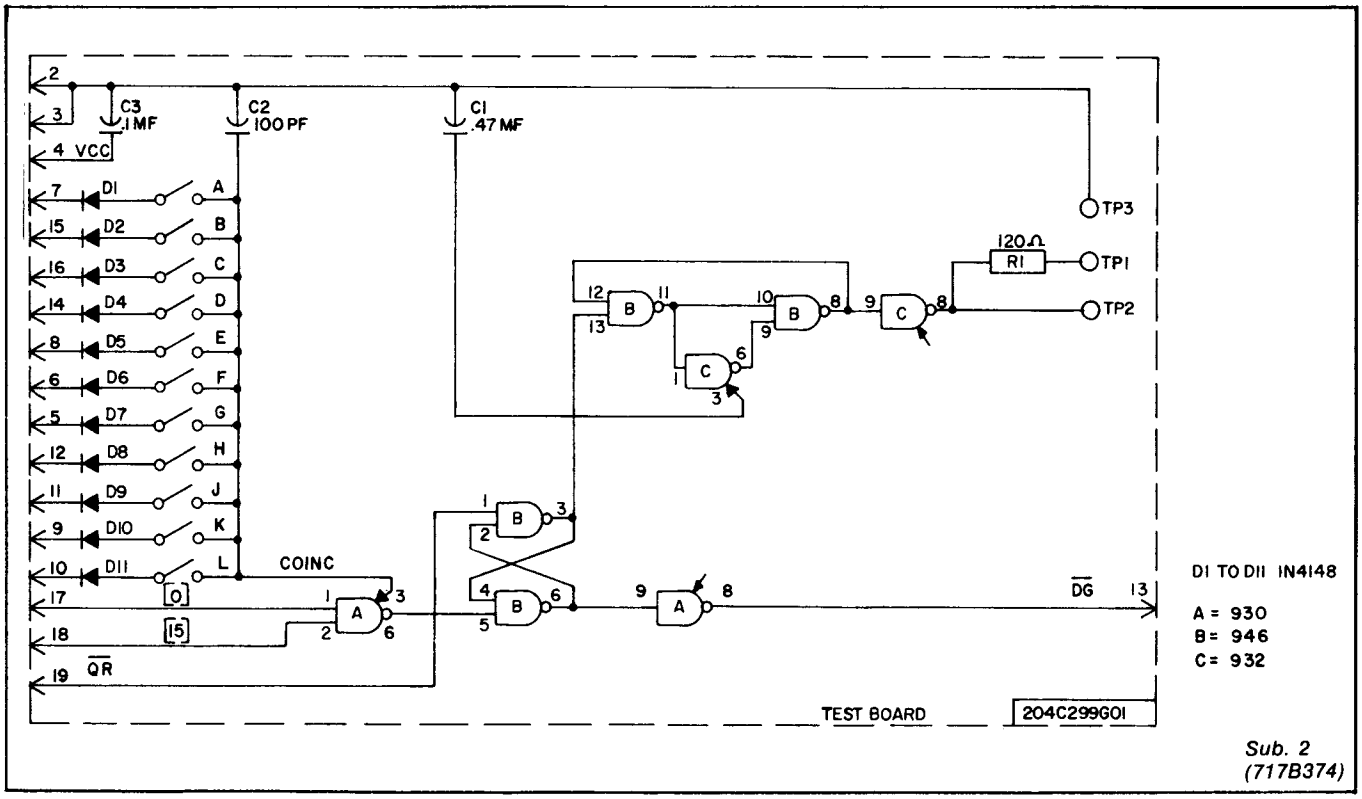

Fig. 10. Test Module Internal Schematic (Optional)

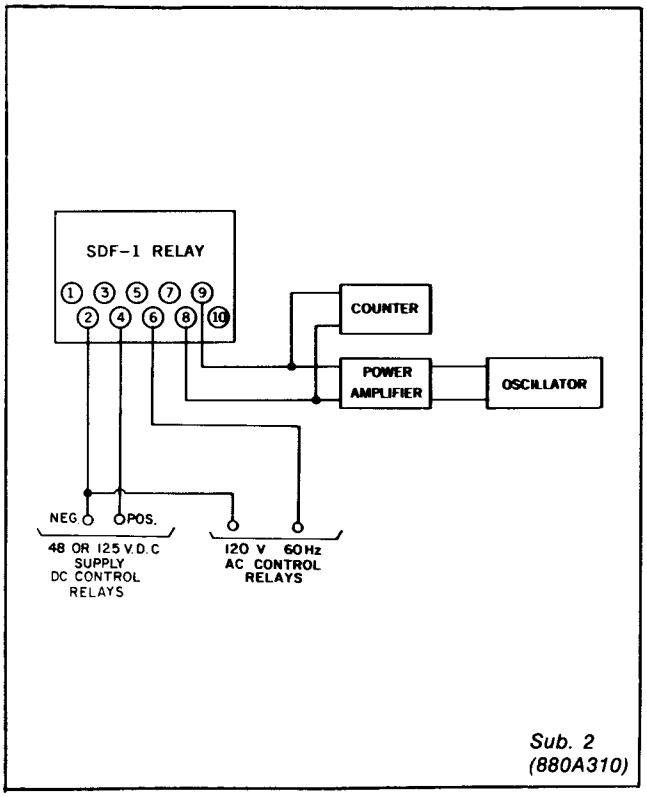

Fig. 11. Diagram of Test Connections for SDF-1 Relay.

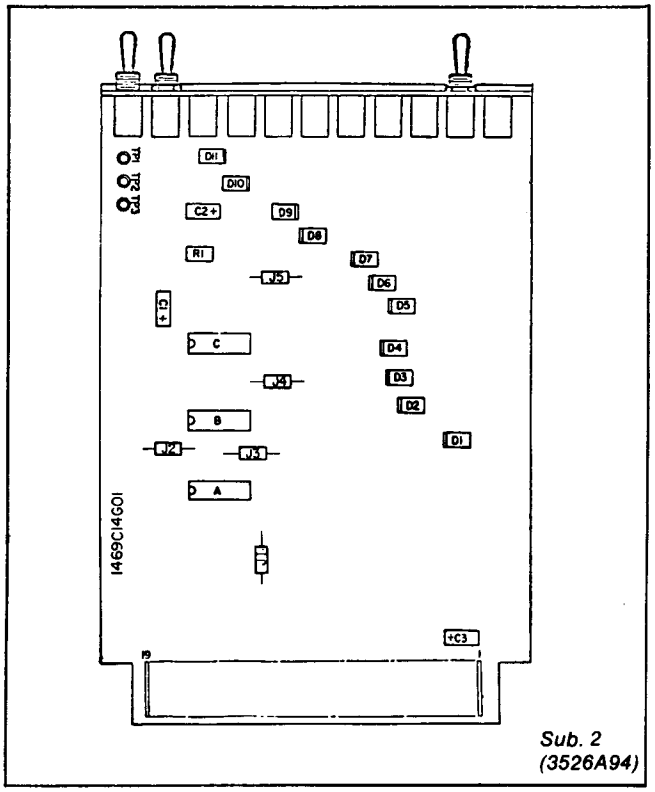

Fig. 12. Test Module Component Location.

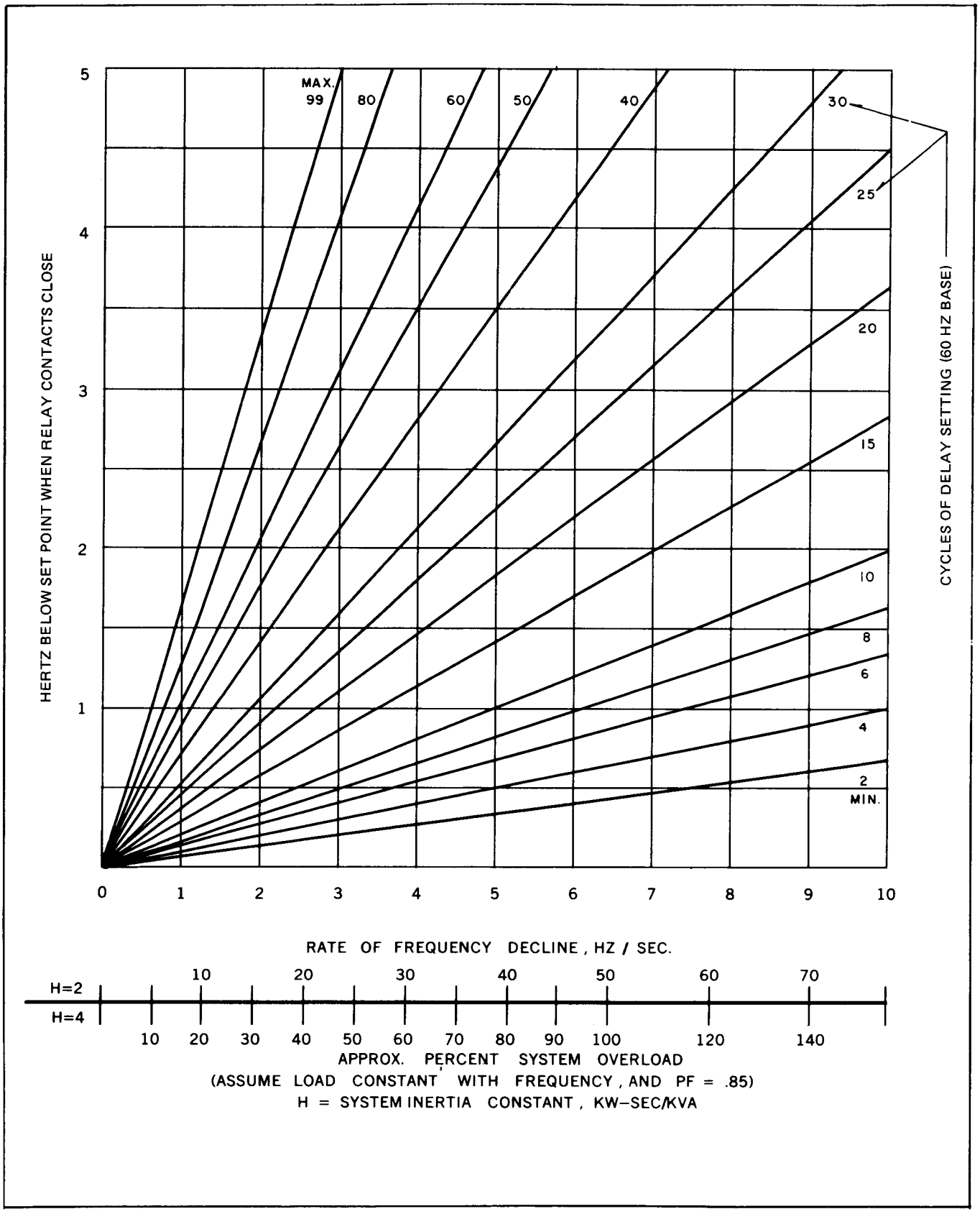

Fig. 13. SDF-1 Relay Tripping Delay Under Declining Frequency Conditions.

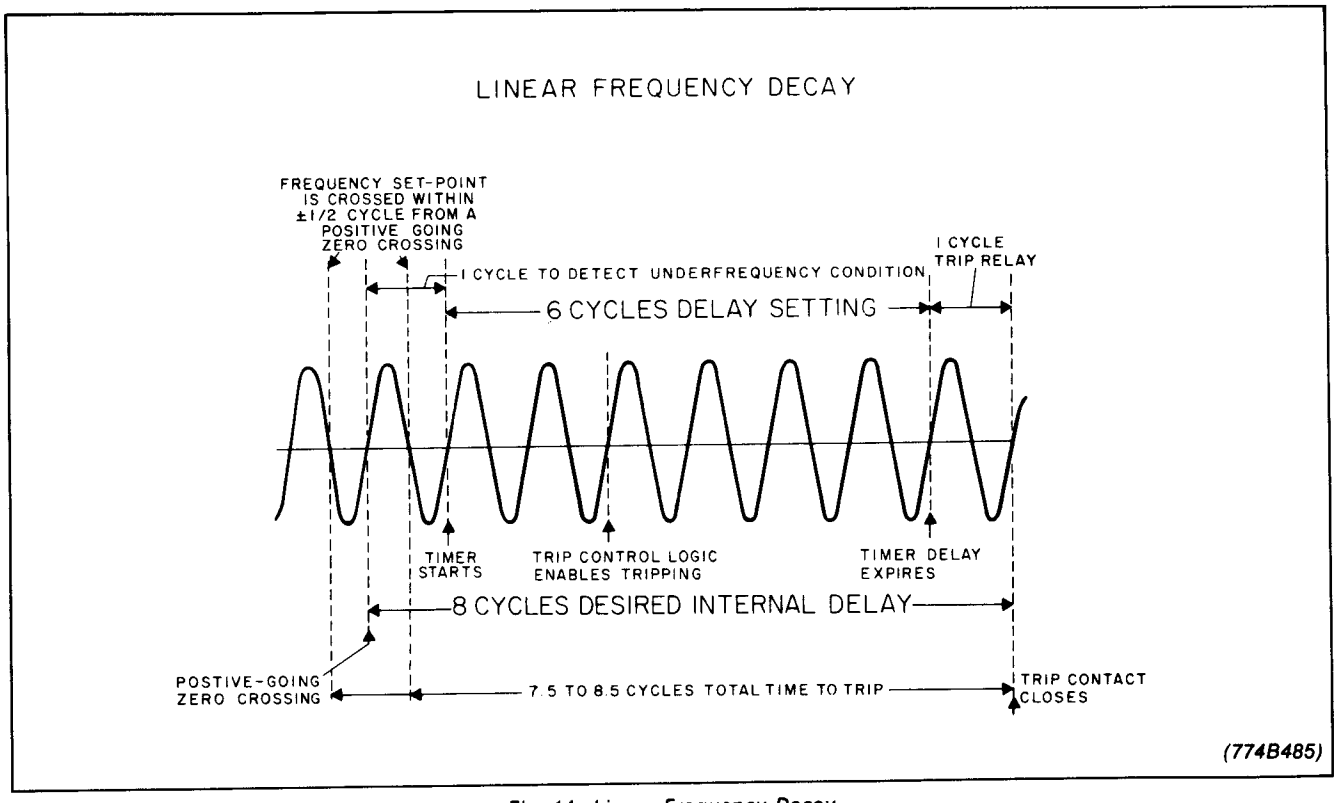

Fig. 14. Linear Frequency Decay.

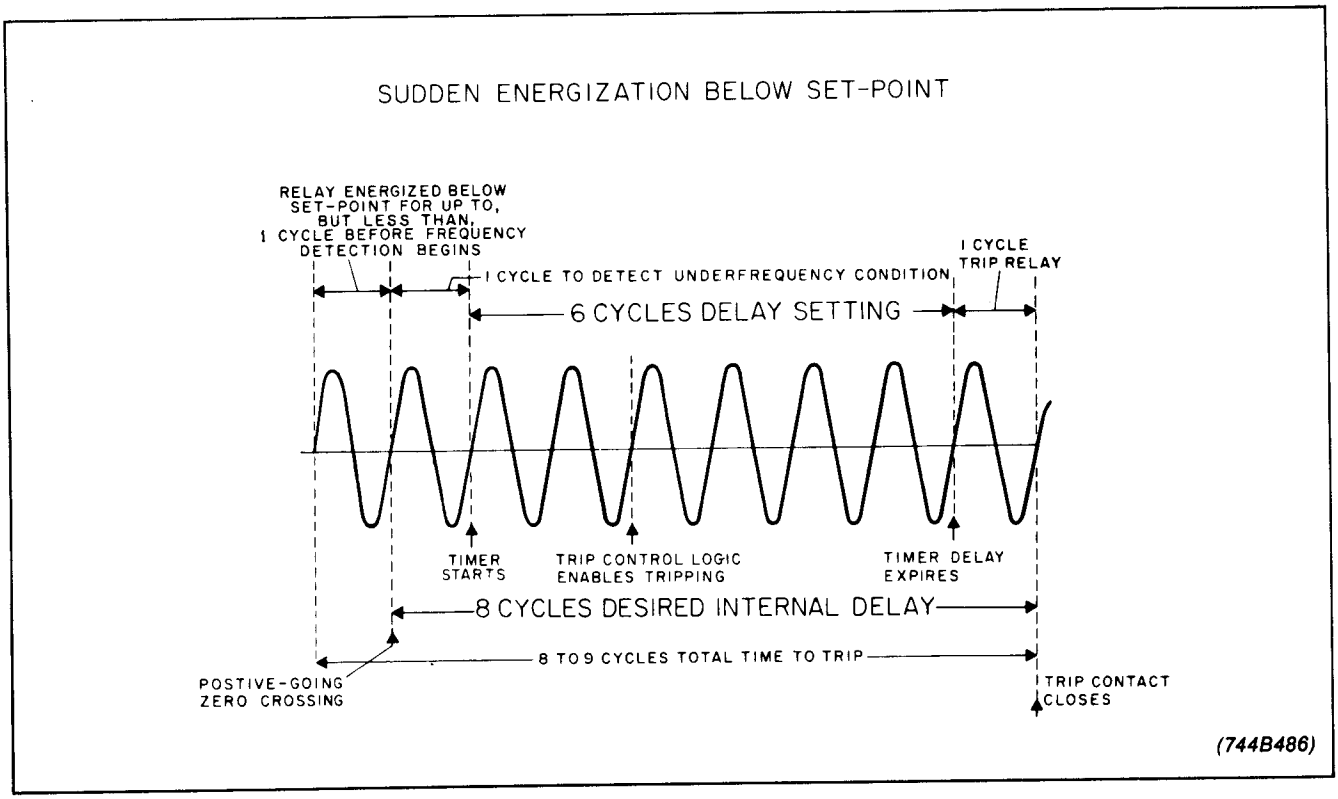

Fig. 15. Sudden Energization Below Set-Point.

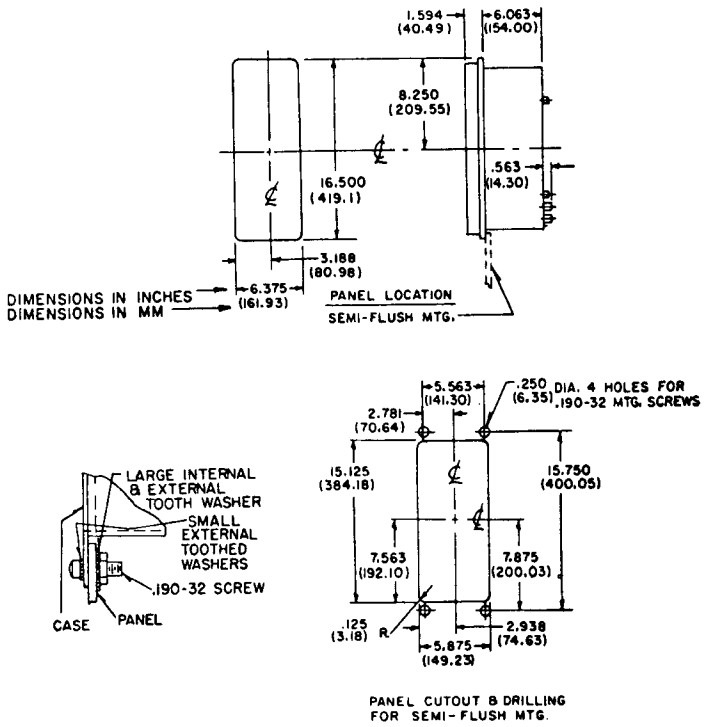

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Fig. 16. Outline and Drilling Plan for the 1E SDF-1 Relay in the Type FT-31 Case.

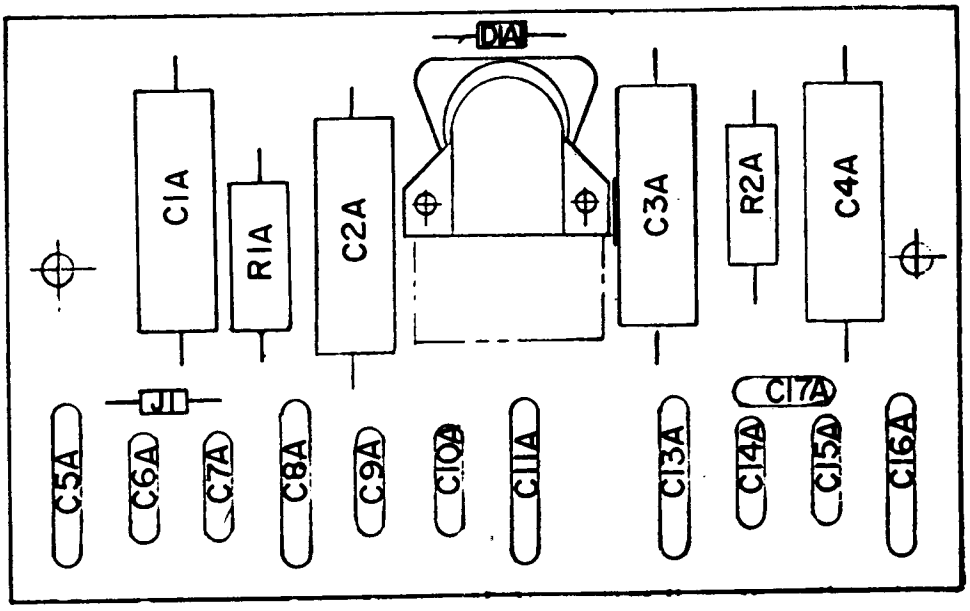

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Fig. 17. Input Output Module Component Location

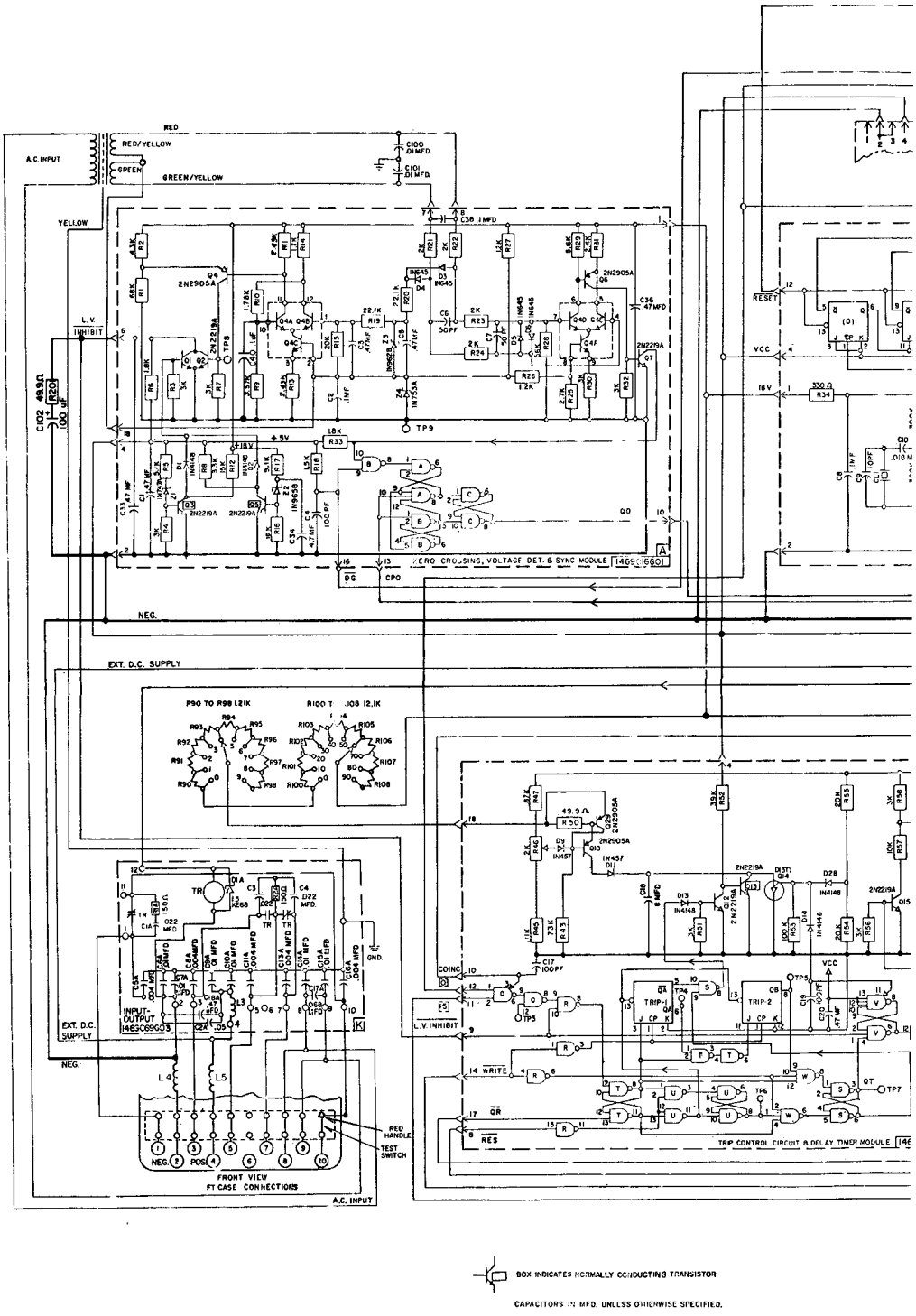
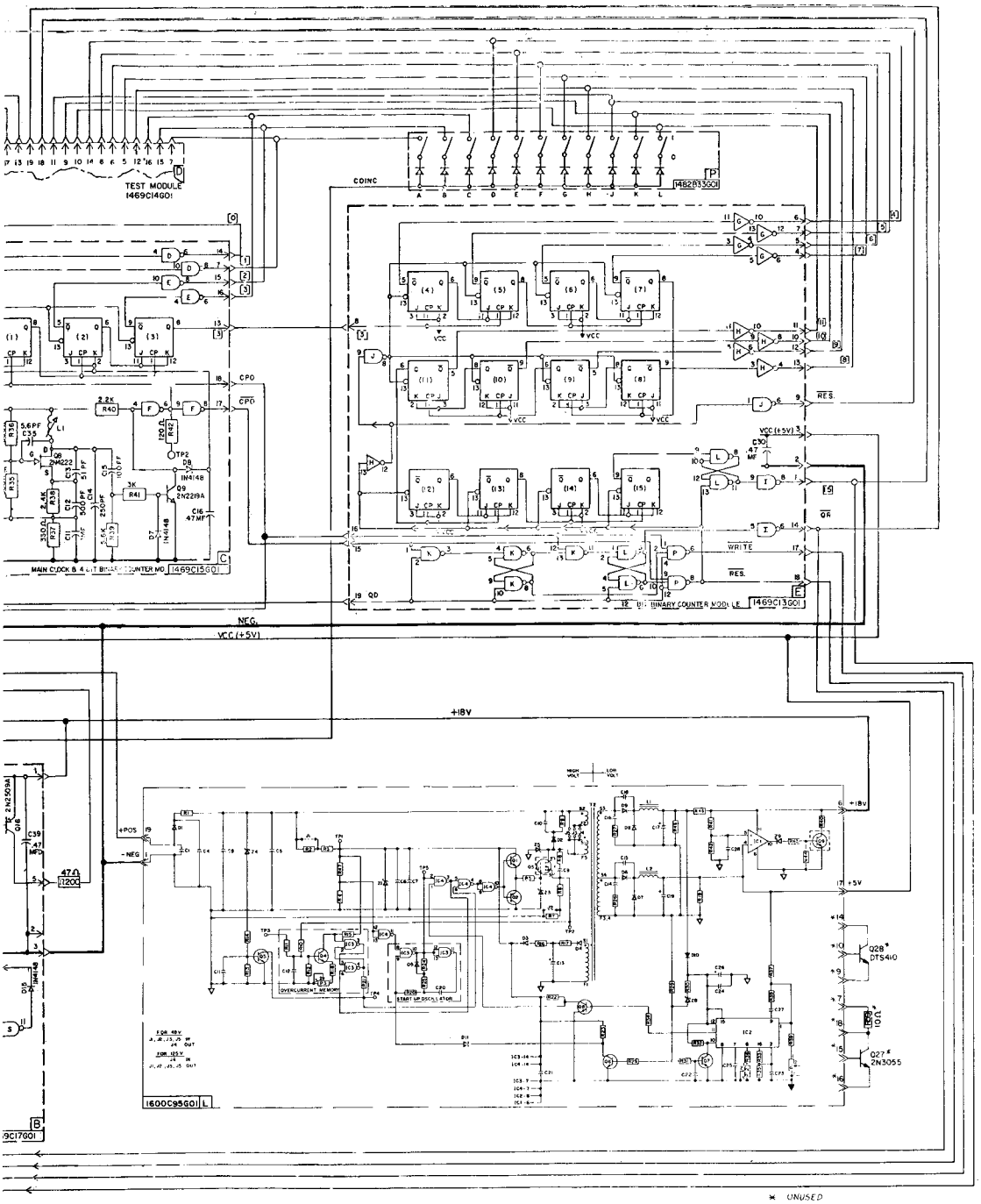


Fig. 18. Internal Schemat



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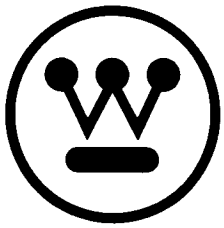
ic Drawing with Two NC Contacts



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