SEL-352-1, -2

BREAKER FAILURE RELAY
CONTROL RELAY
DATA RECORDER

INSTRUCTION MANUAL

SCHWEITZER ENGINEERING LABORATORIES
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CAUTION: The relay contains devices sensitive to electrostatic discharge (ESD). When working on the relay with front or top cover removed, work surfaces and personnel must be properly grounded or equipment damage may result.

CAUTION: There is danger of explosion if the battery is incorrectly replaced. Replace only with Ray-O-Vac® no. BR2335 or equivalent recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.

CAUTION: Automated clearing of the event buffer should be limited to reduce the possibility of wearing out the nonvolatile memory. Limit automated HIS C commands to once per week or less.

CAUTION: Automated clearing of the SER buffer should be limited to reduce the possibility of wearing out the nonvolatile memory. Limit automated SER C commands to once per week or less.

CAUTION: Automated clearing of the breaker report should be limited to reduce the possibility of wearing out the nonvolatile memory. Limit automated BRE C commands to once per week or less.

WARNING: This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.

DANGER: Removal of this front panel exposes circuitry which may cause electrical shock that can result in injury or death.

DANGER: Contact with instrument terminals may cause electrical shock which can result in injury or death.

ATTENTION: Le relais contient des pièces sensibles aux décharges électrostatiques (DES). Quand on travaille sur le relais avec le panneau avant ou du dessus enlevé, les surfaces de travail et le personnel doivent être mis à la terre convenablement pour éviter les dommages à l'équipement.

ATTENTION: Il y a un danger d'explosion si la pile électrique n'est pas correctement remplacée. Utiliser exclusivement Ray-O-Vac® No. BR2335 ou un équivalent recommandé par le fabricant. Se débarrasser des piles usagées suivant les instructions du fabricant.

ATTENTION: Le nombre de suppressions automatiques de l'information sur les évènements devrait être réduit afin de ne pas user la mémoire non-volatile. Limiter la commande automatique HIS C à une opération par semaine ou moins.

ATTENTION: Le nombre de suppressions automatiques de l'information sur les SER devrait être réduit afin de ne pas user la mémoire non-volatile. Limiter la commande automatique SER C à une opération par semaine ou moins.

ATTENTION: Le nombre de suppressions automatiques des rapports sur le disjoncteur devrait être réduit afin de ne pas user la mémoire non-volatile. Limiter la commande automatique BRE C à une opération par semaine ou moins.

AVERTISSEMENT: Cet équipement est expédié avec des mots de passe par défaut. A l'installation, les mots de passe par défaut devront être changés pour des mots de passe confidentiels. Dans le cas contraire, un accès non-autorisé à l'équipement pourrait être possible. SEL décline toute responsabilité pour tout dommage résultant de cet accès non-autorisé.

DANGER: Le retrait du panneau avant expose à la circuiterie qui pourrait être la source de chocs électriques pouvant entraîner des blessures ou la mort.

DANGER: Le contact avec les bornes de l' instrument peut causer un choc électrique pouvant entraîner des blessures ou la mort.

MANUAL CHANGE INFORMATION

The date code at the bottom of each page of this manual reflects the creation or revision date. Date codes are changed only on pages that have been revised and any following pages affected by the revisions (i.e., pagination). If significant revisions are made to a section, the date code on all pages of the section will be changed to reflect the revision date.

Each time revisions are made, both the main table of contents and the affected individual section table of contents are regenerated and the date code is changed to reflect the revision date.

Changes in this manual to date are summarized below (most recent revisions listed at top).

Revision Date	Summary of Revisions
The ***Manual Change Information*** section has been created to begin a record of revisions to this manual. All changes will be recorded in this Summary of Revisions table.	
20010731	Reissued entire manual. Corrected cross-references throughout to match section name changes and reordered information. Section 1: combined with previous ***Section 3: Specifications***; changed name to ***Section 1: Introduction and Specifications***; removed information regarding manual fonts, formatting, and objective reading. Section 3: replaced and renamed to ***Section 3: Breaker Logic***, which includes ***Protection Logic*** and ***Breaker Alarm Logic*** from previous ***Section 4: Relay Logic*** and all of previous ***Section 5: Breaker Failure Applications***; reordered and edited text; added discussion of setting UBLOG, added setting ranges. Section 4: replaced and renamed to ***Section 4: Close Logic***, which retains ***Control Logic*** from previous ***Section 4: Relay Logic*** and all of previous ***Section 6: Control Relay Applications***; reordered and edited text; added a number of figures and modified others. Section 5: replaced and renamed to ***Section 5: Control Logic***, which contains all but ***Protection Logic***, ***Control Logic***, ***Event Report Trigger***, and ***Breaker Alarm Logic*** subsections from previous ***Section 4: Relay Logic.*** Section 6: moved to new ***Section 4: Close Logic***; replaced and renamed to ***Section 6: Metering and Monitoring***, which contains ***Breaker Monitor Report***, ***Breaker Resistor Thermal Report***, ***Metering Report***, ***Status Report***, and ***Relay Word Bit Report*** subsections from previous ***Section 7: Data Recording Application***; dropped the word "Report" from these subsection titles and changed subsection ***Status Report*** to ***Status Monitor***.

Revision Date	Summary of Revisions
20010731 *(continued)*	Section 7: moved all but ***Breaker Monitor Report***, ***Breaker Resistor Thermal Report***, ***Metering Report***, ***Status Report***, and ***Relay Word Bit Report*** to new ***Section 10: Event Reports and SER***, replaced and renamed to ***Section 7: Setting the Relay***, which contains previous ***Section 8: Settings***; removed ***Overview*** and added ***Introduction.*** Section 8: replaced and renamed to ***Section 8: Serial Port Communications and Commands***, which contains previous ***Section 9: Serial Port Communications***. Section 9: replaced and renamed to ***Section 9: Front-Panel Interface***, which contains previous ***Section 10: Front-Panel Interface***. Section 10: replaced and renamed to ***Section 10: Event Reports and SER***, which contains all but ***Breaker Monitor Report***, ***Breaker Resistor Thermal Report***, ***Metering Report***, ***Status Report***, and ***Relay Word Bit Report*** from previous ***Section 7: Data Recording Applications***.
20010420	Reverse of the title page: added cautions, warnings, and dangers in English and French. Section 1: made typographical corrections. Section 2: inserted updated dimension, panel-mount cutout, front- and rear-panel drawings; merged drawings and information from ***Appendix G: Optional I/O Board Specifications*** into this section; added a caution about replacing the clock battery. Section 3: updated specifications. Section 4: reordered some subsections; clarified ***Limitations of SELOGIC® Control Equations***; corrected ***Figure 4.53*** and ***Figure 4.54***. Section 6: changed two cross references from ***Appendix G: Optional I/O Board Specifications*** to ***Section 2: Installation***. Section 8: reordered tables that list the SET settings so they appear in the same order as in the ***Settings Sheets***; added 50RMS setting under **Fault Current Logic Settings** in ***Table 8.2***; added **Breaker Monitor Settings** in ***Table 8.3***; added the Distributed Network Protocol (DNP) 3.00 Level 2 Slave settings in the **SET P Settings** of the ***Settings Sheets***. Section 9: added information about DNP; made text changes throughout the section to advise the user to change default passwords to private, strong passwords at installation; updated ***Figure 9.2: Access Level Relationships***. Section 11: made typographical corrections.

Revision Date	Summary of Revisions
20010420 (*continued*)	Appendix A: added firmware that provides the DNP protocol in the SEL-352-2 Relay and makes various corrections; added firmware version that does not support DNP but makes various corrections in the SEL-352-2 Relay. Appendix B: added Help screen capture. Appendix D: added DNP information to A5C0 Relay Definition Block. Appendix E: corrected formatting error. Appendix G: • Renamed appendix ***Appendix G: Distributed Network Protocol (DNP) 3.00***. • Moved text and drawings about Optional I/O Boards Specifications to ***Section 2: Installation***. • Added text and tables explaining DNP 3.00. Quick Reference: Deleted Relay Word, Front-Panel Operation Map and Event Report Columns.
20000630	Title page: • Added U. S. Patent Number 5,041,737 to the reverse of the page. Section 1: • Updated the section, including adding a new functional diagram (page 1-10). Section 5: • Updated the section, including adding Figure 5.3 (page 5-3) and replacing previous Figures 5.5 through 5.9 with Figures 5.6 through 5.10 (pages 5-8 through 5-12). Section 7: • Made typographical corrections. • Added cautionary notes about clearing the event report buffer (page 7-16) and clearing the Sequential Events Recorder Report (page 7-18). Section 8 and Settings Sheets: • Moved Report Settings (SET R) from the end of the Settings Sheets to the beginning of the Settings Sheets and added explanatory text about setting aliases. Section 9: • Made typographical corrections. • Added note about taking care when powering down the relay after changing the date (page 9-21) or time (page 9-44). • Added note about making Sequential Events Recorder settings with care (page 9-36). Appendix A: • Reformatted the appendix and added firmware SEL-352-1-R103 and SEL-352-2-R101 which support a battery-backed clock hardware change.

Revision Date	Summary of Revisions
20000131	Corrected formatting errors in the table of contents for ***Section 7: Data Recording Applications*** and ***Section 10: Front-Panel Interface***.
20000118	Reissued entire manual to add SEL-352-2 Relay firmware option. Added model variation information to ***Section 1:Introduction***. Added panel mount figure to ***Section 2: Installation***. Added SEL-352-2 Relay information to ***Section 3: Specifications***, ***Section 5: Breaker Failure Applications, Section 7: Data Recording Applications***, ***Section 8: Settings***, ***Section 9: Serial Port Communications, Appendix E: Compressed ASCII Commands***, and ***Appendix F: Relay Word***. Added 110 Vdc level-sensitive input option to ***Section 3: Specifications*** and ***Appendix G: Optional I/O Board Specifications***.
20000104	Appendix A: • Added Firmware Version SEL-352-1-R102.
990623	Section 3: • Changed voltage in 59V Setting Range. Section 4: • Corrected **Figures 4.21** and **4.38.** • Made editorial/typographical corrections. Section 8: • Added SET T Command Settings. • Improved Settings Sheets. Appendix A: • Added Firmware Version SEL-352-1-R101.
990224	Section 2: • Updated **Figure 2.10**. • Updated information in ***Circuit Board Connections*** subsection. • Updated information in ***General Specifications*** subsection in ***Section 3: Specifications***. Appendix G: • Added **Figure G.7** and renumbered figures that followed. • Added **Figure G.18**. • Updated **Figure G.3**, **Figure G.6**, **Figure G.10**, **Figure G.13**, **Figure G.14**, and **Figure G.17**. • Added clarifying notes after **Figure G.5** and **Figure G.16**.

Revision Date	Summary of Revisions
981030	In ***Section 2: Installation*** updated ***Figure 2.1: SEL-352-1 Relay Dimensions, Panel Cutout, and Drill Plan*** and ***Figure 2.5: SEL-352-1 Connectorized™ Rear Panel (Model 03521Y)*** to document new current shorting connectors for Connectorized models. Update model numbers and correct formatting throughout manual.
980617	Update manual to include hardware changes. Model 03521J, a new 3U, one I/O board, Connectorized version has been created, employing plug-in connectors for relay power, ac analog inputs, and dc control inputs/outputs.
980102	New manual for SEL-352-1 Relay was created from last revision of SEL-352 Relay, dated 970820. The SEL-352-1 Relay will replace the SEL-352 Relay as the standard relay offering. Performance enhancements installed to create the 352-1 version are as follows: 1. Subsidence current detection logic, to shorten the dropout time of overcurrent elements. 2. Programmable Display Points and Local Bits, to improve front-panel displays and functionality. 3. Nonvolatile Latch Bits for SELOGIC control equations, to maintain bit status when relay is powered down. 4. Threshold compare capability for SELOGIC control equations, to add magnitude comparisons to the normal Boolean-like logic expressions. 5. Remote Bit control via the CON n serial port command.

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SECTION 1: INTRODUCTION AND SPECIFICATIONS

INTRODUCTION

The SEL-352 Relay is a single- or three-pole breaker failure detection, breaker control, and data recording device. Each of the protection schemes is implemented in SELOGIC® control equations, giving relay engineers unparalleled flexibility in adapting the relay to their needs. The relay provides classical overcurrent-based breaker failure protection for a wide variety of breaker arrangements. Additionally, protection is provided for circuit breaker trip and close resistors, for current through an open breaker, and for breaker flashover.

Logic to control the closing of the circuit breaker is also included. Additional features include metering, sequential events reporting, digital fault recording, remote setting capabilities, breaker operating time monitors, energy interruption monitors, and breaker resistor thermal protection. Simple hardware design and efficient digital signal processing provide reliability. Extensive self-testing and communication capabilities enhance availability.

Figure 1.1 shows a single-phase diagram of the ac connections. All nine connections are not required for most relay functions.

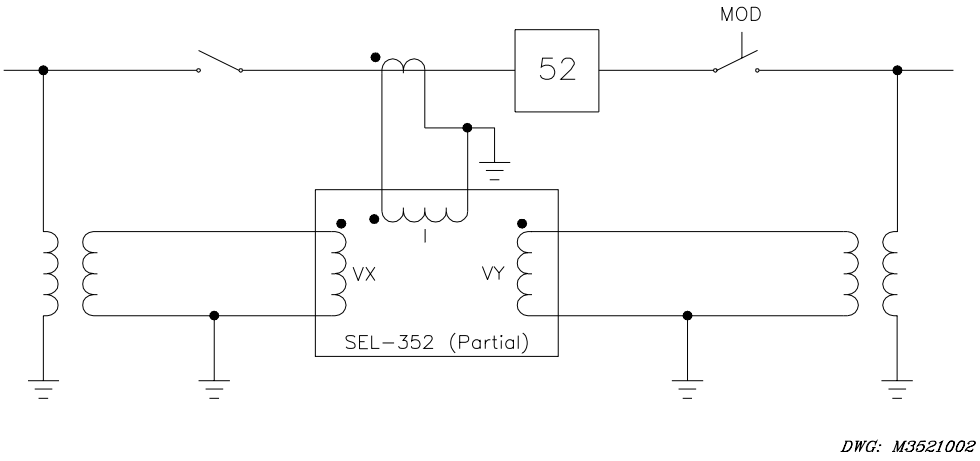


Figure 1.1: Single-Phase Diagram of AC Inputs to the Relay

INSTRUCTION MANUAL OVERVIEW

This instruction manual applies to the SEL-352 Relay. If you are unfamiliar with this relay, we suggest that you read the following sections in the outlined order.

Section 1: Introduction and Specifications for an introduction, instruction manual overview, relay functional overview, and specifications.

Section 3: Breaker Logic to learn about predefined SEL-352 Relay logic schemes that provide protection against several types of circuit breaker failure.

Section 4: Close Logic to understand use of the SEL-352 Relay in implementing automatic and manual circuit breaker closing.

Section 5: Control Logic to understand inputs, the Relay Word, outputs, and logic. Use this section to understand the settings necessary for implementing your logic.

Section 7: Setting the Relay to understand settings not described in ***Section 3*** through ***Section 6***, for default settings, and for settings sheets.

Section 8: Serial Port Communications and Commands for a description of the serial port commands used to set the relay for control, obtain target information, and obtain metering information, etc.

Section 9: Front-Panel Interface for a description of how to perform the serial port commands from the front panel.

Section 6: Metering and Monitoring to learn how to retrieve operations data such as metering, dc battery monitor, breaker monitor, and relay status.

Section 10: Event Reports and SER for a description of event report and sequential events report generation, event report formats, sequential event reports, and report interpretation.

Section 2: Installation to learn how to configure, install, and wire your relay.

Section 11: Testing and Troubleshooting for test procedures and a troubleshooting guide. You can use this section as a tutorial to check your understanding of relay operation.

RELAY FUNCTIONS

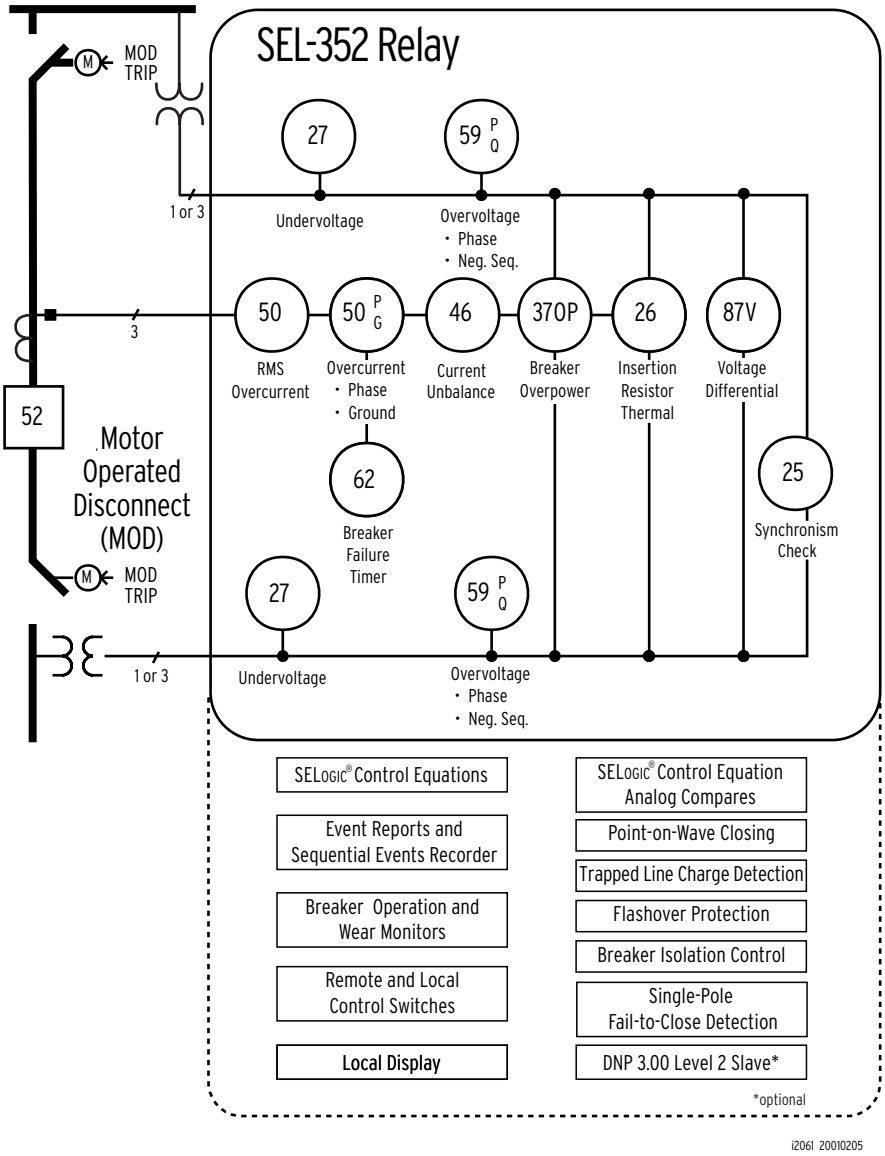


Figure 1.2: Functional Overview

Breaker Failure Detection

The SEL-352 Relay has five fault current-driven breaker failure detection schemes, including one specifically designed for ring-bus or breaker-and-a-half applications. Tailor the relay to your circuit breaker failure detection requirements by selecting the most appropriate scheme or use SELOGIC control equations to implement your own scheme.

The relay detects failures to interrupt fault, load, or line-charging current. It also detects failure of breaker poles to complete a close sequence and can detect open breaker flashover failures. If trip or close resistors remain in service after an operation, the relay detects this failure using a thermal model.

Independent phase current detectors, protection logic, and timers make the relay easy to apply on both simple systems and more complicated breaker arrangements such as single-pole trip installations.

The SEL-352 Relay stores summaries of the last 512 breaker operations in nonvolatile memory. Event type, maximum current, mechanical and electrical operating times, and breaker energy are stored along with the date and time of operation. Using this breaker history, you can monitor breaker wear and effectively schedule routine breaker maintenance.

When a motor-operated disconnect switch (MOD) is used with the protected breaker, the SEL-352 Relay can trip the MOD to isolate the failed breaker when phase current drops below a value the user can set. When an MOD is not installed, use the MOD logic to indicate a "Safe to Disconnect" condition to personnel.

The relay also includes SELOGIC control equations, which allow you to configure the programmable outputs to operate when any of the protective elements pick up. You can implement complete application-specific protective schemes with a minimum of wiring and panel space. SELOGIC control equations also simplify relay testing.

Control Features

Control logic provides flexibility for closing and tripping. For minimal breaker wear, the SEL-352 Relay can be used to close the breaker at an optimum time. Close using a simple pole-staggered close or use complete control by monitoring synchronism, trapped charge polarity, and zero crossings. Control breaker tripping through lockout and reset conditions, instantaneous retripping, and time-delayed retripping.

Use the flexible SELOGIC control equations to create your own recloser, implement manual closing supervision, and/or change existing control logic to meet your needs.

Data Recording

A wide range of user-selectable events trigger the sequential events recording (SER) and digital fault recording (DFR) functions, including any input or output assertion. Breaker Failure Trip (86BFT) output assertion automatically generates a DFR record, and you can set the relay to trigger an event for CLOSE or TRIP input assertions. This ensures a record of every normal circuit breaker operation as well as every circuit breaker failure.

The recorded data contain all information needed to determine the cause of relay and breaker operations. The data collected include current through the circuit breaker, voltage on both sides of the circuit breaker, input, output, and relay element data. Parameters such as event type, relay response time, circuit breaker operation time, currents, voltages, and breaker power dissipation appear directly in the breaker monitor report or can be calculated from the data stored. All event reports are time-tagged by a self-contained clock/calendar.

Additional Features

Additional features make the SEL-352 Relay reliable and economical. The communication functions provide remote and local examination of a wide range of data, including the voltages and currents presented to the instrument, relay settings, history of events, breaker alarms, sequential events, and self-test status data. You can enter and modify relay settings remotely; you can also control all outputs via the communications channel.

A three-level password scheme protects settings and circuit breaker control. The SEL-352 Relay monitors password execution and closes the ALARM contact output to indicate possible unauthorized access. The relay requires no special communications software. Access the relay with a dumb terminal, printing terminal, or computer with serial port and terminal emulation software.

MODEL OPTIONS

SEL-352-1 Relay

The SEL-352-1 Relay has provided sophisticated and reliable service for many years. It continues to satisfy the needs of most of our customers. However, we recommend using the SEL-352-2 Relay for new designs because of the additional features it provides.

SEL-352-2 Relay

The SEL-352-2 Relay provides the following additional features:

- Overcurrent elements for detecting RMS overcurrent conditions on a per-pole or three-phase basis (50R, 50RA, 50RB, and 50RC).
- Percent Wear function for estimating the amount of breaker contact wear per pole.
- **BREAKER W** command for preloading the number of operations, total current, total energy, and percent wear fields in the operation summary on a per-pole basis.
- Optional Distributed Network Protocol (DNP) 3.00 Level 2 Slave communications protocol.

Conventional Terminal Blocks

This model includes hardware that supports three current inputs, six voltage inputs, six optoisolated inputs, seven programmable output contacts, one alarm contact, three EIA-232 ports, one EIA-485 port, and IRIG-B time code. It uses terminal blocks that support #6 ring terminals. This robust package meets or exceeds numerous industry standard type tests.

This relay is available in a 3.50" (2U), 5.25" (3U), or 7.00" (4U) rack-mount package or 4.9", 6.65", or 8.40" panel-mount package. Additional optoisolated inputs and programmable output contacts are available with the larger packages.

Plug-In Connectors (Connectorized®)

This model includes hardware that supports all of the features of the conventional terminal blocks model. It differs in that it uses plug-in connectors instead of terminal blocks. In addition, it provides

- Quick connect/release hardware for rear-panel terminals.
- Level-sensitive optoisolated inputs.

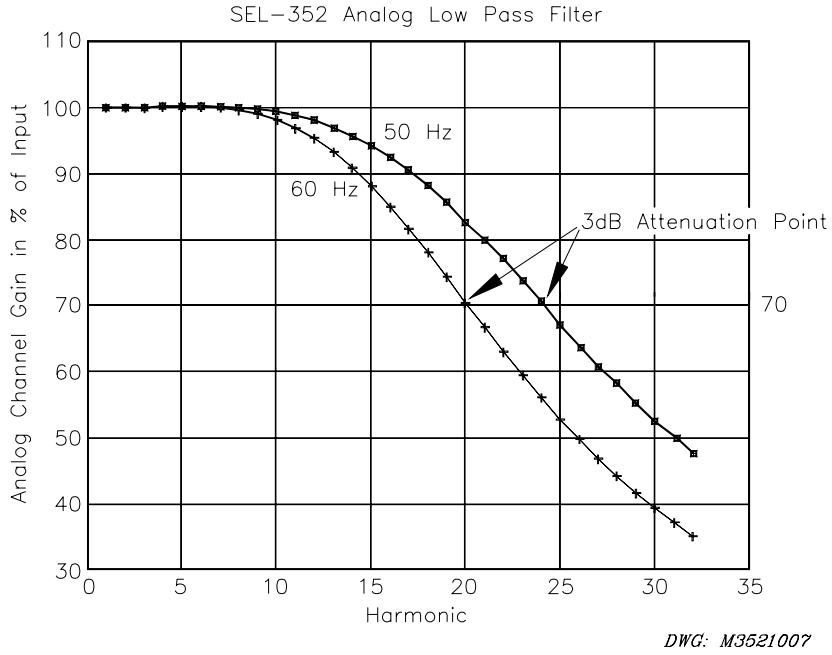
This robust package meets or exceeds numerous industry standard type tests. It is available in a 5.25" (3U) rack-mount package or a 4.9" panel-mount package.

Interface Boards

For more information about available interface boards, see ***Section 2: Installation***.

SIGNAL PROCESSING SPECIFICATIONS

Analog Data Acquisition: –3dB cutoff at 1200 Hz, 64 samples per cycle, see Figure 1.3.



Harmonic	Correction Factor (60 Hz)	Correction Factor (50 Hz)
Fundamental through 8th	1	1
9th	1.01	1
10th	1.02	1.01
11th	1.03	1.01
12th	1.05	1.02
13th	1.07	1.03
14th	1.10	1.04
15th	1.14	1.06
16th	1.18	1.08
17th	1.23	1.11
18th	1.28	1.14
19th	1.35	1.17

Harmonic	Correction Factor (60 Hz)	Correction Factor (50 Hz)
20th	1.42	1.21
21st	1.50	1.25
22nd	1.59	1.30
23rd	1.68	1.36
24th	1.78	1.42
25th	1.89	1.48
26th	2.01	1.56
27th	2.14	1.63
28th	2.27	1.72
29th	2.40	1.80
30th	2.55	1.89
31st	2.70	1.99
32nd	2.86	2.09

Relay Measurement • Correction Factor = Input Signal Level

Figure 1.3: Analog Filter Curve

Digital Filtering: Half-cosine filter for the 50FT overcurrent element.
Cosine filter for all other elements.

Processing Intervals:

1/8-cycle:
- Event Report Triggers
- Targets
- Optoisolated Inputs
- Local Bits
- Remote Bits
- SELOGIC Control Equation SET A Elements
- Fault Current Protection Elements
- 86BF Trip and Reset Elements
- Contact Output Elements
- SELOGIC Control Equation Analog Compares

1/4-cycle: All other elements

GENERAL SPECIFICATIONS

Tightening Torque:

Terminal Block:
Minimum: 7-in-lb (0.8 Nm)
Maximum: 12-in-lb (1.4 Nm)

Connectorized:
Minimum: 4.4-in-lb (0.5 Nm)
Maximum: 8.8-in-lb (1.0 Nm)

Terminal Connections: Terminals or stranded copper wire. Ring terminals are recommended. Minimum temperature rating of 105°C.

AC Current Inputs: 5 A nominal: 15 A continuous, 500 A for 1 s, linear to 100 A symmetrical.
1250 A for 1 cycle.
Burden: 0.27 VA at 5 A, 2.51 VA at 15 A.

1 A nominal: 3 A continuous, 100 A for 1 s, linear to 20 A symmetrical,
250 A for 1 cycle.
Burden: 0.13 VA at 1 A, 1.31 VA at 3 A.

AC Voltage Inputs: 120 V_{L-N}, three-phase, four-wire connection.
150 V_{L-N} continuous (connect any voltage up to 150 Vac).
365 Vac for 10 s.
Burden: 0.13 VA @ 67 V; 0.45 VA @ 120 V.

Power Supply:

Rated: 125/250 Vdc or Vac
- Range: 85–350 Vdc or 85–264 Vac
- Burden: <25 W
- Interruption: 30 ms at 125 Vdc
- Ripple: 100%

Rated: 24/48 Vdc
- Range: 20–60 Vdc polarity dependent
- Burden: <25 W
- Interruption: 30 ms at 48 Vdc
- Ripple: 5%

Note: Interruption and Ripple per IEC 60255-11 [IEC 255-11]: 1979.

Output Contacts: Standard:

Make: 30 A; Carry: 6 A continuous carry at 70°C, 4 A continuous carry at 85°C;
1 second rating: 50 A; MOV protected: 270 Vac, 360 Vdc, 40 J;
Pickup time: Less than 5 ms; Dropout time: Less than 5 ms, typical.
Breaking Capacity (10000 operations):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

Cyclic Capacity (2.5 cycles/second):

24 V	0.75 A	L/R = 40 ms
48 V	0.50 A	L/R = 40 ms
125 V	0.30 A	L/R = 40 ms
250 V	0.20 A	L/R = 40 ms

High Current Interrupting Option:

Make: 30 A; Carry: 6 A continuous carry at 70°C, 4 A continuous carry at 85°C;
1 second rating: 50 A; MOV protected: 330 Vdc, 40 J;
Pickup time: Less than 5 ms; Dropout time: Less than 8 ms, typical.
Breaking Capacity (10000 operations):

24 V	10 A	L/R = 40 ms
48 V	10 A	L/R = 40 ms
125 V	10 A	L/R = 40 ms
250 V	10 A	L/R = 20 ms

Cyclic Capacity (4 cycles in 1 second, followed by 2 minutes idle for thermal dissipation):

24 V	10 A	L/R = 40 ms
48 V	10 A	L/R = 40 ms
125 V	10 A	L/R = 40 ms
250 V	10 A	L/R = 20 ms

Note: Do not use high current interrupting output contacts to switch ac control signals. These outputs are polarity dependent.

Fast High Current Interrupting Option:

Make: 30 A; Carry: 6 A continuous carry at 70°C, 4 A continuous carry at 85°C;
1 second rating: 50 A; MOV protected: 330 Vdc, 40 J;
Pickup time: Less than 200 µs; Dropout time: Less than 8 ms, typical.
Breaking Capacity (10000 operations):

24 V	10 A	L/R = 40 ms
48 V	10 A	L/R = 40 ms
125 V	10 A	L/R = 40 ms
250 V	10 A	L/R = 20 ms

Cyclic Capacity (4 cycles in 1 second, followed by 2 minutes idle for thermal dissipation):

24 V	10 A	L/R = 40 ms
48 V	10 A	L/R = 40 ms
125 V	10 A	L/R = 40 ms
250 V	10 A	L/R = 20 ms

Note: Fast High Current Interrupting Option output contacts **are not** polarity dependent.

Note: Make per IEEE C37.90: 1989; Breaking and Cyclic Capacity per IEC 60255-23 [IEC 255-23]: 1994.

Optoisolated Inputs:

250 Vdc:	Pickup	200	–	300 Vdc; Dropout	150 Vdc.
125 Vdc:	Pickup	105	–	150 Vdc; Dropout	75 Vdc.
110 Vdc:	Pickup	88	–	132 Vdc; Dropout	66 Vdc.
48 Vdc:	Pickup	38.4	–	60 Vdc; Dropout	28.8 Vdc.
24 Vdc:	Pickup	15.0	–	30 Vdc.	

Note: 24, 48, 125 Vdc optoisolated inputs draw approximately 4 mA of current, 110 Vdc inputs draw approximately 8 mA of current, and 250 Vdc inputs draw approximately 5 mA of current. All current ratings are at nominal input voltage.

Routine Dielectric Strength: AC current and voltage inputs: 2500 Vac for 10 s; Power supply, optoisolated inputs, and output contacts: 3100 Vdc for 10 s.

Frequency and Rotation: System Frequency: 50 or 60 Hz; Phase Rotation: ABC or ACB.

Frequency Tracking: NFREQ = 60: Tracking range is 55–63 Hz
NFREQ = 50: Tracking range is 45–55 Hz

Communications Ports: EIA-232: 1 front and 2 rear; EIA-485: 1 rear, 2100 Vdc isolation; Baud rate: 300–19200 baud.

Time-Code Input: Relay accepts demodulated IRIG-B time-code input at Port 1 or 2. Relay is time synchronized to within ±5 ms of time source input.

Operating Temp.: –40° to +85°C (–40° to +185°F).

Weight: 2U rack unit height: 15 lbs (6.8 kg); 3U rack unit height: 17.75 lbs (8 kg).

Type Tests:

*Generic Emissions, Heavy Industrial:	EN 50081-2: 1993, Class A
*Generic Immunity, Heavy Industrial:	EN 50082-2: 1995
*Radiated and Conducted Emissions:	EN 55011: 1998, Class A
*Conducted Radio Frequency:	EN 61000-4-6: 1996, ENV 50141: 1993, 10 Vrms
Radiated Radio Frequency (900 MHz with modulation):	ENV 50204: 1995, 10 V/m
Cold:	IEC 60068-2-1 [IEC 68-2-1]: 1990, EN 60068-2-1: 1993, Test Ad, 16 hours at –40ºC
Dry Heat:	IEC 60068-2-2 [IEC 68-2-2]: 1974, EN 60068-2-2: 1993, Test Bd, 16 hours at +85ºC
Damp Heat, Cyclic:	IEC 60068-2-30 [IEC 68-2-30]: 1980, Test Db, 25º to 55ºC, 6 cycles, 95% humidity
Damp Heat, Steady State:	IEC 60068-2-3 [IEC 68-2-3]: 1990, Test C
Dielectric Strength:	IEC 60255-5 [IEC 255-5]: 1977 and IEEE C37.90: 1989, 2500 Vac on analogs, contact inputs, and contact outputs; 3100 Vdc on power supply; 2200 Vdc on EIA-485 communications port
Impulse:	IEC 60255-5 [IEC 255-5]: 1977, 0.5 J, 5000 V
Vibration:	IEC 60255-21-1 [IEC 255-21-1]: 1988, Class 1
Shock and Bump:	IEC 60255-21-2 [IEC 255-21-2]: 1988, Class 1
Seismic:	IEC 60255-21-3 [IEC 255-21-3]: 1993, Class 2
1 MHz Burst Disturbance:	IEC 60255-22-1 [IEC 255-22-1]: 1988, Class 3
Electrostatic Discharge:	IEC 60255-22-2 [IEC 255-22-2]: 1996, IEC 61000-4-2 [IEC 1000-4-2]: 1995, Level 4
Radiated Radio Frequency:	IEC 60255-22-3 [IEC 255-22-3]: 1989, ENV 50140: 1993, IEEE C37.90.2: 1995, 35 V/m
Fast Transient Disturbance:	IEC 60255-22-4 [IEC 255-22-4]: 1992, IEC 61000-4-4 [IEC 1000-4-4]: 1995 Level 4
Object Penetration:	IEC 60529 [IEC 529]: 1989, IP 30, IP54 from the front panel using the SEL-9103 front cover dust and splash protection (type test)
Surge Withstand Capability:	IEEE C37.90.1: 1989, 3000 V oscillatory, 5000 V fast transient

Note: * = Terminal Block version only.

Certifications: ISO: Relay is designed and manufactured using ISO-9001 certified quality program.

Processing Specifications: 64 samples per power system cycle.

RELAY ELEMENT SPECIFICATIONS

Overcurrent Elements

50FT — Fault Current Element with Subsidence Current Logic
setting ranges .....0.50–45.00 A secondary, 0.01-A steps (I_{nom} = 5 A)
.....0.10–9.00 A secondary, 0.01-A steps (I_{nom} = 1 A)
pickup time..... less than 0.55 cycle at 2 multiples of pickup
dropout time .....less than 0.75 cycle
pickup and dropout.....±0.025 A secondary ±5% of setting
transient overreach ..... ±14% of setting

50MD/50LD — MOD and Load/Line Current Elements
setting ranges .....0.10–45.00 A secondary, 0.01-A steps (I_{nom} = 5 A)
.....0.02–9.00 A secondary, 0.01-A steps (I_{nom} = 1 A)
pickup time..... less than 0.9 cycle at 2 multiples of pickup
dropout time ..... less than 1.35 cycles
pickup and dropout.....±0.025 A secondary ±5% of setting
transient overreach ..... ±5% of setting

50MN — Minimum Current Element
current threshold (fixed)..... 0.10 A secondary (I_{nom} = 5 A)
..... 0.02 A secondary (I_{nom} = 1 A)
pickup time..... less than 0.9 cycle at 2 multiples of pickup
dropout time ..... less than 1.35 cycles
pickup and dropout.....±0.03 A secondary
transient overreach ..... ±5% of setting

50N — Ground Overcurrent Element
setting ranges .....0.10–45.00 A secondary, 0.01-A steps (I_{nom} = 5 A)
.....0.02–9.00 A secondary, 0.01-A steps (I_{nom} = 1 A)
pickup time..... less than 0.9 cycle at 2 multiples of pickup
dropout time ..... less than 1.35 cycles
pickup and dropout.....±0.025 A secondary ±5% of setting
transient overreach ..... ±5% of setting

50RMS — RMS Overcurrent Element..... (Only available in the SEL-352-2 Relay)
setting ranges .....0.50–45.00 A secondary, 0.10-A steps (I_{nom} = 5 A)
.....0.10–9.00 A secondary, 0.02-A steps (I_{nom} = 1 A)
pickup time..... less than 0.9 cycle at 2 multiples of pickup
dropout time ..... less than 1.125 cycles
pickup and dropout.....$\pm 0.01 \cdot I_{nom}$ A secondary ±5% of setting
transient overreach ..... ±5% of setting

Pickup/Dropout Curves

Figure 1.4 through Figure 1.7 are based on actual test data at room temperature using various settings. Relay element specifications given previously in this section include the entire temperature range of the relay. Output contact times are not included.

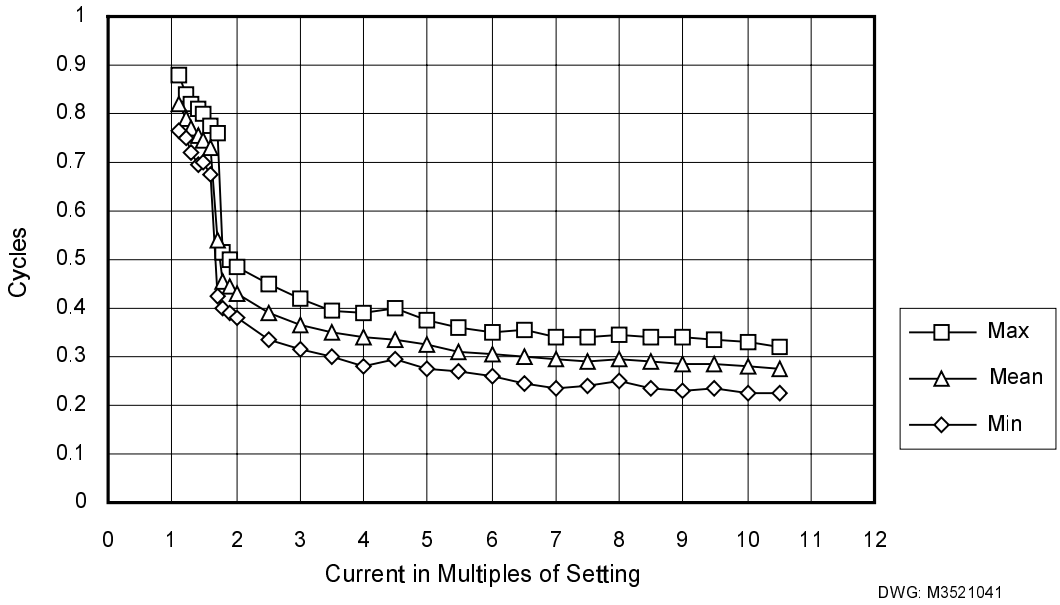


Figure 1.4: 50FT Pickup Curves

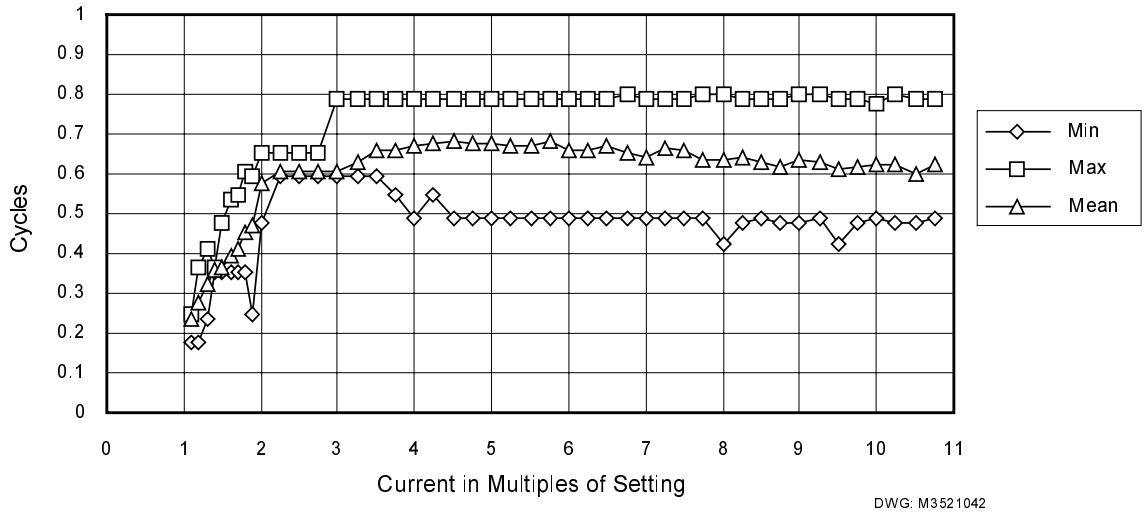


Figure 1.5: 50FT Dropout Curves

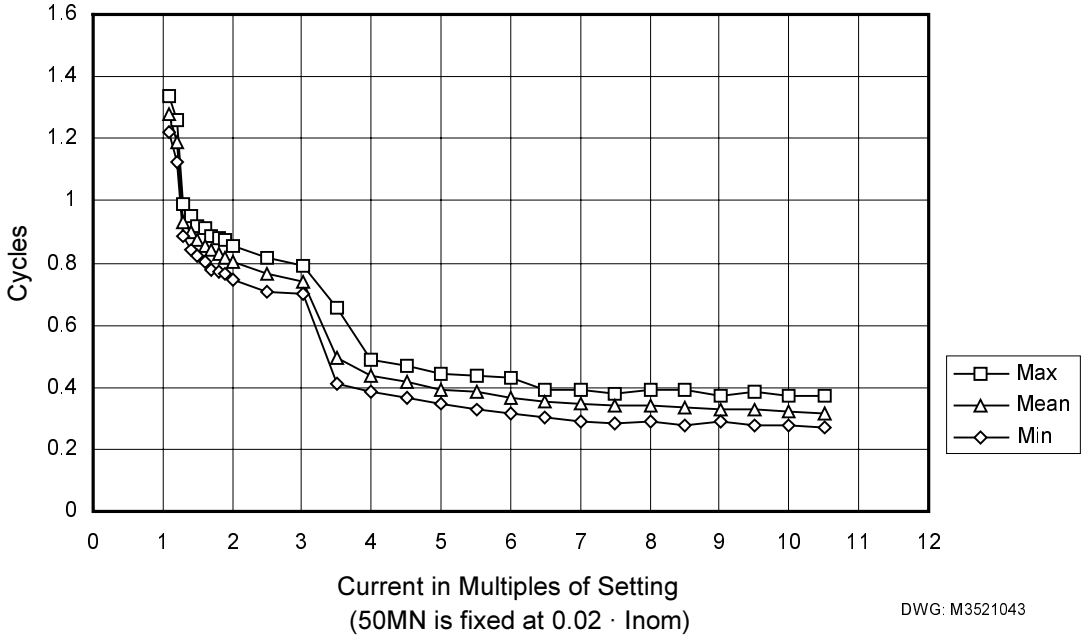


Figure 1.6: 50MN, 50LD, 50MD, 50N Pickup Curves

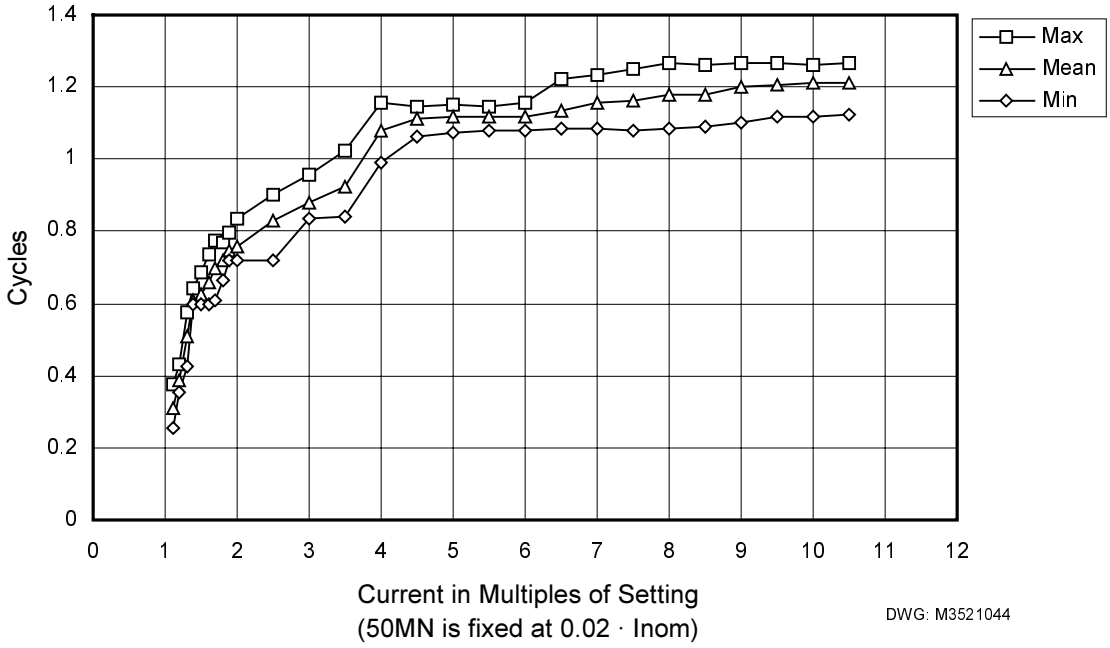


Figure 1.7: 50MN, 50LD, 50MD, 50N Dropout Curves

Voltage Elements

87H/87FO/87TH Voltage Across Breaker Overvoltage Elements
- setting range ..... 1.0–150.0 V secondary, 0.1-V steps
- pickup time ..... less than 1.35 cycles
- dropout time ..... less than 1.55 cycles
- pickup and dropout ..... ±0.09 V secondary ±5% of setting
- transient overreach ..... ±5% of setting

X47Q/Y47Q Negative-Sequence Overvoltage Element
- setting range ..... 2.0–140.0 V secondary, 0.1-V steps
- pickup time ..... less than 1.35 cycles
- dropout time ..... less than 1.55 cycles
- pickup and dropout ..... ±0.27 V secondary ±6% of setting
- transient overreach ..... ±5% of setting

X59H High-Set Overvoltage Element
- setting range ..... 1.0–130.0 V secondary, 0.1-V steps
- pickup time ..... less than 1.35 cycles
- dropout time ..... less than 1.55 cycles
- pickup and dropout ..... ±0.09 V secondary ±5% of setting
- transient overreach ..... ±5% of setting

X27D/Y27D Dead Line Undervoltage Element
- setting range ..... 1.0–120.0 V secondary, 0.1-V steps
- pickup time ..... less than 1.35 cycles
- dropout time ..... less than 1.55 cycles
- pickup and dropout ..... ±0.09 V secondary ±5% of setting
- transient overreach ..... ±5% of setting

X59L/Y59L Live Line Overvoltage Element
- setting range ..... 10.0–120.0 V secondary, 0.1-V steps
- pickup time ..... less than 1.35 cycles
- dropout time ..... less than 1.55 cycles
- pickup and dropout ..... ±0.09 V secondary ±5% of setting
- transient overreach ..... ±5% of setting

Synchronism Check Element

25SC/25SM Maximum Slip Frequency for Controlled/Manual Close
- setting range ..... 0.005–0.500 Hz, 0.001-Hz steps
- pickup and dropout ..... ±0.002 Hz ±2% of setting

25AC Maximum Controlled Close Angle
- setting range ..... 32·(25SC) to 90°, min = 1°, 0.1° steps
- pickup and dropout ..... ±0.5° ±5% of setting

25AM Maximum Manual Close Angle
- setting range ..... 32·(25SM) to 90°, min = 1°, 0.1° steps
- pickup and dropout ..... ±0.5° ±5% of setting

Current Unbalance Element

46P — Phase Current Unbalance Element

46P detects phase discordance when the protected breaker closes. For example, A-phase is unbalanced if phase current is above the 50LD setting in one or more phases and:

|IA| < (|IA| + |IB| + |IC|) / 46UB setting where 46UB setting = 8, 16, 32, or 64.
Time to stabilize measurement
due to transient conditions ..... less than 1.35 cycles

Overpower Elements

37OP — Breaker Overpower Element
setting range ..... 0.10–3400.00 W secondary, 0.01-W steps (I_{nom} = 5 A)
..... 0.02–680.00 W secondary, 0.01-W steps (I_{nom} = 1 A)
pickup time ..... less than 2.10 cycles
dropout time ..... less than 3.00 cycles
maximum element error, secondary units:
±2.25 mW ±10.25% (measured input power)
±2.63% (measured voltage) ±9.45% (measured current)

Breaker Resistor Thermal Elements

26CF — Close Resistor Failure Element
26CP — Close Resistor Pending Failure Element
26TF — Trip Resistor Failure Element
26TP — Trip Resistor Pending Failure Element
setting range ..... 0.010–1000.000 Joules secondary, 0.001 J-steps (I_{nom} = 5 A)
..... 0.002–200.000 Joules secondary, 0.001 J-steps (I_{nom} = 1 A)
pickup error is based on 37OP element over time

Settable Timers

SYNCT — Synchronizing Time Dropout (SYNCdo)
setting range ..... 0.00–99999.00 cycles, 1/4-cycle steps
pickup setting ..... ±0.25 cycles or ±0.25% of setting

62TT — Failure-to-Trip Fault Current Trip Input Timer
62FC — Failure-to-Trip Fault Current Failure Timer
62T1 — General Purpose Timer 1
62M2 — Maximum Bus Clearing Time
62M3 — Maximum MOD Operate Time
setting range ..... 0.0–8191.0 cycles, 1/8-cycle steps
pickup setting ..... ±0.125 cycles or ±0.25% of setting

SCT — Synchronous Close Timer (CLSdo)
62LD — Failure-to-Trip Load Current Failure Timer
62LP — Failure-to-Trip Load Current Pending Failure Timer
62AF — Failure of Breaker 52A Contact to Indicate Operation Failure Timer
62AP — Failure of Breaker 52A Contact to Indicate Operation Pending Failure Timer
62FF — Flashover Failure Timer
62FP — Flashover Pending Failure Timer
62UC — Phase Discordance Close Input Pickup Timer
62OP — Trip and Close Resistor Heating Pickup Timer

62L2	Loss-of-Dielectric Timer
62UF	Phase Discordance Failure Timer
62UP	Phase Discordance Pending Failure Timer
62T3	General Purpose Timer 3
62T4	General Purpose Timer 4
62RT	Delayed Trip Time
62RC	Staggered Close Time
	setting range ..... 0.00–16383.00 cycles, 1/4-cycle steps
	pickup setting ..... ±0.25 cycles or ±0.25% of setting
62ZCA	A-Phase Zero-Crossing Timer
62ZCB	B-Phase Zero-Crossing Timer
62ZCC	C-Phase Zero-Crossing Timer
62PCA	A-Phase Peak-Crossing Timer
62PCB	B-Phase Peak-Crossing Timer
62PCC	C-Phase Peak-Crossing Timer
	setting range ..... 0.00–40.00 ms, 0.01-ms steps
	pickup setting ..... ±200 µsec
62VN	Voltage Nulling Delay Timer
	setting range ..... 0.00–240.00 minutes, 0.01-min steps
	pickup setting ..... ±0.25 cycles or ±0.25% of setting

Fixed Timers

62F1	Flashover Voltage Time Delayed Dropout Timer	5 cycles ±0.25 cycles
62F2	Load Current Pickup Timer (Flashover Logic)	5 cycles ±0.25 cycles
62F3	Trip or Close Dropout Timer (Flashover Logic)	6 cycles ±0.25 cycles
62M1	86BF Reset Signal Duration Timer	60 cycles ±0.125 cycles
62M4	86BF Reset Time Delay, MOD Logic Enabled	300 cycles ±0.125 cycles
62LT1	Loss-of-Dielectric Input Debounce Timer	60 cycles ±0.25 cycles
62LT3	Loss-of-Dielectric Input Debounce Timer	60 cycles ±0.25 cycles
MCT	Manual Close Input Dropout Timer	2 cycles ±0.25 cycles
SEN	Synchronism Calculation Enable Pickup Timer	15 cycles ±0.25 cycles
SS	Slip Security Pickup Timer	4.5 cycles ±0.25 cycles

Internal Logic Timers

62XZPB	B-Phase Positive Zero-Crossing Delay Timer for X Side	0.33 cycles
62XZNB	B-Phase Negative Zero-Crossing Delay Timer for X Side	0.33 cycles
62XZPC	C-Phase Positive Zero-Crossing Delay Timer for X Side	0.66 cycles
62XZNC	C-Phase Negative Zero-Crossing Delay Timer for X Side	0.66 cycles
62YZPB	B-Phase Positive Zero-Crossing Delay Timer for Y Side	0.33 cycles
62YZNB	B-Phase Negative Zero-Crossing Delay Timer for Y Side	0.33 cycles
62YZPC	C-Phase Positive Zero-Crossing Delay Timer for Y Side	0.66 cycles
62YZNC	C-Phase Negative Zero-Crossing Delay Timer for Y Side	0.66 cycles
62T	Trapped Charge Trip Input Dropout Timer	4 cycles
62V	Trapped Charge Voltage Dropout Timer	7 cycles
TCDpu	Trapped Charge Detection Pickup Timer	1 cycle
TCDdo	Trapped Charge Detection Dropout Timer	12 cycles
62BALRM	Breaker Alarm Dropout Timer	60 cycles
62OI	Operation Input Dropout Timer for Breaker Alarms	5 cycles
62BDNC	BDNC Breaker Alarm Close Inputs Pickup Timer	3 seconds
62TWO	Trip Input Dropout Debounce Timer	0.25 cycles

Metering

VAX	A-Phase Voltage for the X-Side ac inputs
VBX	B-Phase Voltage for the X-Side ac inputs
VCX	C-Phase Voltage for the X-Side ac inputs
VAY	A-Phase Voltage for the Y-Side ac inputs
VBY	B-Phase Voltage for the Y-Side ac inputs
VCY	C-Phase Voltage for the Y-Side ac inputs
	Units ..... kilovolts (kV) primary
	Accuracy ..... ±0.67 V secondary
IA	A-Phase current ac input
IB	B-Phase current ac input
IC	C-Phase current ac input
	Units ..... Amps (A) primary
	Accuracy ..... ±0.05 A secondary (I_{nom} = 5 A)
	..... ±0.01 A secondary (I_{nom} = 1 A)

Multiple Setting Groups

SS1	Setting group selection input 1
SS2	Setting group selection input 2
	Number of setting groups 3
	Setting group change delay ..... TGR setting and up to 3 seconds uncertainty

DATA RECORDING SPECIFICATIONS

Event Records

MER	Event Report Trigger
	pickup accuracy ..... 0.000 to 0.125 cycles
	number of events ..... 600 ÷ LER setting (15, 30, or 60 cycles)
SER1	Sequential-Event-Recorder Trigger List 1
SER2	Sequential-Event-Recorder Trigger List 2
SER3	Sequential-Event-Recorder Trigger List 3
	pickup accuracy ..... 0.000 to 0.125 cycles
	number of trigger elements ..... 24 per list, 72 total
	number of events displayed 512

Breaker Monitor Reporting

	electrical operate time units ..... ms
	mechanical operate time units ..... ms
	energy units ..... MJ, primary
	current units ..... A, primary
	breaker contact wear (SEL-352-2 Relay only) ..... %
	number of operations displayed 512
	other relay elements determine accuracy

SERIAL PORT SPECIFICATIONS

Port 1	EIA-485 with IRIG-B input
Port 2	EIA-232 with IRIG-B input and +5 Vdc output. Maximum total current draw on +5 Vdc supply through serial ports is 1 A.
Port 3	EIA-232 with +5 Vdc output
Port 4	EIA-232

TABLE OF CONTENTS

SECTION 2: INSTALLATION 2-1

TABLES

FIGURES

SECTION 2: INSTALLATION

Design your installation using the mounting and connection information in this section. Options include rack or panel mounting and terminal block or plug-in connector (Connectorized®) wiring. This section also includes information on configuring the relay for your application.

RELAY MOUNTING

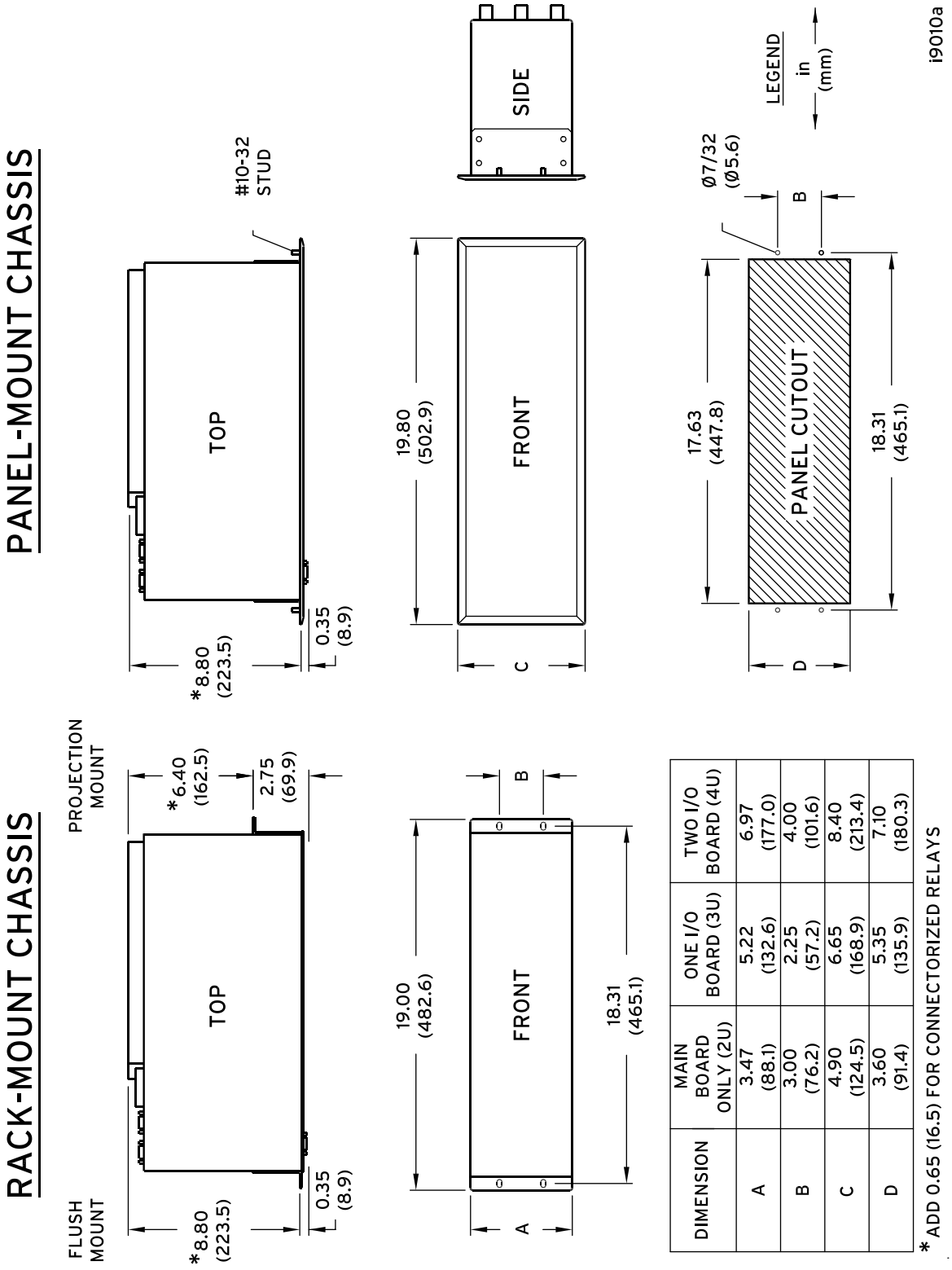
Rack Mount

We offer the SEL-352 Relay in a rack-mount version that bolts easily into a standard 19-inch rack. See Figure 2.2 and Figure 2.3. From the front of the relay, insert four bolts (two on each side) through the holes on the relay mounting flanges, and use nuts to secure the relay to the rack. See Figure 2.1.

Panel Mount

We also offer the SEL-352 Relay in a panel-mount version for a clean look. Panel-mount relays have sculpted front-panel molding that covers all installation holes. See Figure 2.4 and Figure 2.5. Cut your panel and drill mounting holes according to the dimensions in Figure 2.1. Insert the relay into the cutout, aligning four relay mounting studs on the rear of the relay with the drilled holes in your panel, and use nuts to secure the relay to the panel.

Dimensions and Cutout



DIMENSION	MAIN BOARD ONLY (2U)	ONE I/O BOARD (3U)	TWO I/O BOARD (4U)
A	3.47 (88.1)	5.22 (132.6)	6.97 (177.0)
B	3.00 (76.2)	2.25 (57.2)	4.00 (101.6)
C	4.90 (124.5)	6.65 (168.9)	8.40 (213.4)
D	3.60 (91.4)	5.35 (135.9)	7.10 (180.3)

Figure 2.1: Dimension Drawing and Panel-Mount Cutout

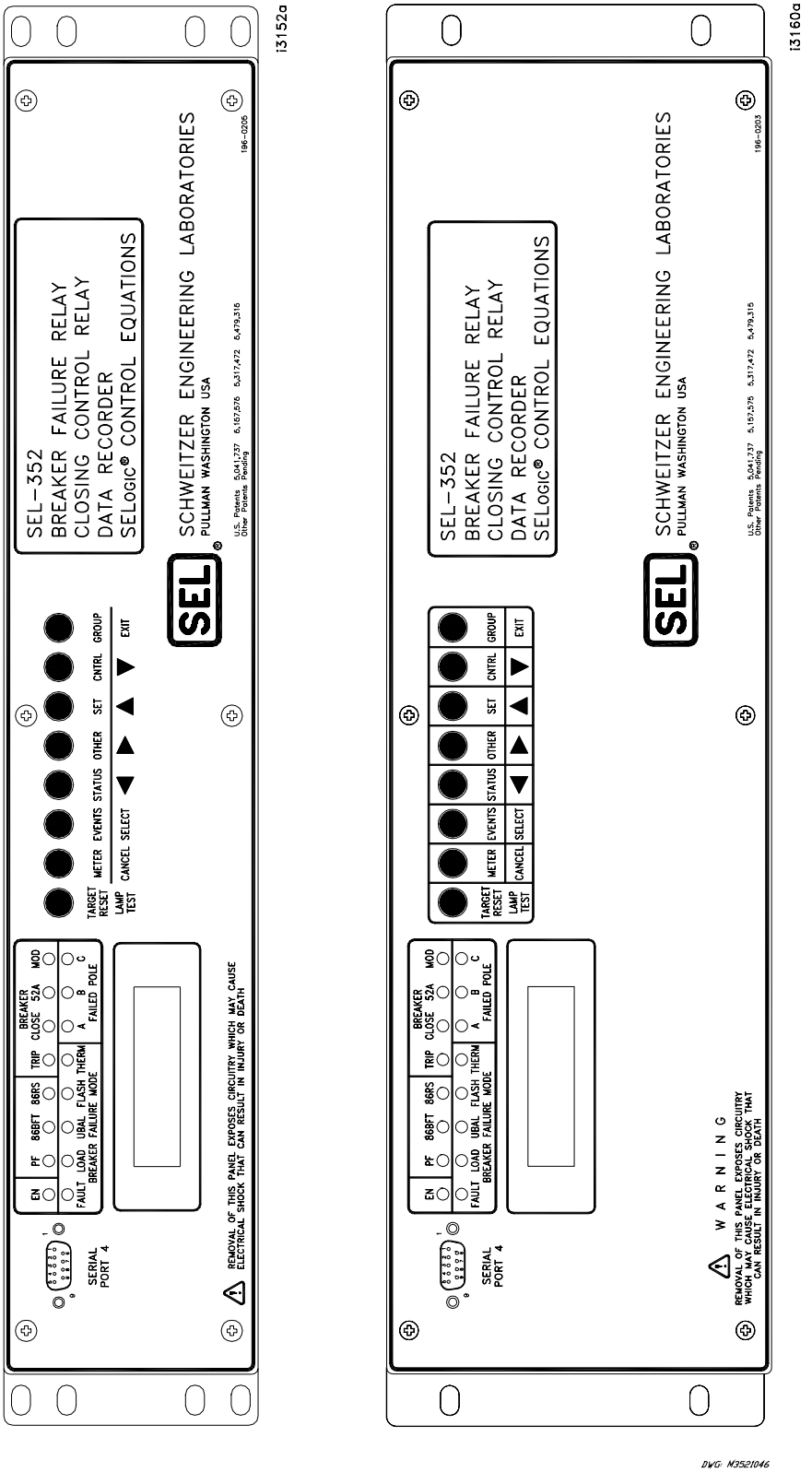


Figure 2.2: Front-Panel Drawings–Models 0352x0xxxH and 0352x1xxxH

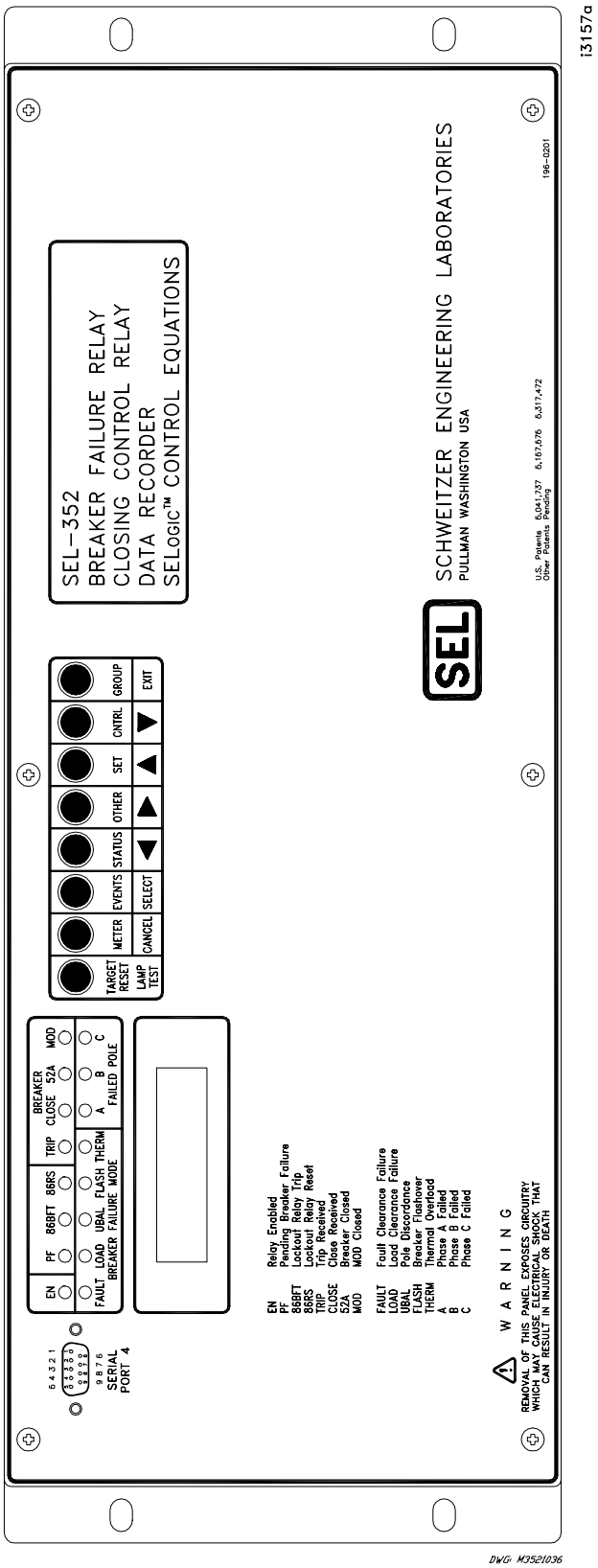


Figure 2.3: Front-Panel Drawing–Model 0352x2xxxH

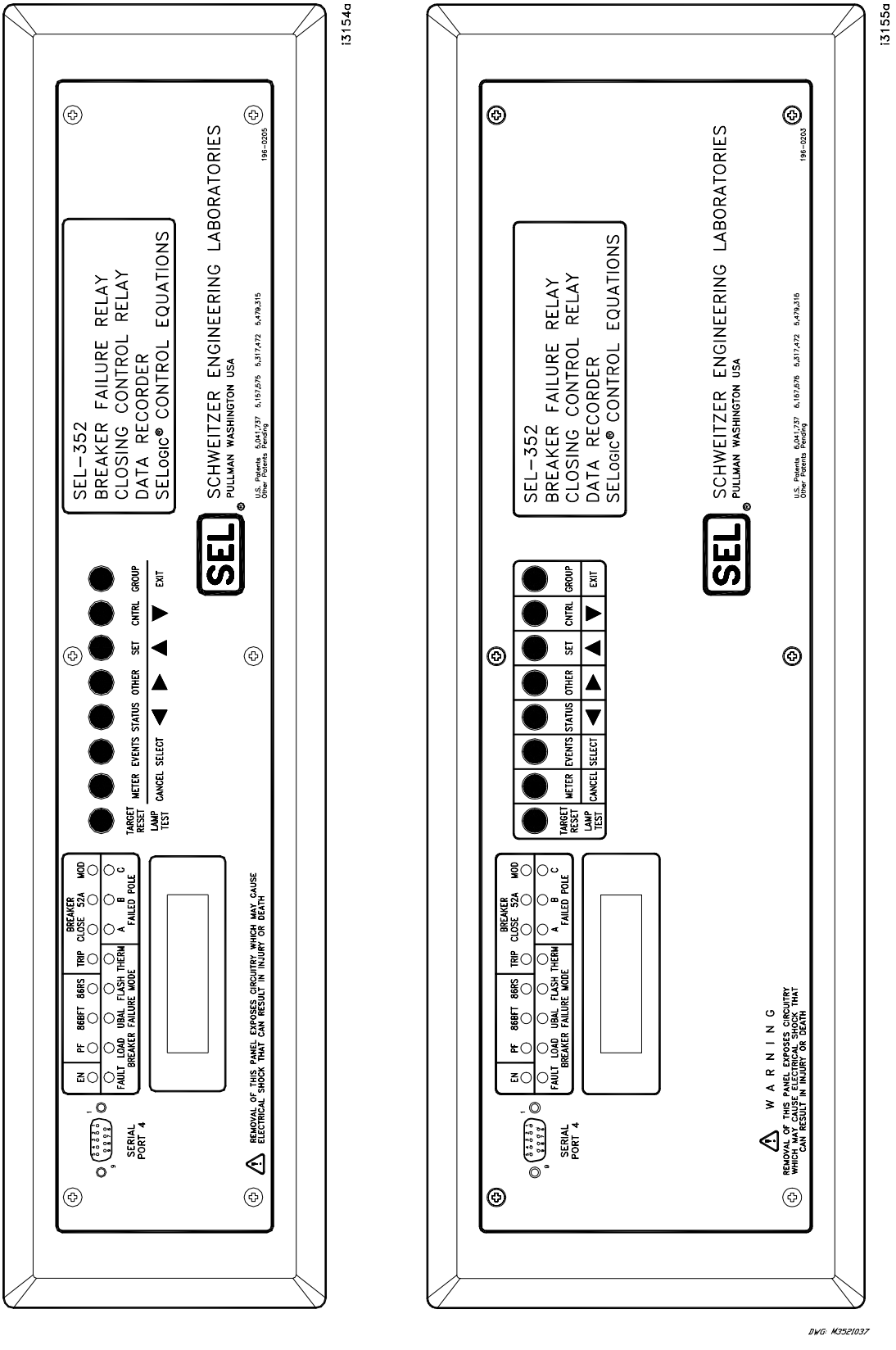


Figure 2.4: Front-Panel Drawings–Models 0352x0xxx3 and 0352x1xxx3

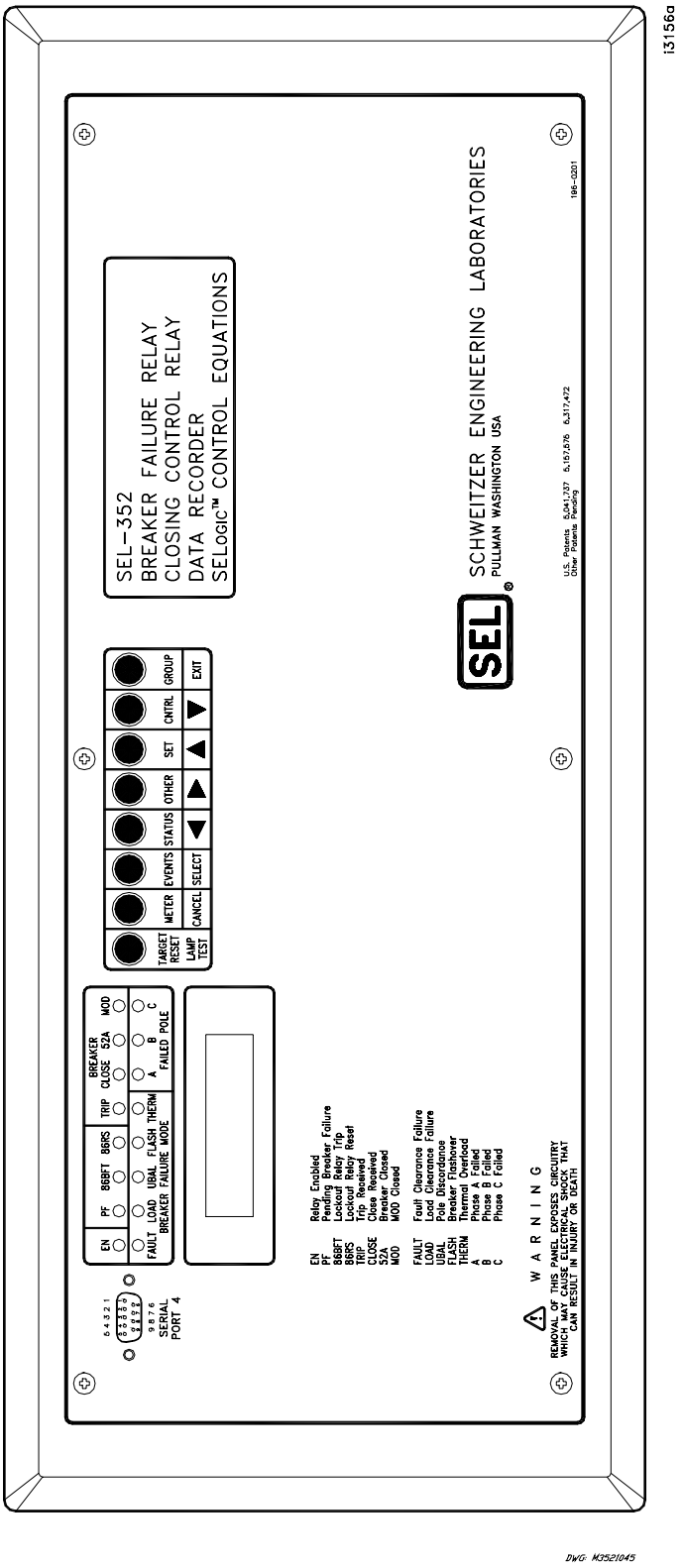


Figure 2.5: Front-Panel Drawing–Model 0352x2xxx3

REAR-PANEL CONNECTIONS

We provide two options for secure connection of wiring to the relay rear panel. One of these is the conventional terminal block, in which you use size #6–32 screws to secure rear-panel wiring. The other option uses plug-in (Connectorized) connections that offer robust connections while minimizing installation and replacement time.

Connectorized rear-panel connections reduce repair time dramatically in the unlikely event that a relay should fail. These connections greatly simplify routine bench testing; connecting and disconnecting rear-panel wiring takes only a few minutes.

Connectorized relays use a current shorting connector for current inputs, a plug-in terminal block that provides maximum wiring flexibility for inputs and outputs, and a quick disconnect voltage-rated connector for voltage inputs. The manufacturers of these connectors have tested them thoroughly, and many industry applications have proven the performance of these connectors. In addition, we have tested these connectors thoroughly to be certain that they conform to our standards for protective relay applications.

Terminal Block

Make terminal block connections with size #6–32 screws using a Phillips or slotted screwdriver. You may request locking screws from the factory. Figure 2.6 and Figure 2.7 are examples of relays with rear-terminal connections. Refer to the figures at the end of this section to make all terminal block connections.

Connectorized

To use the Connectorized version of the SEL-352 Relay, ask your SEL sales or customer service representative for the appropriate model option table and order wiring harness kit WA03520YxxxA, where x designates wire sizes and length. You can find the model option table on the SEL website at http://www.selinc.com. Refer to Figure 2.8 to make all Connectorized connections.

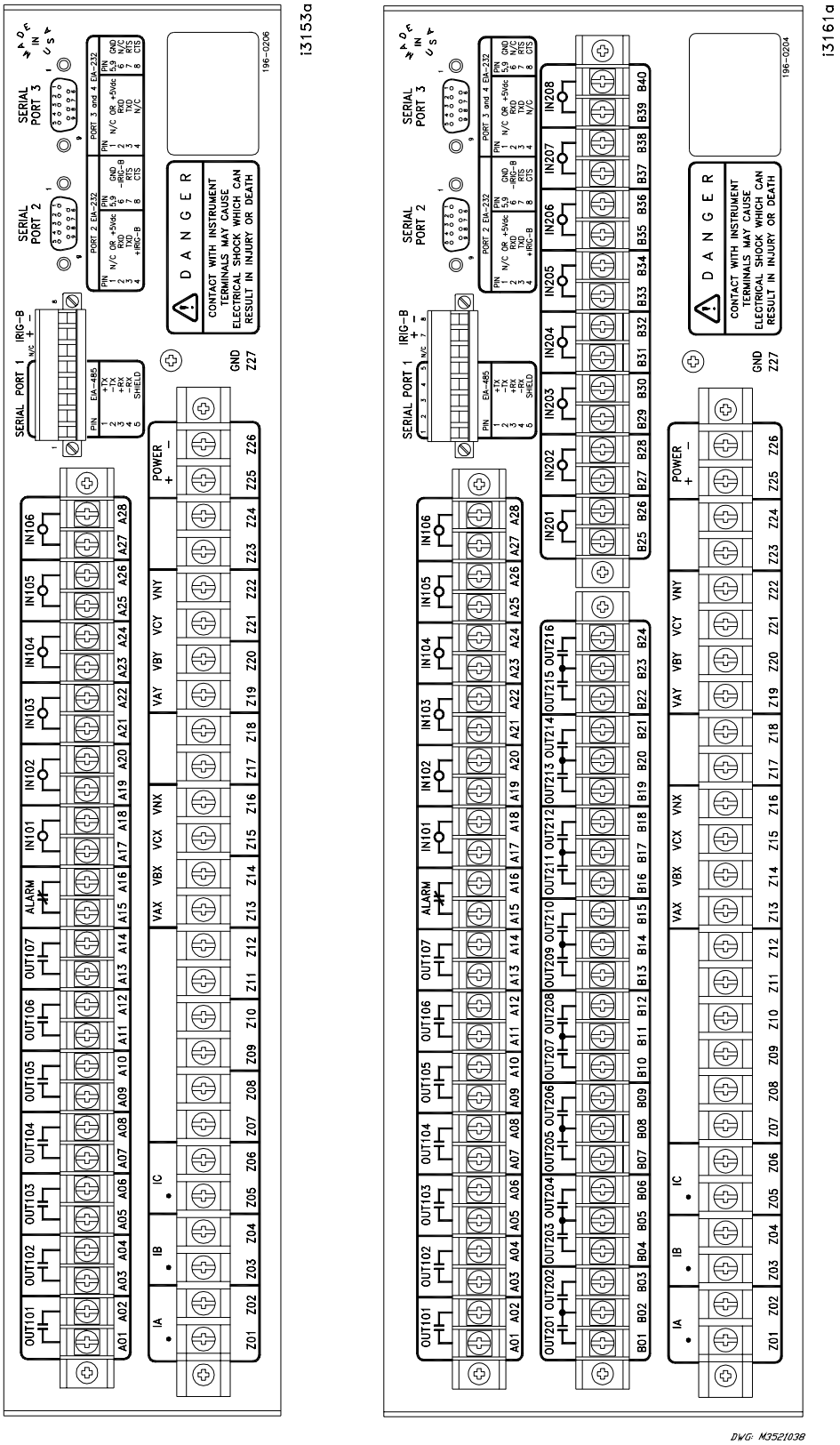


Figure 2.6: Rear-Panel Drawings–Models 0352x0xxxxX and 0352x1xxxx1

Figure 2.7: Rear-Panel Drawing–Model 0352x2xxxx15

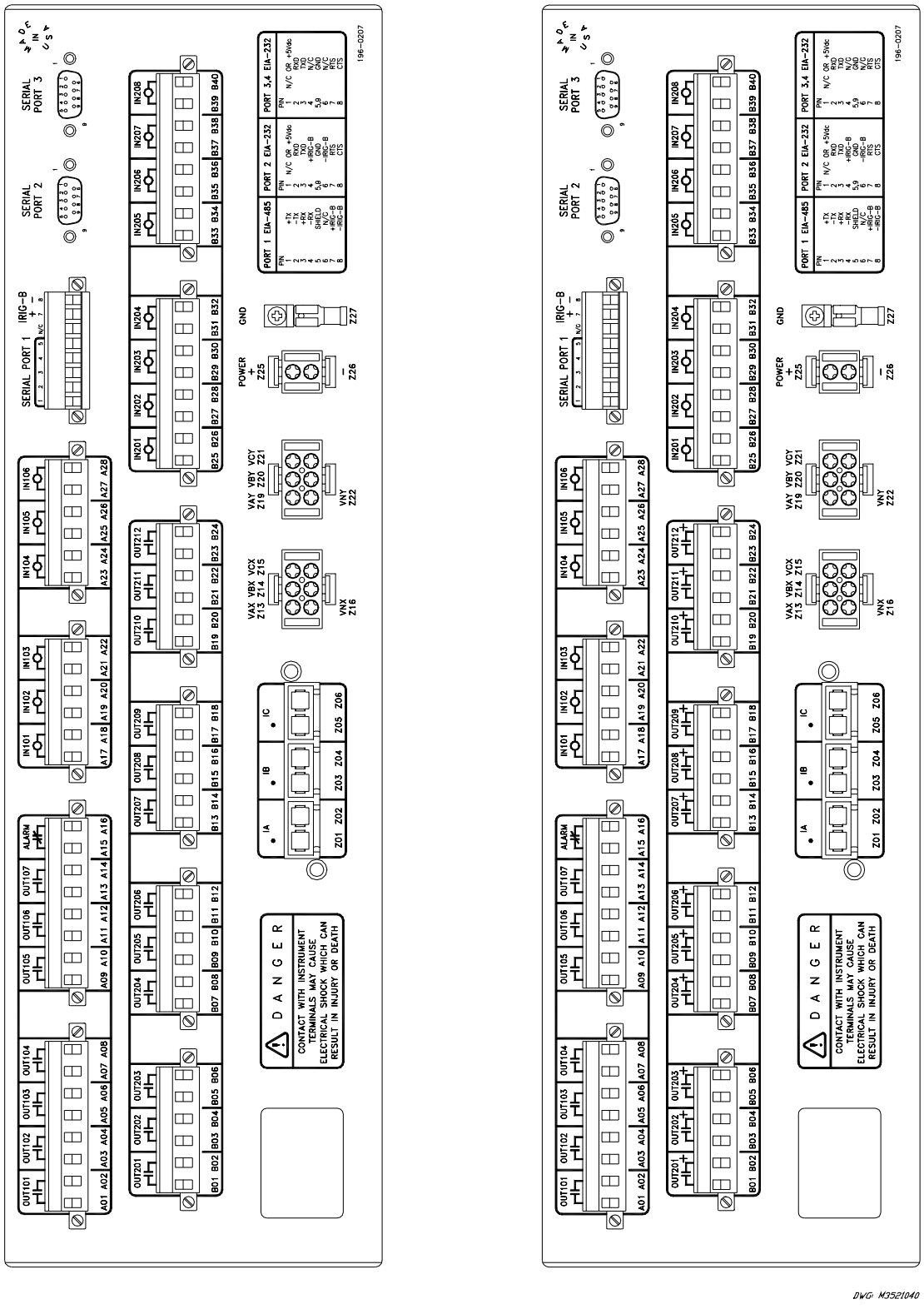


Figure 2.8: Rear-Panel Drawings–Models 0352xYxxxx2 and 0352xYxxxx6

Connections

Frame Ground

For safety and performance, ground the relay chassis at terminal GND (Z27). Connectorized relays provide a 0.250-inch-by-0.023-inch spade connector for this connection. The grounding terminal of either relay version connects directly to relay chassis ground.

Power Supply

Connect rear-panel terminals marked + (Z25) and – (Z26) to a source of control voltage. Control power passes through these terminals to a fuse(s) and to the switching power supply. The control power circuitry is isolated from the frame ground. The 24/48 V power supply is polarity sensitive. Refer to ***Section 1: Introduction and Specifications*** for power supply voltage ranges.

Current Transformer Inputs

Connect current inputs to the set of current input terminals. Note that the CT shorting connector providing current connections to Connectorized relays installs in only one orientation. Note also that the current input terminals on both terminal block and Connectorized relays have a mark at one terminal per phase to indicate polarity. Each current input is independent of the other two inputs.

Note: When installing CT shorting connectors, ensure that you secure each connector to the relay chassis with the screws at each connector end. When removing a CT shorting connector, pull it straight away from the relay rear panel. Removing a shorting connector causes internal mechanisms within the connector to individually short out each power system current transformer.

Potential Transformer Input

The two three-phase sets of voltage inputs are internally wye-connected voltage inputs. Each three-phase set of voltages is independent of the other.

The relay requires difference-voltage potentials obtained from voltage transformers on both sides of the circuit breaker for Scheme 1 of the flashover protection logic and the thermal protection logic.

Optoisolated Inputs

Connect control input wiring to the six standard inputs IN101–IN106 and to any of the I/O board optoisolated inputs IN201–IN208 you need for your application.

All control inputs are dry optoisolated inputs and are not polarity dependent. Specify a nominal-rated control voltage of 48, 110, 125, or 250 Vdc for level sensitive and 24 Vdc for nonlevel sensitive when ordering. To assert an input, apply nominal-rated control voltage to the terminals assigned to that input. A terminal pair is brought out for each input. Refer to the ***General Specifications*** in ***Section 1: Introduction and Specifications*** for optoisolated input ratings. There are no internal connections between inputs. ON and OFF values are normally within one volt of each other, in the indicated range.

Output Contacts

Four types of output contacts are available with various input/output board configurations.

The SEL-352 Relay main board has eight standard independent output contacts OUT101 through OUT107 and ALARM. Output contact and optoisolated input options are discussed in ***Optional Interface Boards*** at the end of this section. The following diagrams and descriptions present the various output contacts available. The contact diagrams are identical for both terminal block and Connectorized relay types. They are illustrated here as they apply to a terminal block version.

Standard independent dry output contacts that are not polarity dependent are represented by Figure 2.9.

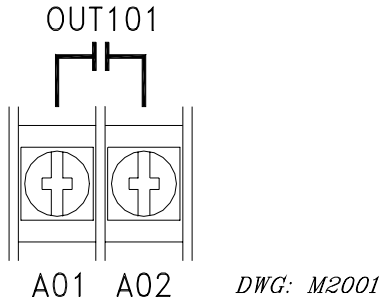


Figure 2.9: Standard Independent Output Contact Representation

Standard dry output contacts that **share** a common terminal for each pair of contacts, but are not polarity dependent, are represented by Figure 2.10:

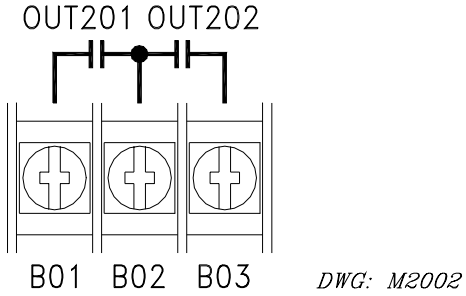


Figure 2.10: Standard Shared Terminal Output Contact Representation

High Current Interrupting dry output contacts are **polarity dependent** and are represented by Figure 2.11. Notice the polarity mark above terminal A02. Reversed polarity appears as a short across the contact terminals.

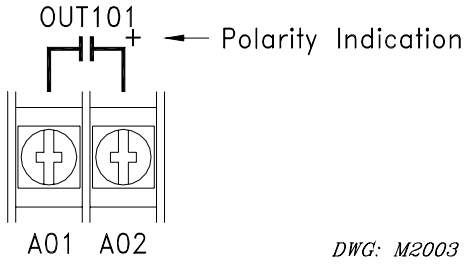


Figure 2.11: High Current Interrupting Output Contact Representation

Fast High Current Interrupting dry output contacts that are not polarity dependent are represented by Figure 2.12.

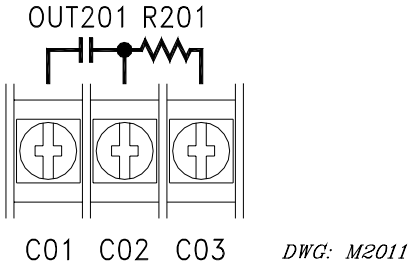


Figure 2.12: Fast High Current Interrupting Output Contact Representation (Note: Some early model versions did not show the resistor)

Communications Port

Refer to Table 2.1 for a list of cables that you can purchase from SEL for various communication applications. Refer to ***Section 8: Serial Port Communications and Commands*** for detailed cable diagrams for selected cables.

Note: Listing of devices not manufactured by SEL is for the convenience of our customers. SEL does not specifically endorse or recommend such products nor does SEL guarantee proper operation of those products, or the correctness of connections, over which SEL has no control.

The relay rear panel provides pin definitions for Ports 1, 2, 3, and 4. Refer also to ***Section 8: Serial Port Communications and Commands*** for more serial port details. Port 1 is an EIA-485 protocol connection on the rear of the relay. Port 1 accepts a plug-in/plug-out terminal block that supports wire sizes from 24 AWG to as large as 12 AWG. The connector comes with the relay. Ports 2, 3, and 4 are EIA-232 protocol connections with Ports 2 and 3 on the rear of the relay and Port 4 on the front of the relay. These female connectors are 9-pin, D-subminiature connectors. You can use any combination of these ports or all of them simultaneously for relay communication.

For example, to connect the SEL-352 Relay Ports 2, 3, or 4 to the 9-pin male connector on a laptop computer, order cable number C234A and specify the length needed. Standard length is eight feet. To connect the SEL-352 Relay Port 2 to the SEL-2020 or SEL-2030 Communications Processor that supplies the communication link and the time-synchronization signal, order cable number C273A and specify the length needed. For connecting devices at more than 100 feet,

fiber-optic transceivers are available. The SEL-2800 family of transceivers provides fiber-optic links between devices for electrical isolation and long-distance signal transmission. Call the factory for further information on these products.

Table 2.1: SEL-352 Relay Communications Cable Numbers

SEL-352 Port #	Connect to Device (gender refers to the device)	SEL Cable #
2, 3, 4	PC, 25-Pin Male (DTE)	C227A
2, 3, 4	PC, 9-Pin Male (DTE)	C234A
2, 3	SEL-2020 or SEL-2030 without IRIG-B	C272A
2	SEL-2020 or SEL-2030 with IRIG-B	C273A
2	SEL-IDM, Ports 2 through 11	Requires a C254 and C257 cable
2, 3	Modem, 5 Vdc Powered (Pin 10)	C220*
2, 3	Standard Modem, 25-Pin Female (DCE)	C222

* The 5 Vdc serial port jumper must be installed to power the modem using C220 (see ***EIA-232 Serial Port Jumpers*** later in this section).

Clock Synchronization, IRIG-B

Refer to Table 2.1 for a list of cables that you can purchase from SEL for various time-synchronizing applications.

The SEL-352 Relay accepts a demodulated IRIG-B format signal for synchronizing an internal clock to some external source such as the SEL-2020 or SEL-2030 Communications Processor, SEL-IDM, or satellite time clock. Connect the IRIG-B source to the relay through the connectors for serial Ports 1 or 2. Refer to the port pin definition of each port for the appropriate connection.

Plug-In Connectors (Connectorized Model 0352xY)

For the Connectorized SEL-352 Relay model 0352xY, the wiring harness kit, designated SEL-WA0352, must be ordered separately. It contains several pre-wired connectors for the relay current and voltage inputs, power, and ground connections. It also contains unwired connectors for the relay optoisolated inputs, contact outputs, and EIA-485 serial port connections. A small slotted-tip screwdriver and a wire stripping tool are required for preparation of these unwired connectors. Refer to the Ordering Information for the SEL-WA0352 wiring harness for selection of wire size, type, and length for the pre-wired connectors.

The SEL-WA0352 wiring harness includes the following connectors (not pre-wired):

- Two eight-position female plug-in connectors for output contacts OUT101 through OUT104 and OUT105 through ALARM.

- Two six-position female plug-in connectors for optoisolated inputs IN101 through IN103 and IN104 through IN106.
- One eight-position female plug-in connector for the EIA-485 serial port connection Port 1, and the demodulated IRIG-B input. (Alternatively, IRIG-B may be brought through Port 2.)
- Four six-position female plug-in connectors for I/O board output contacts OUT201 through OUT203, OUT204 through OUT206, OUT207 through OUT209, and OUT210 through OUT212.
- Two eight-position female plug-in connectors for I/O board optoisolated inputs IN201 through IN204 and IN205 through IN208.

These connectors accept wire sizes AWG 24 to 12. Strip the wires 0.31" (8 mm) and install with a small slotted-tip screwdriver. Secure each connector to the relay chassis with the screws located on each end of the connector.

The SEL-WA0352 wiring harness includes the following pre-wired connectors:

- One six-position CT shorting connector for current inputs IA, IB, and IC. The wire size selection is from AWG 16 to 10.
- One six-position connector (four positions used) for voltage inputs VAX, VBX, VCX, and VNX. The wire size selection is from AWG 18 to 14.
- One six-position connector (four positions used) for voltage inputs VAY, VBY, VCY, and VNY. The wire size selection is from AWG 18 to 14.
- One connector for POWER inputs (+ and –). The wire size selection is from AWG 18 to 14.
- One spade connector for chassis GROUND connection.

Plug the CT shorting connector into terminals Z01 through Z06. Secure the connector to the relay chassis with the two screws located on each end of the connector. When removing the CT shorting connector, pull it straight away from the relay rear panel. When the connector is removed, internal mechanisms within the connector separately short out each power system current transformer. This connector may be installed in only one orientation.

Plug the voltage connectors into terminals Z13 to Z16 for the VX inputs and Z19 to Z22 for the VY inputs, as appropriate. These connectors may be installed in only one orientation.

Plug the power connector into terminals Z25 (+) and Z26 (–). Control power passes through these terminals to a fuse and to the relay power supply. This circuitry is isolated from the relay chassis ground.

Ground the relay chassis at terminal Z27 with the spade connector provided (tab size 0.25" wide by 0.032" thick). If the tab on the chassis is removed, the chassis ground connection can be made with the size #6-32 screw.

Note: Important: Improvements in Connectorized SEL-352 Relays (Plug-In Connectors) Result in Part Number Changes

The current transformer shorting connector (for current channel inputs IA, IB, IC, and IN) has been made more robust. This improvement makes the new connector design incompatible with the old design. Thus, presently constructed Connectorized SEL-352

Relays with this improved connector have a new part number (partial part numbers shown):

Old	New
03521J	0352xY

The respective wiring harness part numbers for these old and new Connectorized SEL-352 Relays are (partial part numbers shown):

Old	New
WA03521J	WA0352xY

The other connectors on the Connectorized SEL-352 Relay rear panel (power input, voltage inputs, output contacts, etc.) are the same for the old or new models. Only the current transformer shorting connector has changed.

Figure 2.8 shows the rear panel for the new model 0352xY. This figure can also be used as a reference for the old model 0352xJ. All terminal labeling/numbering remains the same.

TYPICAL AC/DC CONNECTIONS

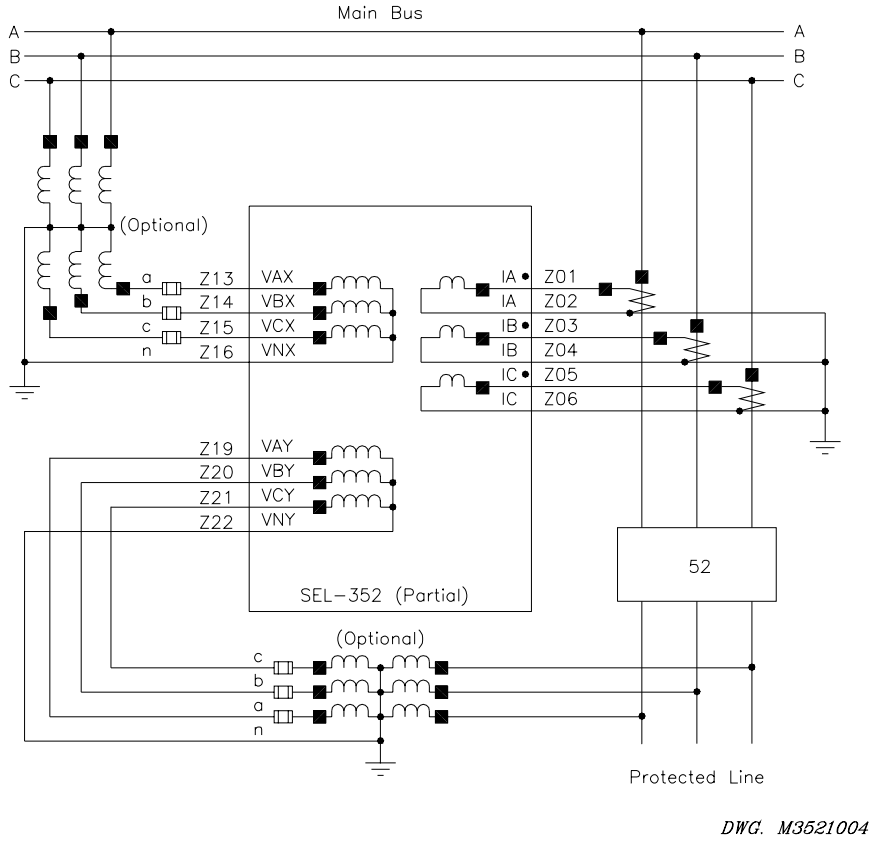


Figure 2.13: SEL-352 Relay Typical External AC Connections

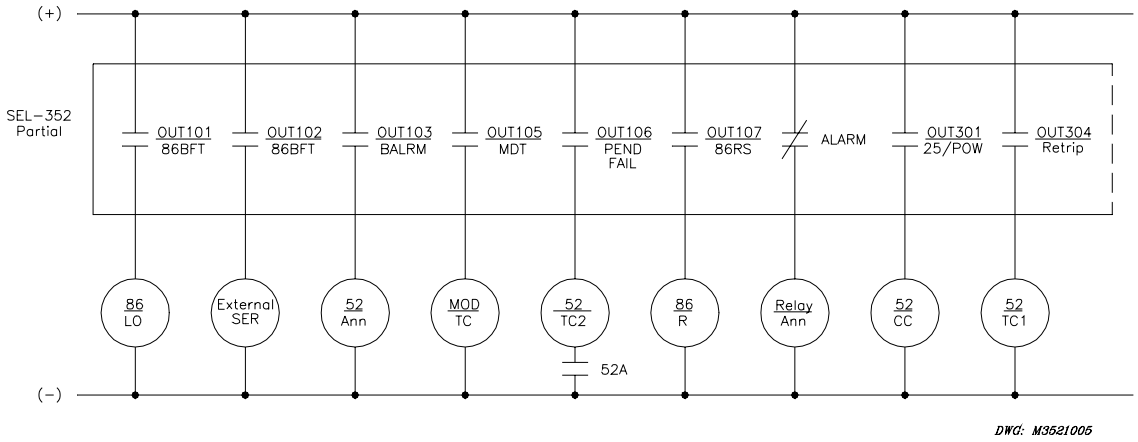


Figure 2.14: SEL-352 Relay Example DC Output Contact Connections

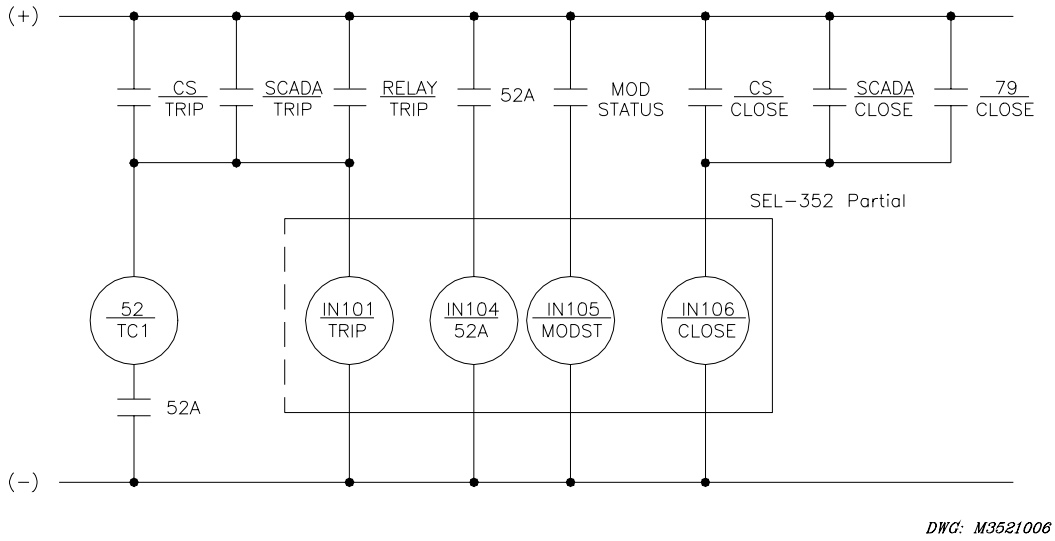


Figure 2.15: SEL-352 Relay Example DC Input Connections

CIRCUIT BOARD CONFIGURATION

In this section we describe (1) how to remove the relay circuit boards so you can change circuit board jumpers or replace the clock battery and (2) how to replace the circuit boards in the relay.

Accessing the Relay Circuit Boards

1. De-energize the relay by removing the connections to rear-panel terminals + (Z25) and – (Z26). Accomplish this easily on Connectorized relays by removing the connector at rear-panel terminals + (Z25) and – (Z26).

2. Remove any cables connected to serial ports on the front and rear panels.

3. Loosen the six front-panel screws (they remain attached to the front panel) and remove the relay front panel.

   CAUTION

   The relay contains devices sensitive to electrostatic discharge (ESD). When working on the relay with front or top cover removed, work surfaces and personnel must be properly grounded or equipment damage may result.

4. Each circuit board corresponds to a row of rear-panel terminal blocks or connectors and is affixed to a draw-out tray. Identify which draw-out tray needs to be removed. An SEL-352 Relay Model 0352x0 has only a main board. A Model 0352x1 or 0352xY relay has an extra I/O board below the main board.

5. Disconnect circuit board cables as necessary so you can remove the board and draw-out tray you want. To remove the extra I/O board, first remove the main board. Remove ribbon cables by pushing the extraction ears away from the connector. Remove the six-conductor power cable by grasping the wires near the connector and pulling away from the circuit board.

6. Grasp the drawout assembly of the board and pull the assembly from the relay chassis.

7. Locate the jumper(s) or battery to be changed. Make the changes you want. Note that the output contact jumpers are soldered in place.

8. When finished, slide the drawout assembly into the relay chassis. Reconnect the cables you removed in step 5. Replace the relay front-panel cover.

9. Replace any cables previously connected to serial ports.

10. Reenergize the relay by reconnecting wiring to rear-panel terminals + (Z25) and – (Z26). On Connectorized versions, replace the power connector at rear-panel terminals + (Z25) and – (Z26).

Main Board

Output Contact Jumpers

Refer to Figure 2.16 to see the layout of the main board and locate the solder jumpers to the rear of the output contacts. Select the contact type for the output contacts. With a jumper in the A position, the corresponding output contact is an “a” output contact. An “a” output contact is open when the output contact coil is de-energized and closed when the output contact coil is energized. With a jumper in the B position, the corresponding output contact is a “b” output contact. A “b” output contact is closed when the output contact coil is de-energized and open when the output contact coil is energized. These jumpers are soldered in place but may be changed in the field.

Note that the ALARM output contact is a “b” contact and that the other output contacts are all “a” contacts. This is the normal configuration of these jumpers in a standard relay shipment. The additional I/O boards have slightly different layout locations for the jumpers relative to the corresponding output contacts.

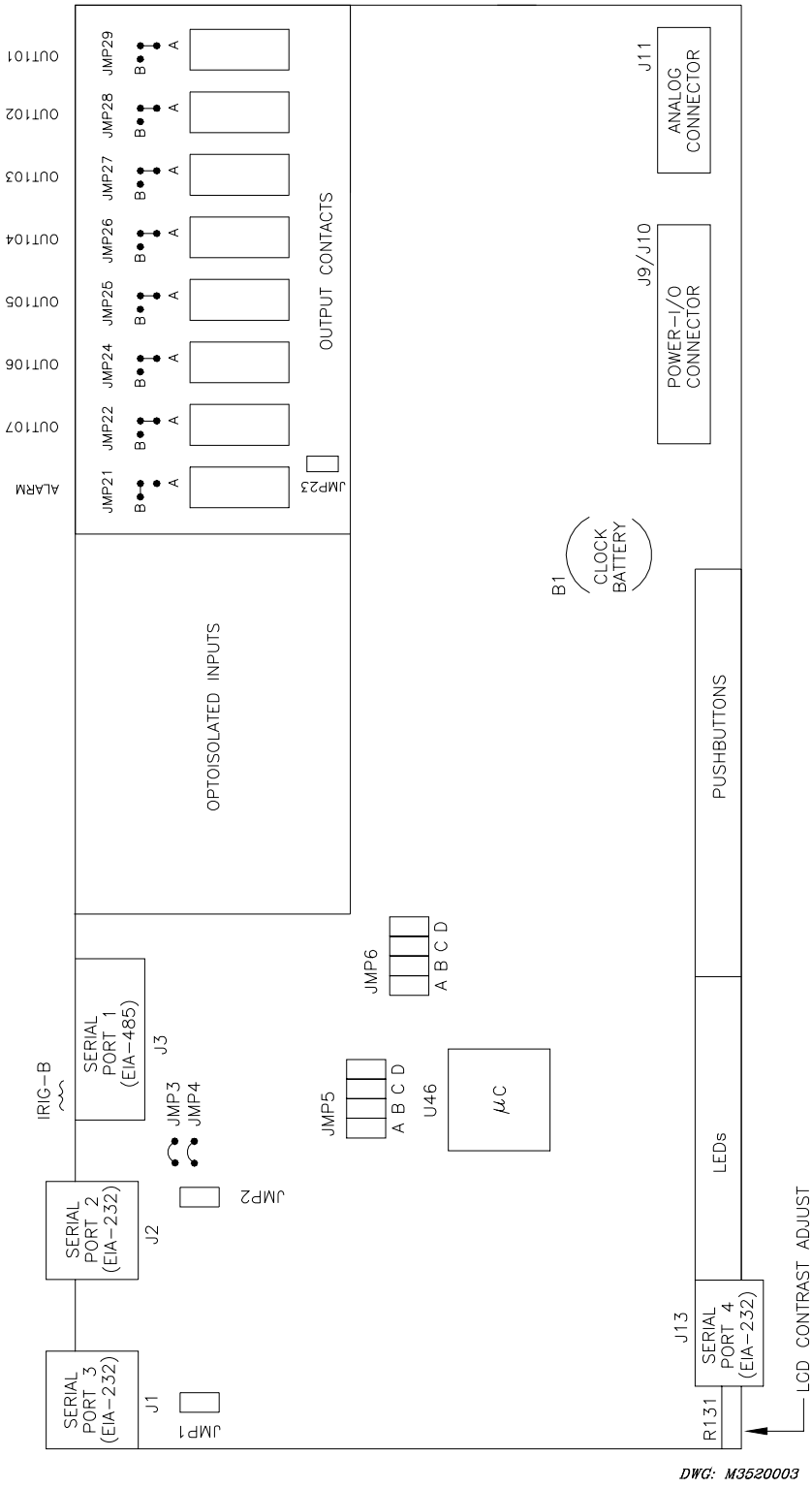


Figure 2.16: SEL-352 Relay Main Board Jumpers, Connections, and Battery Locations

Second ALARM Contact Jumper

Note the locations of main board jumper JMP23 and output contact OUT107 in Figure 2.16, and refer to Table 2.2 to understand the relationship between the jumper and output contact. The jumper JMP23 controls the operation of output contact OUT107. JMP23 provides the option of a second alarm output contact by changing the signal that drives output contact OUT107.

Table 2.2: SEL-352 Relay Second ALARM Contact Jumper Position

JMP23 Position	Output Contact OUT107 Operation
Bottom (Pins 1 & 2)	Second Alarm output contact (operated by alarm logic/circuitry). Relay Word bit OUT107 has no effect on output contact OUT107 when jumper JMP23 is in this position.
Top (Pins 2 & 3)	Regular output contact OUT107 (operated by Relay Word bit OUT107). Jumper JMP23 comes in this position in a standard relay shipment.
Neither	Disable output contact OUT107. If JMP23 is not installed, output contact OUT107 is not functional and will remain in its de-energized state.

If jumper JMP23 is installed on the two bottom pins and both output contacts OUT107 and ALARM are the same output contact type (a or b), they will be in the same state (closed or open). If jumper JMP23 is installed on the two bottom pins and output contacts OUT107 and ALARM are different output contact types (one is an "a" and one is a "b"), they will be in opposite states (one is closed and one is open).

Password and Breaker Jumpers

Refer to Figure 2.16 and note the password and breaker jumpers identified as JMP6. To change these jumpers, remove the relay front panel and main board according to the steps outlined previously in ***Accessing the Relay Circuit Boards***.

Put password jumper JMP6A (left-most jumper) in place to disable serial port and front-panel password protection. With the jumper removed, password security is enabled. View or set the passwords with the **PASSWORD** command (see ***Section 8: Serial Port Communications and Commands***).

Put breaker jumper JMP6B in place to enable the serial port commands **OPEN**, **CLOSE**, and **PULSE**. The relay ignores these commands while you remove JMP6B. Use these commands primarily to assert output contacts for circuit breaker control or testing purposes (see ***Section 8: Serial Port Communications and Commands***).

Do not install jumpers in position JMP6C or JMP6D. If a jumper is in position JMP6D and you lose dc power to the relay, the relay will power up in SELBoot when power is restored. The front panel will show "SELBoot" and then a warning to remove the jumper when you attempt serial port communication.

EIA-232 Serial Port Jumpers

Refer to Figure 2.16. Jumpers JMP1 and JMP2 are toward the rear of the main board, near the rear-panel EIA-232 serial communications ports. These jumpers connect or disconnect +5 Vdc to Pin 1 on the EIA-232 serial communications Ports 2 and 3. SEL normally ships relays with these jumpers removed (out of place) so that the +5 Vdc is not connected to Pin 1 on the EIA-232 serial communications ports. JMP1 controls the +5 Vdc for Port 3, and JMP2 controls the +5 Vdc for Port 2 (see Table 8.1 in ***Section 8: Serial Port Communications and Commands***). If these jumpers are installed, be certain not to short the power supply with an incorrect communication cable. The +5 Vdc connections supply current as high as 1 A.

Solder jumpers JMP3 and JMP4 allow connection of an IRIG-B source to Port 2. Removal of JMP3 and JMP4 will cause Port 2 to no longer accept an IRIG-B signal. The Port 1 connector always accepts an IRIG-B signal. Port 2 and Port 1 IRIG-B circuits are in parallel; therefore, connect only one IRIG-B source at a time.

Condition of Acceptability for North American Product Safety Compliance

To meet product safety compliance for end-use applications in North America, use an external fuse rated 3 A or less in-line with the +5 Vdc source on Pin 1. SEL fiber-optic transceivers include a fuse that meets this requirement.

Other Jumpers

Additional main board jumpers JMP5A through JMP5D, located near JMP6, are not functional in the SEL-352 Relay. Originally they were installed for developmental testing purposes but are not used in the production version of the relay. Jumpers must not be installed in any JMP5 position.

Low-Level Analog Interface

SEL designed the SEL-352 Relay main board to accept low-level analog signals as an optional testing method. ***Section 11: Testing and Troubleshooting*** contains a more detailed discussion of the patented Low-Level Test Interface; Figure 11.1 shows the pin configuration. The SEL-RTS (Relay Test System) interfaces with the relay through a ribbon cable connection on the main board. With the front panel removed, the low-level interface connector is on the front edge at the far right of the top board. Refer to Figure 2.16. Remove the ribbon cable from the main board (top board), and connect the SEL-RTS ribbon cable to the main board. This removes the connection from the transformers in the bottom of the relay chassis and connects the SEL-RTS system for low-level testing. Refer to the SEL-RTS Instruction Manual for system operation. For normal operation, be sure to properly reinstall the ribbon cable that connects the transformers in the bottom of the chassis to the main board.

Clock Battery

Refer to Figure 2.16 for clock battery B1 location. This lithium battery powers the relay clock (date and time) if the external power source is lost or removed. The battery is a 3 V lithium coin cell. At room temperature (25°C) the battery will operate nominally for 10 years at rated load.

Because little self-discharge of the battery occurs when an external source powers the relay, battery life can extend well beyond the nominal 10 years. The battery cannot be recharged.

If the relay does not maintain the date and time after power loss, replace the battery. Follow the instructions previously described in ***Accessing the Relay Circuit Boards*** in this section to remove the relay main board.

CAUTION

There is danger of explosion if the battery is incorrectly replaced. Replace only with Ray-O-Vac® no. BR2335 or equivalent recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Remove the battery from beneath the clip and install a new one. The positive side (+) of the battery faces up. Reassemble the relay as described in ***Accessing the Relay Circuit Boards***. Set the relay date and time via serial communications port or front panel (see ***Section 8: Serial Port Communications and Commands*** or ***Section 9: Front-Panel Interface***).

Optional Interface Boards

Different interface boards are available for SEL-352 Relay application flexibility. The number of inputs, number of outputs, operating speeds, interrupt capabilities, and operation configuration vary depending on the interface board. This subsection describes each optional I/O board and shows a partial rear-panel diagram for each optional I/O board. To determine what I/O boards are installed in an existing relay, issue the **INI <ENTER>** command. Refer to ***Section 8: Serial Port Communications and Commands*** for a complete description of the command. Each I/O board has a type number associated with it as shown in Table 2.3.

Table 2.3: Interface Board Types

Interface Board	Type	Inputs	Outputs
Main	00	6	7, Standard Independent
Interface 1	21	8	16, Standard Shared-Terminal
Interface 2	42	8	12, Standard Independent
Interface 4	84	16	4, Standard Independent
Interface 5	E5	8	8, Fast Hybrid (High Current Interrupting)
Interface 6	46	8	12, Hybrid (High Current Interrupting)

Interface Board 1 (16 Outputs, 8 Inputs)

Optoisolated Inputs

All eight control inputs are dry optoisolated inputs and are not polarity dependent. Input options are 24 Vdc standard or 48, 110, 125, or 250 Vdc level sensitive. Control voltage must be specified when ordering. To assert an input, apply control voltage to the terminals assigned to that input. Each input is individually isolated, and a terminal pair is brought out for each input.

There are no internal connections between inputs. See ***General Specifications*** in ***Section 1: Introduction and Specifications*** for ratings.

Output Contacts

30 A make
6 A carry
Closing (pickup for "a" contacts, dropout for "b" contacts): 1/4-cycle or less
Opening (dropout for "a" contacts, pickup for "b" contacts): 1/2-cycle or less (typical is 1/4-cycle)

These 16 **standard** dry output contacts **share** a common terminal for each pair of contacts, but are not polarity dependent. The rear of the relay will be similar to the following figures:

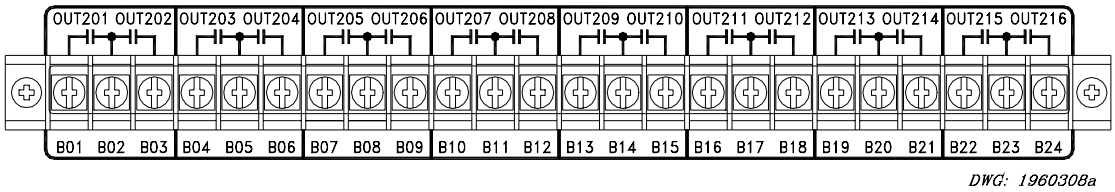


Figure 2.17: Interface Board 1 Output Contacts (Board Position 1)

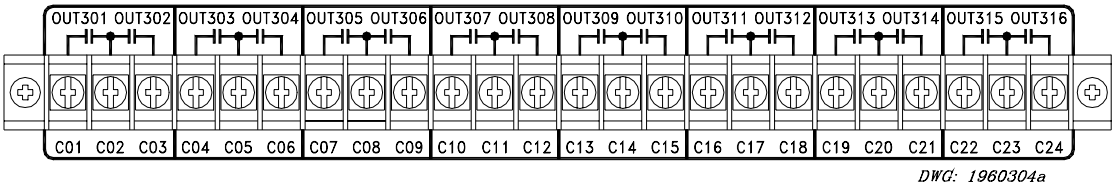


Figure 2.18: Interface Board 1 Output Contacts (Board Position 2)

Configure the output contacts as "a" contacts or "b" contacts with solder jumpers. Figure 2.19 shows the location of the jumpers and explains the jumper position. Contacts are factory configured as "a" contacts.

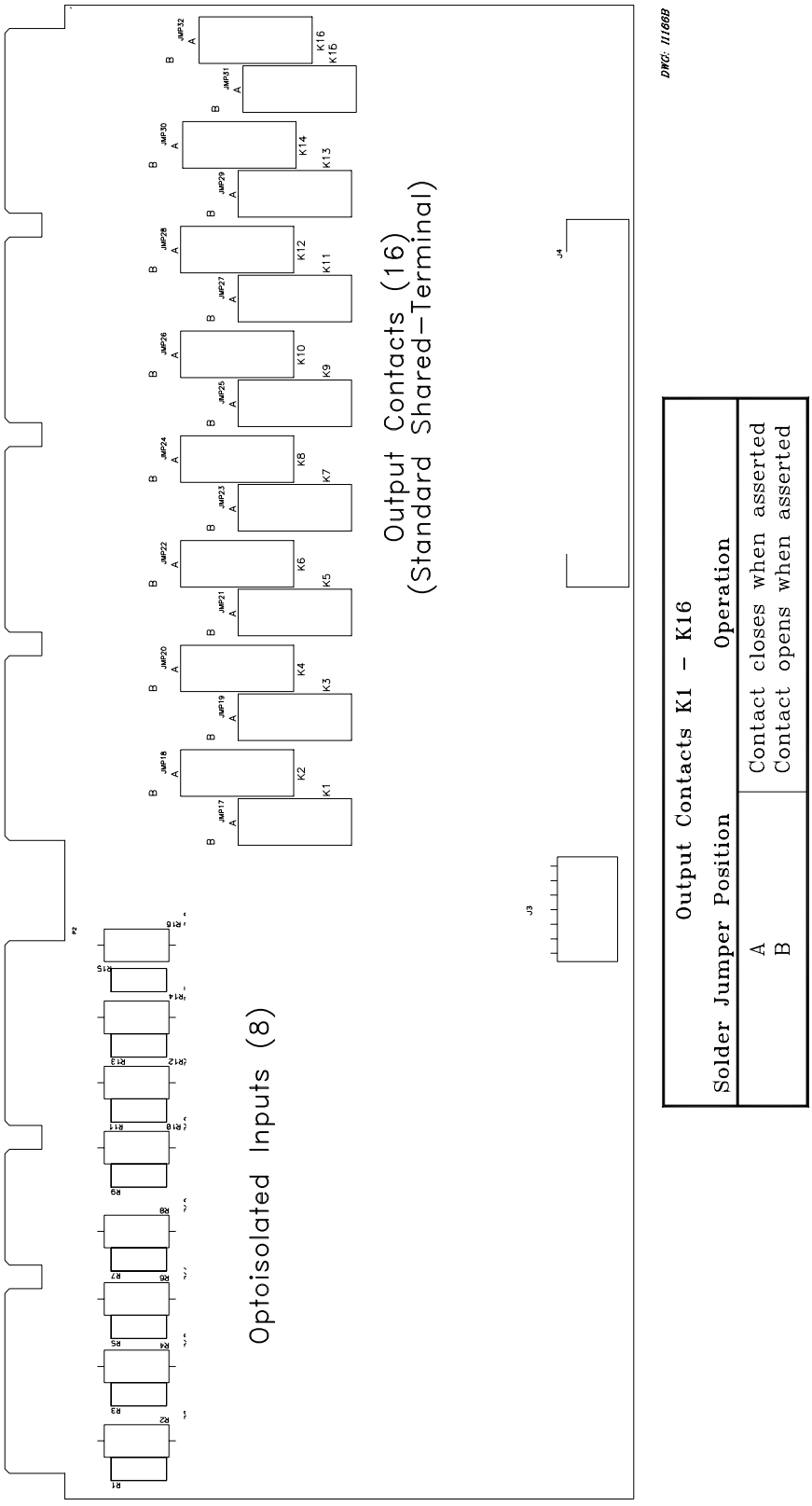


Figure 2.19: Interface Board 1 Component Layout

Interface Board 2 (12 Outputs, 8 Inputs)

Optoisolated Inputs

All eight control inputs are dry optoisolated inputs and are not polarity dependent. Input options are 24 Vdc standard or 48, 110, 125, or 250 Vdc level sensitive. Control voltage must be specified when ordering. To assert an input, apply control voltage to the terminals assigned to that input. Each input is individually isolated, and a terminal pair is brought out for each input. There are no internal connections between inputs. See ***General Specifications*** in ***Section 1: Introduction and Specifications*** for ratings.

Output Contacts

30 A make
6 A carry
Closing (pickup for "a" contacts, dropout for "b" contacts): 1/4-cycle or less
Opening (dropout for "a" contacts, pickup for "b" contacts): 1/2-cycle or less (typical is 1/4-cycle)

Interface Board 2 provides 12 output contacts. These 12 **standard** dry output contacts have **independent** terminals for each pair of contacts and are not polarity dependent. The rear of the relay will be similar to the following figures:

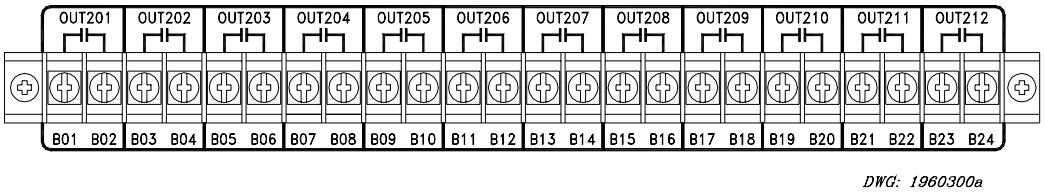


Figure 2.20: Interface Board 2 Output Contacts (Board Position 1)

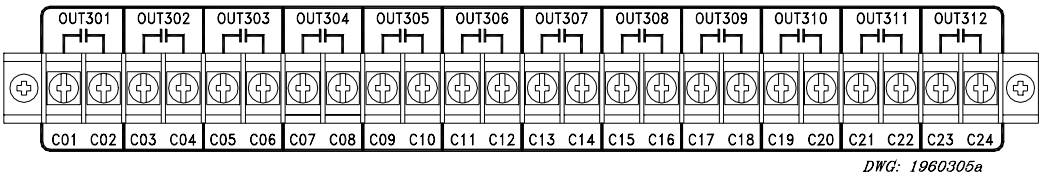


Figure 2.21: Interface Board 2 Output Contacts (Board Position 2)

Configure the output contacts as "a" contacts or "b" contacts with solder jumpers. Figure 2.22 and Figure 2.23 show the locations of the jumpers and explain the jumper positions. Contacts are factory configured as "a" contacts.

Note: The plug-in connector version of this board has only 4 jumper-configurable outputs (see Figure 2.23).

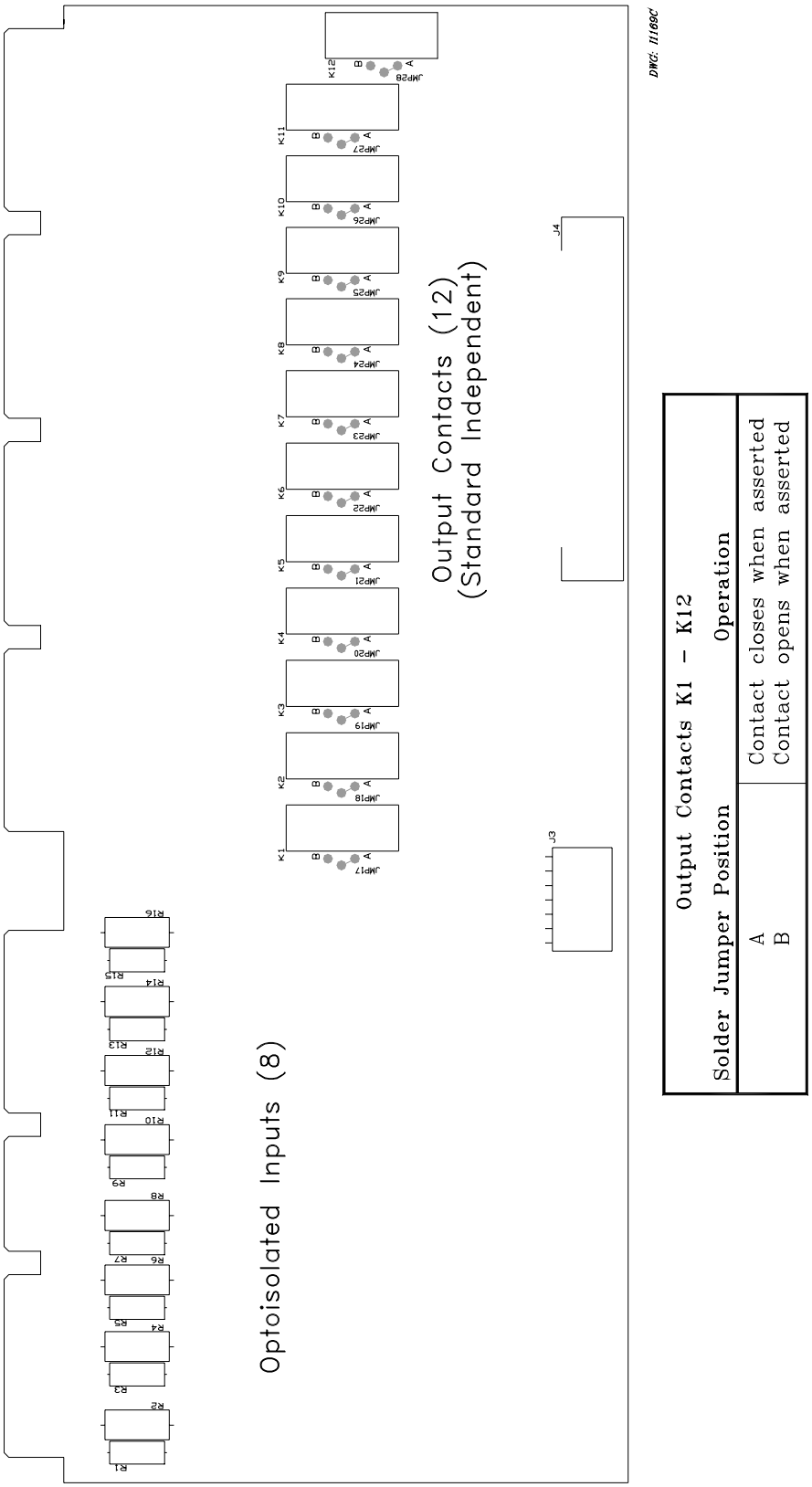


Figure 2.22: Interface Board 2 Component Layout (Screw-Terminal Block Version)

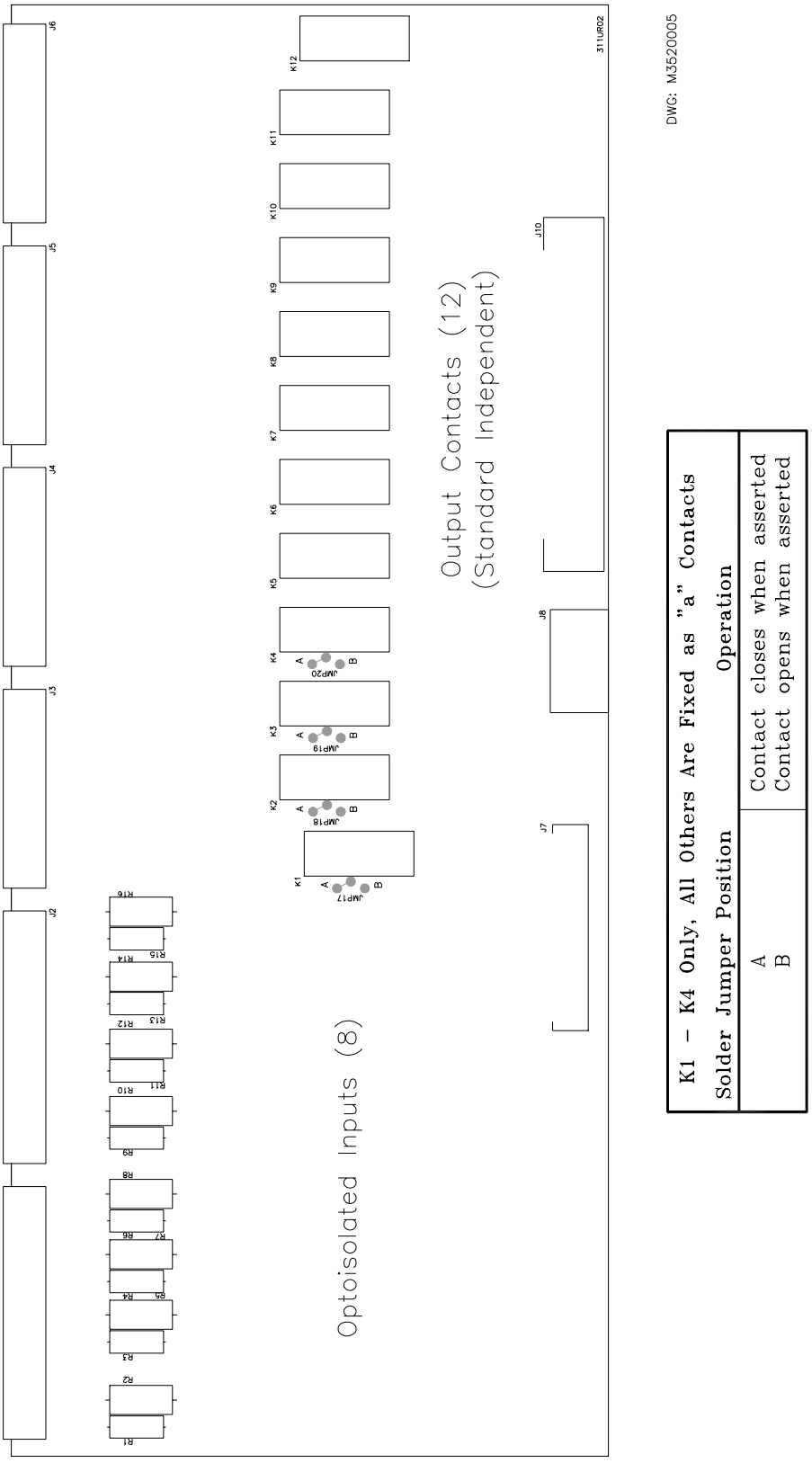


Figure 2.23: Interface Board 2 Component Layout (Plug-In Connector Version)

Interface Board 4 (4 Outputs, 16 Inputs)

Optoisolated Inputs

All eight control inputs are dry optoisolated inputs and are not polarity dependent. Input options are 24 Vdc standard or 48, 110, 125, or 250 Vdc level sensitive. Control voltage must be specified when ordering. To assert an input, apply control voltage to the terminals assigned to that input. Each input is individually isolated, and a terminal pair is brought out for each input. There are no internal connections between inputs. See ***General Specifications*** in ***Section 1: Introduction and Specifications*** for ratings.

Output Contacts

30 A make
6 A carry
Closing (pickup for "a" contacts, dropout for "b" contacts): 1/4-cycle or less
Opening (dropout for "a" contacts, pickup for "b" contacts): 1/2-cycle or less (typical is 1/4-cycle)

Interface Board 4 provides four "standard independent" output contacts. These four **standard independent** dry output contacts have terminals for each pair of contacts and are not polarity dependent. The rear of the relay will be similar to the following figures:

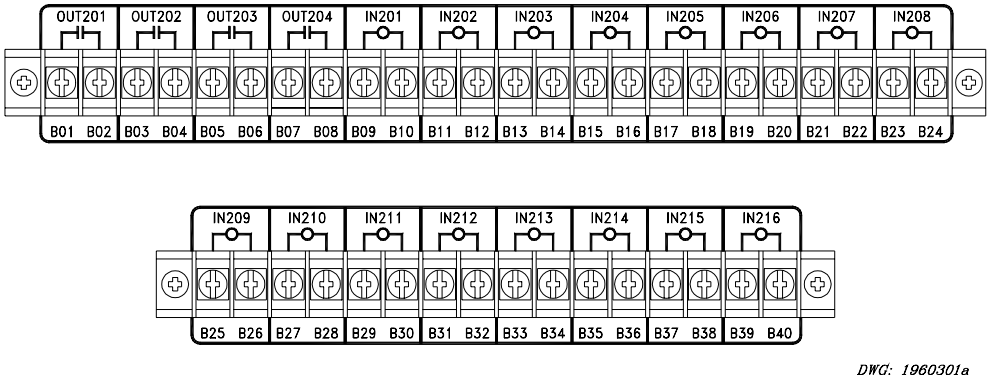


Figure 2.24: Interface Board 4 Output Contacts and Inputs (Board Position 1)

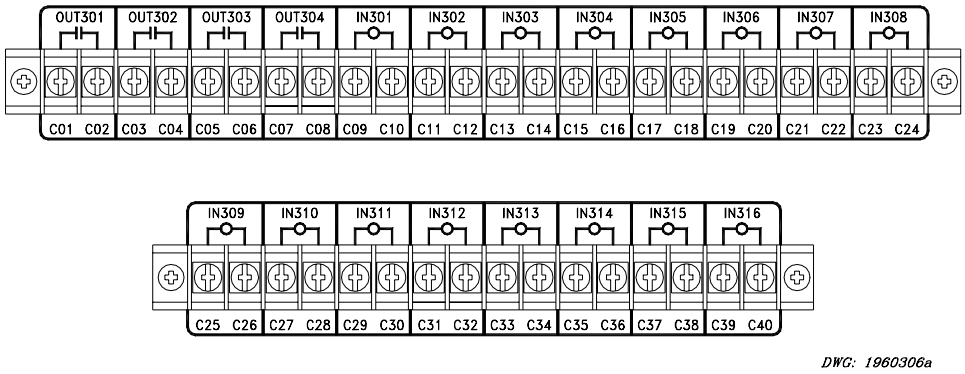


Figure 2.25: Interface Board 4 Output Contacts and Inputs (Board Position 2)

Configure the output contacts as “a” contacts or “b” contacts with solder jumpers. Figure 2.26 shows the location of the jumpers and explains the jumper position. Contacts are factory configured as “a” contacts.

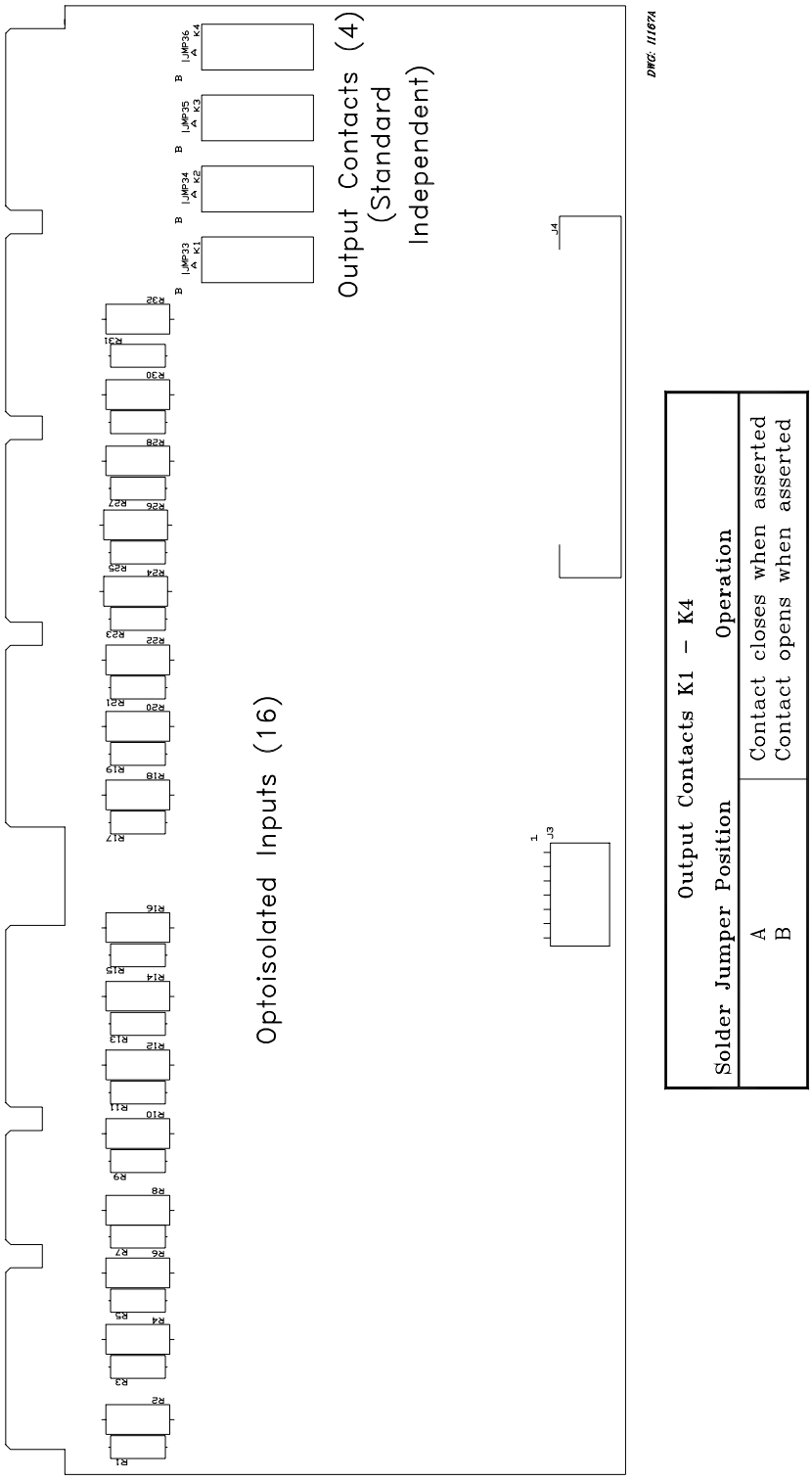


Figure 2.26: Interface Board 4 Component Layout

Interface Board 5 (8 Outputs, 8 Inputs)

Optoisolated Inputs

All eight control inputs are dry optoisolated inputs and are not polarity dependent. Input options are 24 Vdc standard or 48, 110, 125, or 250 Vdc level sensitive. Control voltage must be specified when ordering. To assert an input, apply control voltage to the terminals assigned to that input. Each input is individually isolated, and a terminal pair is brought out for each input. There are no internal connections between inputs. See ***General Specifications*** in ***Section 1: Introduction and Specifications*** for ratings.

Output Contacts

30 A make
6 A carry
10 A interrupt for L/R<0.04 seconds at 125 Vdc
10 A interrupt for L/R<0.02 seconds at 250 Vdc
Closing (pickup for "a" contacts, dropout for "b" contacts): 200 µs
Opening (dropout for "a" contacts, pickup for "b" contacts): 1/2-cycle or less (typical is 1/4-cycle)

Interface Board 5 provides eight output contacts. These eight **Fast High Current Interrupting** dry output contacts can interrupt 10 A of inductive current with an L/R <0.04 seconds. They operate (close for "a" contacts and open for "b" contacts) in less than 10 µs (.00001 seconds). Due to relay capabilities the outputs of the SEL-352 Relay are specified at 200 µs (.0002 seconds).

The output contact that is in the eighth position (K1 in Figure 2.30) may be configured as either an "a" or "b" contact. Figure 2.30 explains the jumper position. K1 is factory configured as an "a" contact. All other outputs 1–7 are fixed "a" contacts (closed when coil is energized).

Short transient inrush current may flow when a switch that is in series with the contact is closed, and the contact is open. This transient will not energize the circuit used in typical applications. Trip and close coils and standard auxiliary relays will not pick up; however, an extremely sensitive digital input or light-duty, high-speed auxiliary may pick up for this condition. The transient occurs when the capacitance of the output contact circuitry is charged. A third terminal (C03 in Figure 2.28) provides a path for charging the capacitance when the circuit is open.

Figure 2.29 shows some possible connections for this third terminal that will eliminate the possibility of transients when closing a switch. Circuit load is not shown. In general, the third terminal must be connected to the dc rail that is on the same side as the open switch condition. If an open switch may exist on either side of the output contact, only one condition may be considered. Two open switches (one on each side of the contact) defeat the charge circuit.

The rear of the relay will be similar to the following drawings:

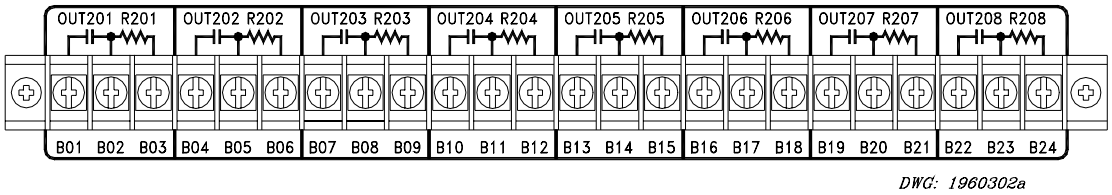


Figure 2.27: Interface Board 5 Output Contacts (Board Position 1)

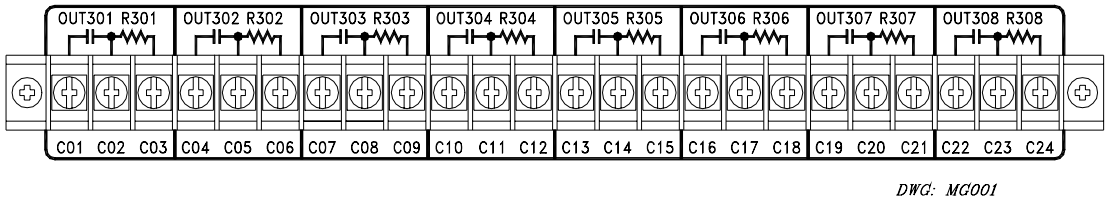


Figure 2.28: Interface Board 5 Output Contacts (Board Position 2)

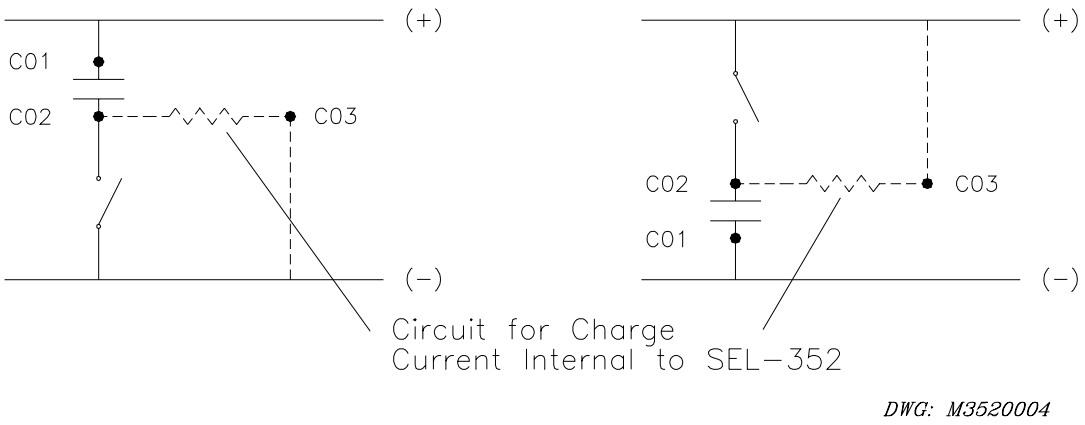


Figure 2.29: Possible Connections for Fast High Current Interrupting Output Contacts (Circuit Load Not Shown, Third Terminal Connection is Optional)

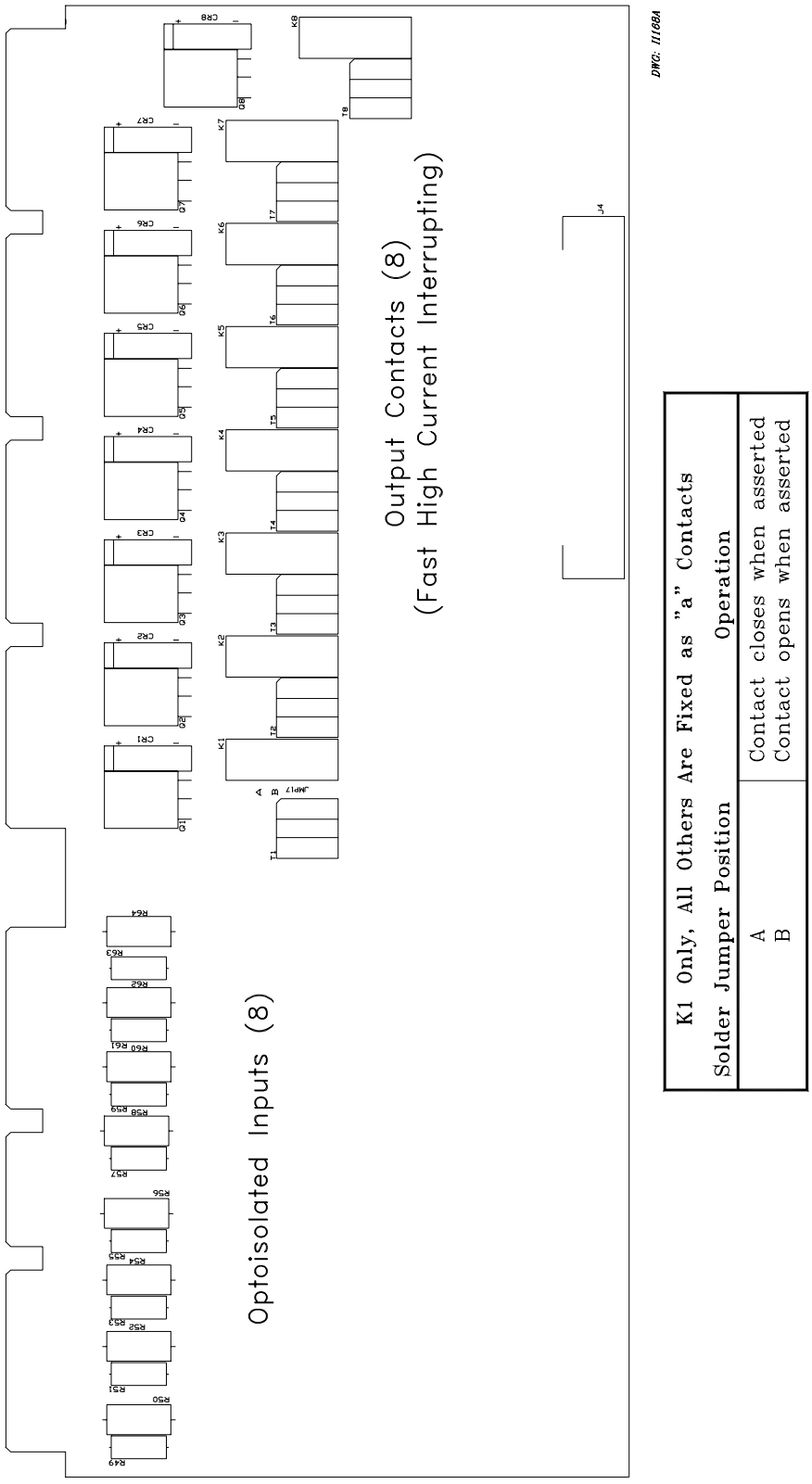


Figure 2.30: Interface Board 5 Component Layout

Interface Board 6 (12 Outputs, 8 Inputs)

Optoisolated Inputs

All eight control inputs are dry optoisolated inputs and are not polarity dependent. Input options are 24 Vdc standard or 48, 110, 125, or 250 Vdc level sensitive. Control voltage must be specified when ordering. To assert an input, apply control voltage to the terminals assigned to that input. Each input is individually isolated, and a terminal pair is brought out for each input. There are no internal connections between inputs. See ***General Specifications*** in ***Section 1: Introduction and Specifications*** for ratings.

Output Contacts

30 A make
6 A carry
10 A interrupt for L/R <0.04 seconds at 125 Vdc
10 A interrupt for L/R <0.02 seconds at 250 Vdc
Closing (pickup for "a" contacts, dropout for "b" contacts): 1/4-cycle or less
Opening (dropout for "a" contacts, pickup for "b" contacts): 1/2-cycle or less (typical is 1/4-cycle)

Interface Board 6 provides 12 output contacts. These 12 **High Current Interrupting** dry output contacts can interrupt 10 A of inductive current with an L/R <0.04 seconds at 125 Vdc. At 250 Vdc, they will interrupt 10 A of inductive current for an L/R <0.02 seconds. These outputs **are polarity dependent.** Notice the polarity mark above terminal B02 and C02 in the following figures that are similar to the rear of the relay:

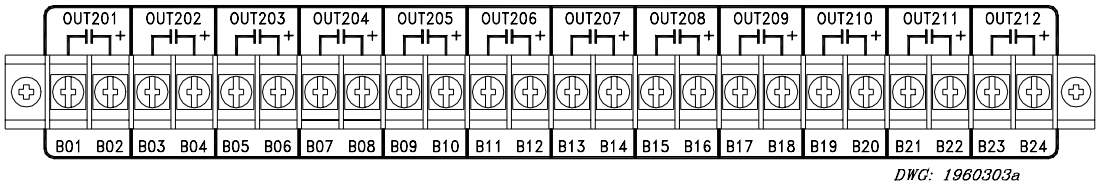


Figure 2.31: Interface Board 6 Output Contacts (Board Position 1)

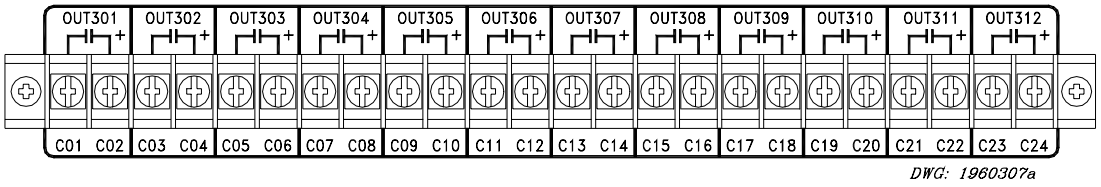


Figure 2.32: Interface Board 6 Output Contacts (Board Position 2)

Configure the output contacts as "a" contacts or "b" contacts with solder jumpers. Figure 2.33 and Figure 2.34 show the locations of the jumpers and explain the jumper positions. Contacts are factory configured as "a" contacts.

Note: The plug-in connector version of this board has only four jumper-configurable outputs (see Figure 2.34.)

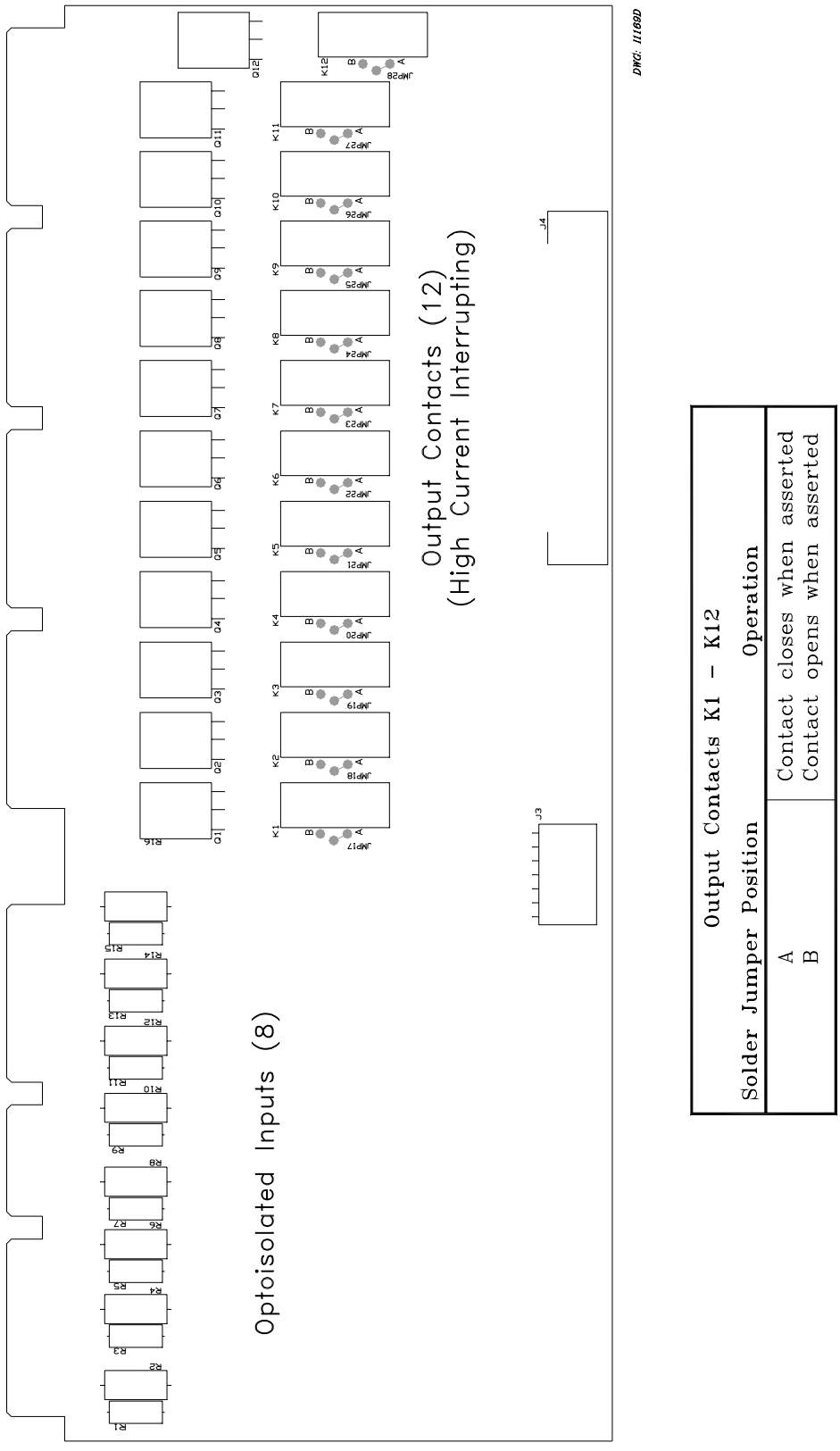


Figure 2.33: Interface Board 6 Component Layout (Screw-Terminal Block Version)

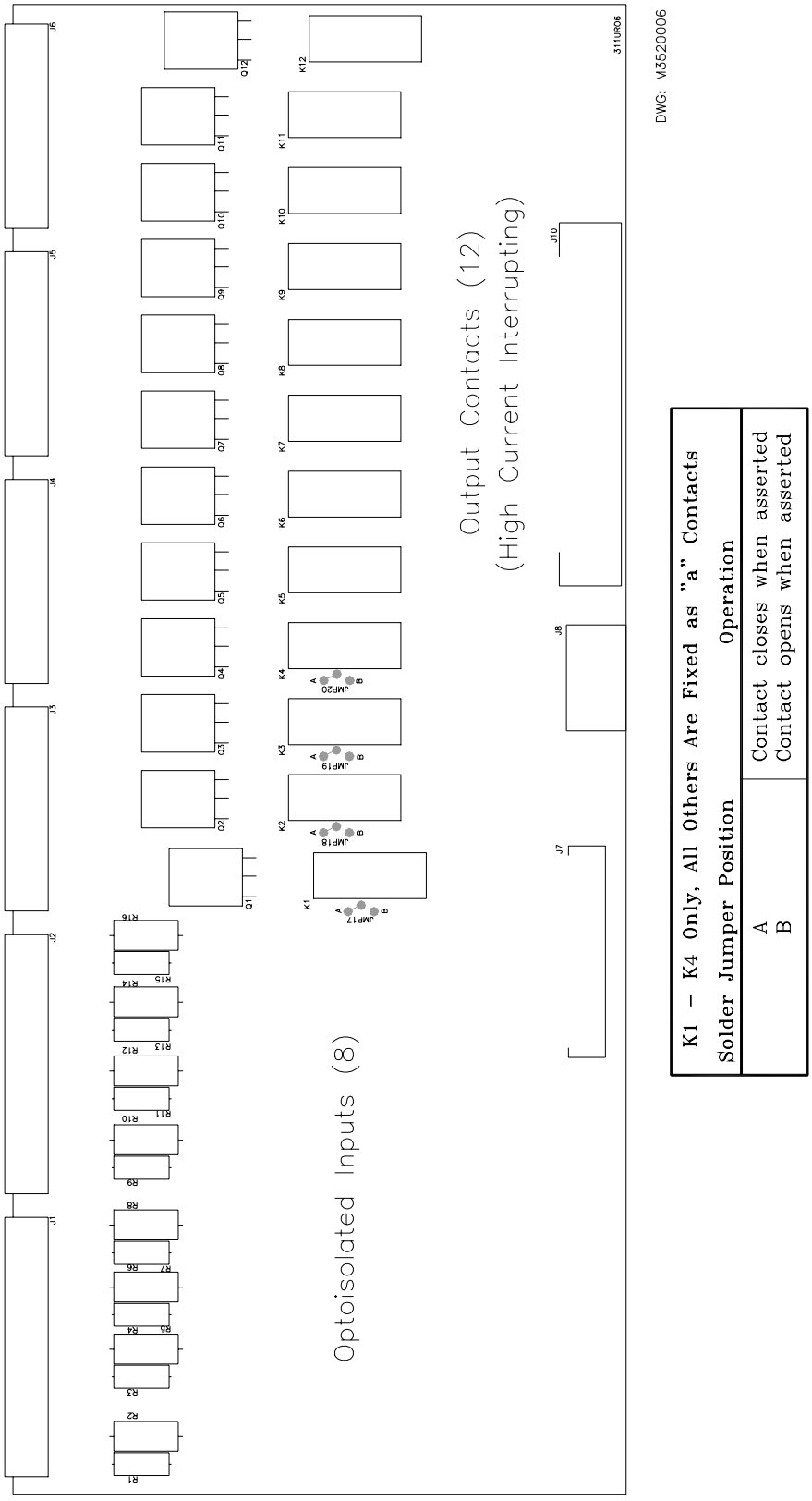


Figure 2.34: Interface Board 6 Component Layout (Plug-In Connector Version)

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SECTION 3: BREAKER LOGIC

INTRODUCTION

The predefined logic schemes of the SEL-352 Relay provide protection for several circuit breaker (CB) failure modes:

- Failure to clear a fault (five available schemes for fault current conditions)
- Failure to trip under load (load current conditions)
- Failure to complete trip sequence due to trip resistor(s) or close resistor(s) remaining inserted (thermal protection of close and trip resistors)
- Failure to close (current unbalance)
- Failure while open (flashover conditions)
- Loss-of-dielectric pressure
- Failure of the breaker 52A contact to indicate operation (breaker alarm logic)

Each of the protection schemes is implemented in SELOGIC® control equations, giving relay engineers unparalleled flexibility in adapting the relay to their needs. This flexibility is simplified by selecting the predefined schemes. Set the scheme setting to CUSTOM to make changes to the predefined logic.

BREAKER FAILURE RELAYING OVERVIEW

Ideally, when a fault occurs on a power system, the primary protection for the system operates to remove the faulted equipment from service. Zones of protection are arranged to minimize service disruption when local primary protection operates. When local protection fails to clear a fault, backup protection clears the fault, sometimes removing more equipment from service than the primary protection would have during correct operation.

Both local and remote backup protection are available to the system protection engineer. Remote backup consists of overlapping, time-coordinated protection zones, which can operate if a fault outside the instantaneous protection zone persists. Local backup protection uses redundant equipment, which operates to clear a fault if primary protection fails. The extent of redundancy depends on the availability of resources, the overall system impact, and the importance of the load.

Breaker failure relaying is one form of local backup protection. Consider using breaker failure relaying instead of remote backup if any of the following conditions are true:

- Remote backup fault clearing time is greater than maximum allowed fault clearing time due to system stability or equipment damage considerations.
- Critical loads are lost due to remote fault clearing, which can be maintained using local breaker failure relaying.
- Remote fault clearing is sequential, requiring the local fault contribution to be cleared before remote relaying can detect the fault.

If the breaker fails to clear a fault, all electrically adjacent breakers must open. Opening these adjacent breakers stops a continuing fault and interrupts current flow in the failed breaker. Figure 3.1 shows a basic breaker failure scheme. TRIPA, TRIPB, and TRIPC are used as the breaker failure initiate inputs from the local primary and backup protection. The 50 overcurrent element is set to pick up for specific current levels. For high fault current levels, the 50 element should be immune to dc and reset quickly when the protected breaker opens. For lower current levels, the 50 element should be secure, immune to dc and exponentially decaying ramp currents. When the timer expires, it closes an output contact to energize the 86 lockout relay, which initiates local tripping of all electrically adjacent breakers. Optionally, the 86 lockout relay can initiate transfer tripping to clear electrically adjacent remote breakers.

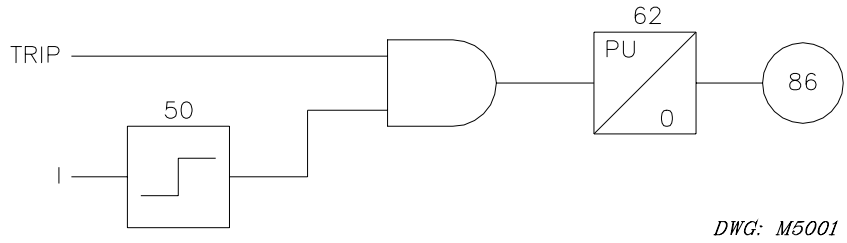

Figure 3.1: Basic Breaker Failure Protection Scheme

Time delay selection is important. Figure 3.2 illustrates the timing of the basic breaker failure scheme. Calculate an absolute maximum fault clearing time based upon system stability and equipment I^2t withstand considerations. In the event of a breaker failure, total time to clear all electrically adjacent breakers must be less than this absolute maximum. The 62 timer pick up delay should be set to allow time for the protected breaker to operate and the 50 element to reset. Also, a short safety margin should be added. The amount of time available for a safety margin is limited by the operating time of the protective relays and the local and remote breakers.

When the failed breaker is isolated by disconnect switches or when a breaker is removed from service for maintenance and testing, the breaker failure scheme should be disabled. This prevents inadvertent tripping of other breakers in service.

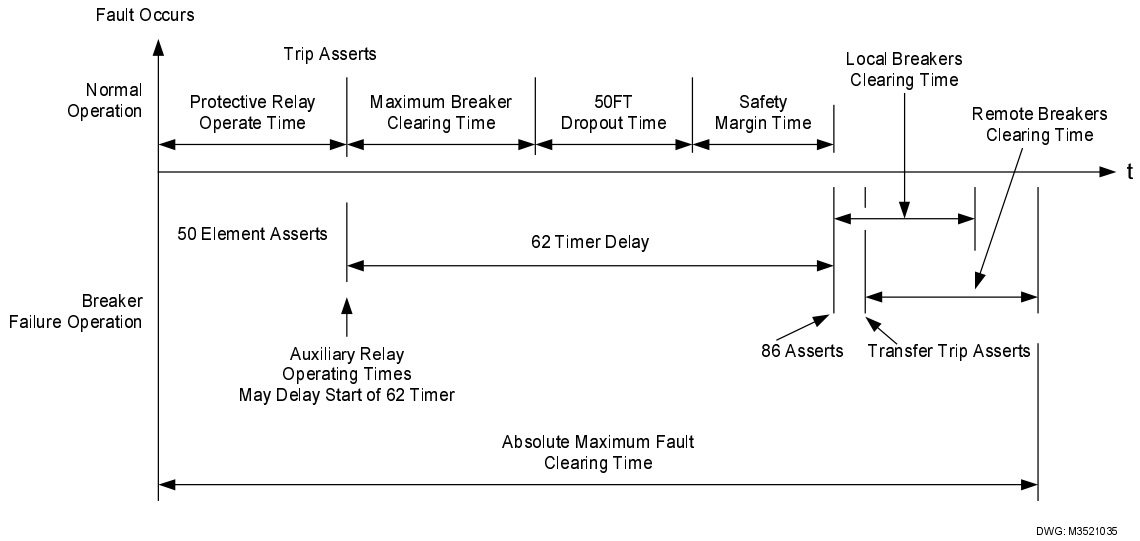

Figure 3.2: Basic Breaker Failure Scheme Timing

In ring-bus and breaker-and-a-half installations, two circuit breakers must operate to interrupt the fault current. Current distribution between the two breakers is unknown until the first breaker opens. A single breaker may initially carry the bulk of the fault current. Both breakers receive the trip signal at the same time and are expected to operate at the same time, but the 50FT element associated with the low current breaker may not assert until the other breaker opens. Figure 3.3 illustrates this idea, showing the current flow if Breaker 2 fails. This causes an uncertainty with respect to the timing of 50FT element assertion. This uncertainty is absent in a single breaker arrangement. Timing uncertainty is accounted for in the SEL-352 Relay breaker protection schemes intended for these complex bus/breaker arrangements. The SEL-352 Relay is intended to protect a single breaker, regardless of the bus/breaker arrangement. In breaker-and-a-half and ring-bus arrangements, you must use an independent breaker failure relay for each breaker.

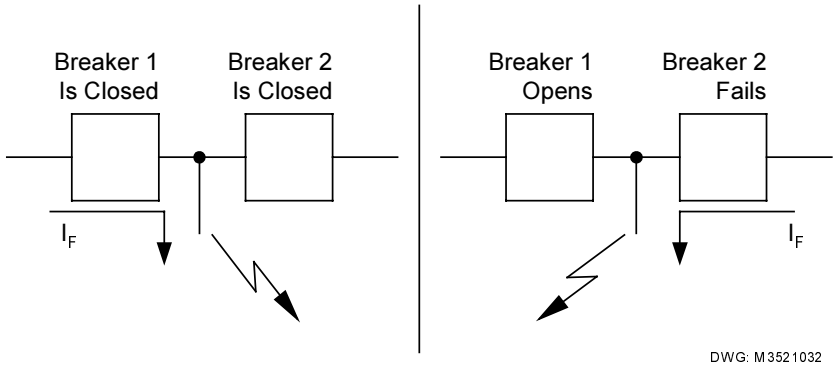

Figure 3.3: Breaker Failure in a Complex Bus/Breaker Arrangement

AVAILABLE AC CONNECTIONS

Simple breaker failure protection can be provided by monitoring only current, but the SEL-352 Relay has six ac voltage inputs for monitoring all three phases on each side of the breaker. These six voltage inputs and the three current inputs provide complete breaker failure protection, control, and monitoring.

The thermal logic designed to monitor the trip and close resistors of breakers is the only logic that requires the second set of voltage connections, but much of the relay logic is enhanced if both are connected.

Figure 3.4 shows a single-phase connection diagram of all nine ac inputs to the relay.

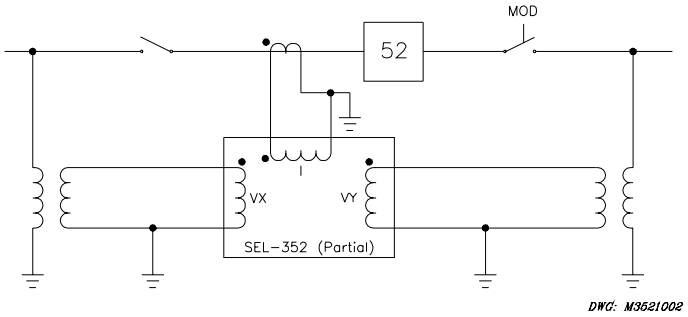

Figure 3.4: Single-Phase Diagram of AC Inputs to the Relay

Apply current to the relay from current transformers on each phase of the protected breaker. Apply voltage to the relay from potential transformers on each side of each phase of the breaker. The relay calculates voltage drop across each phase of the breaker by measuring each voltage input and comparing these on a per-phase basis.

The SEL-352 Relay has voltage nulling logic to compensate for steady-state unbalance between the voltage sources. If you do not use the voltage-based breaker protection feature, you do not need to connect the voltage inputs.

EXAMPLE BREAKER SPECIFICATIONS

Figure 3.4 shows an example breaker arrangement. Table 3.1 lists pertinent breaker, line, and system information that will be used to describe an application of the SEL-352 Relay for breaker failure protection.

Table 3.1: Example Line/Breaker Information

System Per-Unit Bases:	525 kV; 100 MVA; 2756 Ω; 110.0 A
Line length:	100 miles
Line impedances:	Z1 = Z2 = 0.0218 pu
	Z0 = 0.0758 pu
Source impedances:	ZS1 = 0.0034 pu
	ZS0 = 0.0055 pu
Single- or three-pole tripping and closing.	
Zone 1, three-phase minimum fault duty:	I_{3ph} = 49.6 pu = 5456 A
Line-charging current:	I_c = 350 A
CTR:	3000/5 (600/1)
PTR:	4300/1
Breaker:	500 kV, 3000 A, 3800 MVA
Maximum trip time:	33 ms
Nominal close time:	66 ms
Close resistors:	35 Ω/column, 2 columns
Trip resistors:	110 Ω/column, 2 columns
Transfer trip channel time:	0.5 cycle

The protection scheme in this example protects the breaker for all failures to trip. When fault current exceeds the minimum three-phase fault duty for a Zone 1 fault, the fault must clear in 8.5 cycles or less. All other trips must clear within 10 cycles. Because the protected breaker has trip and close resistors, and three-phase potentials are available on both sides of the breaker, the example uses the SEL-352 Relay trip and close resistor thermal protection schemes. Breaker closure and flashover failures are covered.

FAULT CURRENT CONDITIONS

Application Description

The SEL-352 Relay provides five different protection schemes to detect the failure of the circuit breaker to clear a fault. While the schemes share elements and timers, each is independent. Enable a fault current protection scheme or customize the logic. The SEL-352 Relay applies the single chosen scheme to all three breaker poles.

The difference among the schemes is the implementation of timers and latches that define the breaker failure scheme.

Schemes 2 and 3 are intended for single-breaker applications and Schemes 1, 4, and 5 are intended for multiple-breaker applications, although any of the schemes can be used in either single-breaker or multiple-breaker applications. Use Table 3.2 to help select the scheme that best fits your application. All five schemes are applicable to single-pole trip installations.

Table 3.2: Breaker Failure Scheme Selection

Breakers	Pulsed Trip Inputs	Breaker Failure Timer Reset By:	Scheme
Single	No	50FT or TRIP Dropout	3
Single	Yes	50FT Dropout	2
Multiple	No	50FT or TRIP Dropout	5
Multiple	Yes	Timer	4
Multiple	Yes	50FT Dropout	1

Operating Characteristic

Figure 3.5, through Figure 3.14 show logic diagrams for A-phase logic only. In each case, B-phase and C-phase logic are identical in form, using the respective phase trip inputs, timers, and overcurrent elements.

Special logic has been implemented in these five schemes to improve the speed of these schemes by detecting CT subsidence current. This logic is discussed below.

Select scheme timer settings based on the following factors:

- Maximum permissible fault duration
- Protective relay operating time

- Protected breaker operating time
- 50FT element dropout time
- Operating times of electrically adjacent breakers
- Desired breaker failure operating safety margin

If an auxiliary interposing relay is used between the protective relay trip output and the breaker fail initiate (TRIPA, TRIPB, TRIPC) input to the SEL-352 Relay, you must also account for the operating time of the auxiliary relay. Be aware that different models of auxiliary relays have a wide variety of operating times. Most scheme operating considerations are listed in Table 3.2. Additional timing considerations and recommended settings are listed below by scheme number.

Subsidence Current Logic

In schemes for detecting breaker failure to clear a fault, it is important to be able to detect as quickly as possible not only the pickup but the dropout of fault-detecting overcurrent elements. Half-cosine filtering is used to accelerate this detection of element pickup and dropout. However, the dropout detection can be delayed by a phenomenon called CT subsidence current. This current may appear as a small exponentially decaying dc current with a fairly long time constant. The effect of this current upon the half-cosine filter may be to create artificial phasor magnitudes large enough to prevent proper detection that the primary ac current actually has been interrupted. This failure to detect interruption of the primary ac current may delay detection of overcurrent element dropout by some fraction of a cycle. As a result, longer time coordination intervals must be used in the breaker failure logic to preserve security. The SEL-352 Relay employs an innovative logic for detecting the presence of subsidence current, thereby speeding the detection of overcurrent element dropout. The logic is shown in Figure 3.5, for A-phase current. B-phase and C-phase logic schemes are similar.

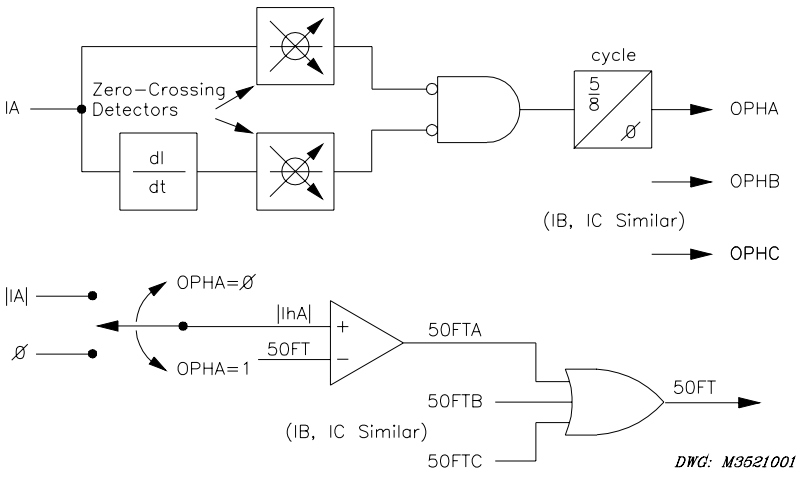

Figure 3.5: Subsidence Current Logic

In the upper drawing, the raw ac input current IA and the first derivative of IA are examined for zero crossings. The logical outputs of the two zero-crossing detectors are inverted and passed through an AND gate to a timer with a 5/8-cycle pickup time. With normal ac current flowing as IA, there are sufficient zero-crossing detections that the output of the AND gate never stays at logical 1 long enough to pick up the timer. Therefore, the internal control bit OPHA (A-phase open) stays at logical 0. In the lower drawing, with OPHA = 0, the "switch" causes the

magnitude of the half-cosine filtered IA to equal the value for |IhA|. The overcurrent element 50FTA compares |IhA| to the pickup setting 50FT. If |IhA| is greater than 50FT, the element is picked up and Relay Word bit 50FTA asserts; if |IhA| is less than 50FT, the element is dropped out and 50FTA deasserts.

When the primary ac current is interrupted, the CT secondary current IA in the upper drawing can take on a decaying dc exponential form, the subsidence current. Here, the zero-crossing detectors are likely to see few or no crossings. The output of the AND gate will now persist longer than the 5/8-cycle timer pickup value, so setting OPHA = 1. In the lower drawing, with OPHA = 1, the "switch" causes |IhA| to be set to zero, rather than to the calculated magnitude of IA. This setting of |IhA| to zero causes immediate dropout of the 50FTA element. Had |IhA| remained equal to |IA|, the detection of dropout may have been delayed considerably. Thus, the subsidence current detection logic, by sensing the presence of the exponential dc current, forces the overcurrent element to drop out sooner and permits faster breaker failure timing margins.

While the subsidence current detection logic operates nominally in about 5/8 cycle, processing latency could, in the worst case, stretch the 50FT dropout time to 3/4 cycle.

Scheme 1 (Fault Current)

Consider reading about Scheme 5 and then Scheme 4 before Scheme 1. These schemes are easier to understand than Scheme 1.

Scheme 1 (FTLOG=1) provides breaker failure protection for breaker-and-a-half and ring-bus breaker applications; it also can be used for single-breaker applications. This scheme adds a set/reset latch, a rising edge latch and dropout timer, and other logic to the logic of Scheme 5 to allow for a pulsed trip input. The 62TT timer latches the trip input for time TTdo when the input is asserted for a quarter-cycle. The 62FC breaker failure timer resets when both the 62TT timer dropout time (TTdo) expires and the 50FT element drops out. This timing scheme provides consistent breaker failure clearing times between adjacent breakers. This logic is necessary in multiple breaker applications because the fault current may be below the fault current threshold for one breaker until the adjacent breaker clears.

To understand the operation of the Scheme 1 logic, review two possible scenarios:

1) The 50FTA element asserts before the TRIPA input asserts.

2) The TRIPA input asserts before the 50FTA element asserts.

---

1) If the 50FTA element picks up before TRIPA assertion, the 62FC timer starts when the TRIPA input asserts. The 62FC timer continues to time until 50FTA drops out and the 62TT timer expires. If the 62FC timer expires, the FBF bit in the Relay Word asserts.

2) In ring-bus and breaker-and-a-half installations, the TRIPA input can assert before the 50FT overcurrent element picks up. If the TRIPA input asserts before the 50FT element picks up, the 62TT timer output asserts and the 62FC timer starts. The 62TT timer output remains asserted for TTdo time. The 62FC timer continues to time until the 62TT timer has expired and the 50FTA overcurrent element drops out. If the 50FTA element picks up and remains asserted until 62FC expires, the FBF bit in the Relay Word asserts.

In both cases, the LFA latch latches the 62FC timer. After the 62FC timer latches, trip signal dropout does not affect the breaker fail protection scheme.

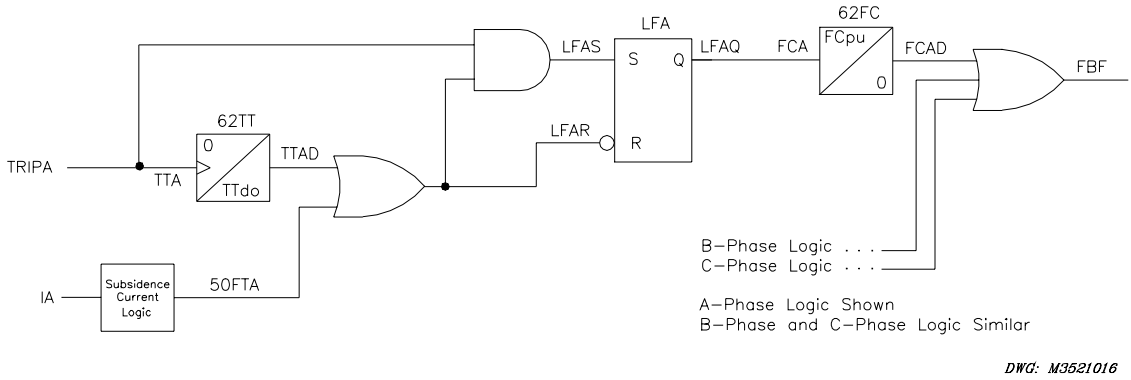

Figure 3.6: A-Phase Failure to Trip for Fault Logic, Scheme 1

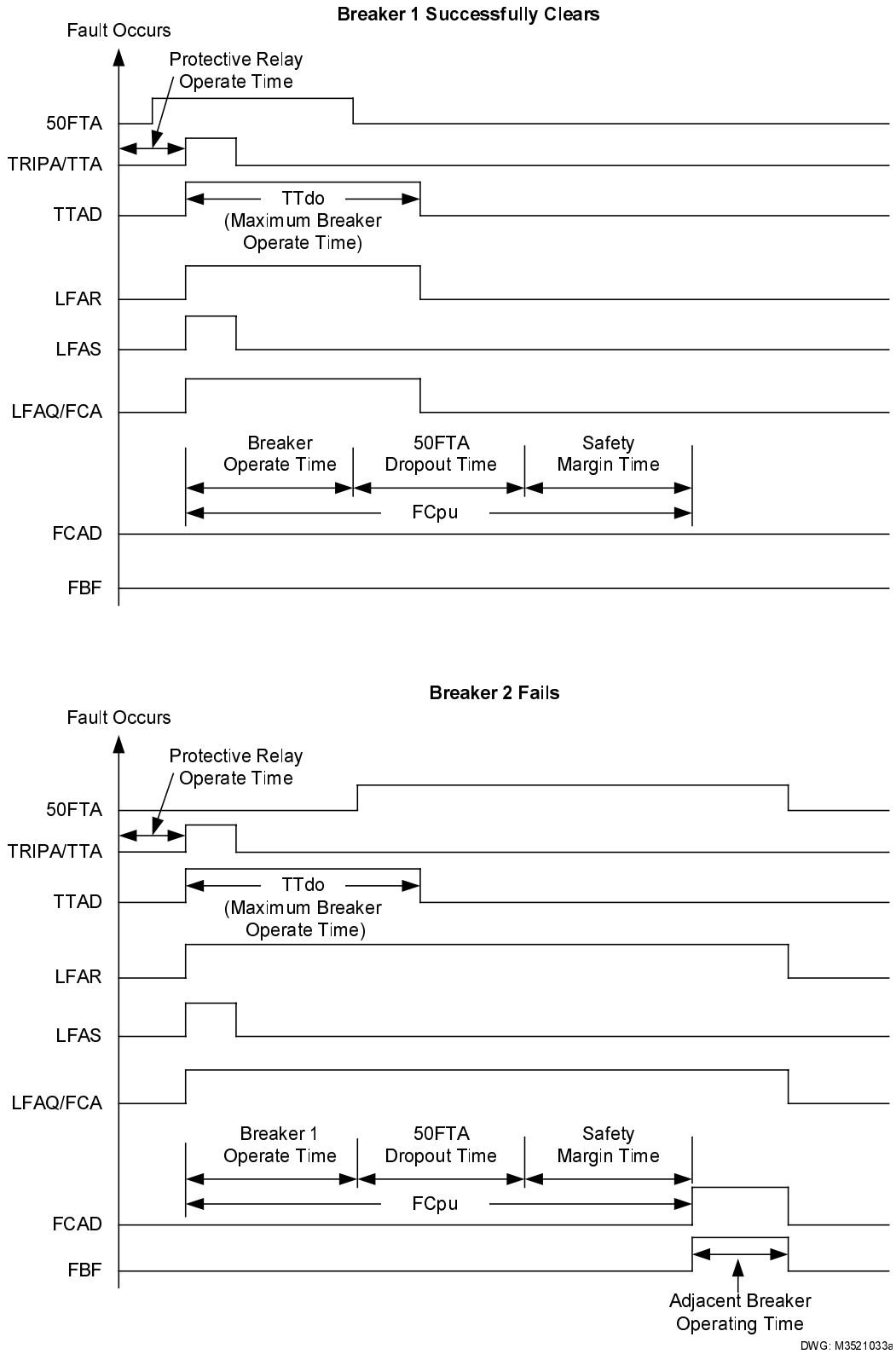

Figure 3.7: Scheme 1 Breaker Failure Timing

Scheme 2 (Fault Current)

Scheme 2 (FTLOG=2) provides breaker failure protection logic for single-breaker applications. It may also be used for multiple-breaker applications where sequential/delayed tripping is acceptable due to current distribution. This scheme adds a set/reset latch to the Scheme 3 logic to allow for a pulsed trip input. LFA latches when TRIPA and 50FTA are both asserted for a quarter-cycle. It resets when 50FTA deaaserts. The 62FC timer starts after LFA is set and continues to time until 50FT resets LFA or FCpu times out.

The logic shown in Figure 3.8 protects the system from a breaker failure during a fault. This scheme is applicable to single breaker configurations. In a single breaker arrangement, fault current causes the 50FTA element to assert immediately following fault inception and just prior to TRIPA input assertion. If 50FTA is asserted when the relay receives the TRIPA input, the 62FC timer starts and latches. At this point, trip signal dropout does not affect the breaker failure scheme. If the 50FTA element remains asserted until the 62FC timer expires, the Relay Word FBF bit asserts. If the breaker operates successfully, the 50FTA element drops out before the 62FC timer expires, and FBF does not assert.

Although it is very simple and effective in single breaker arrangements, Scheme 2 is not recommended when the protected breaker is part of a ring-bus or breaker-and-a-half installation. Consider using Scheme 1, Scheme 4, or Scheme 5 in such breaker arrangements.

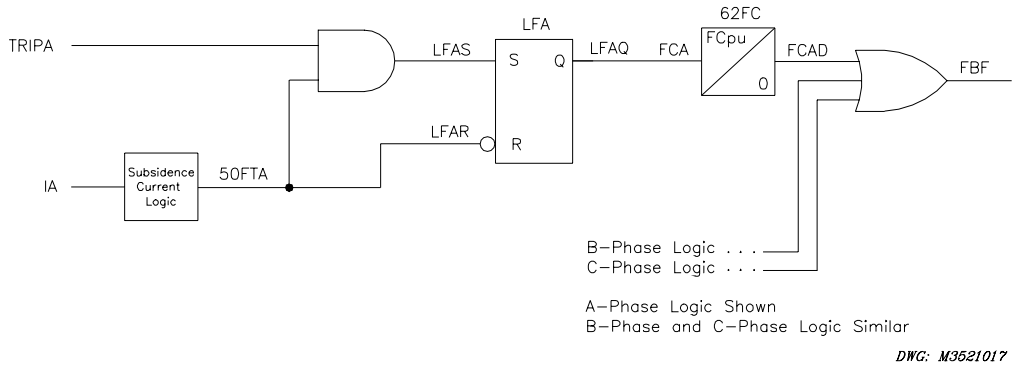

Figure 3.8: A-Phase Failure to Trip for Fault Logic, Scheme 2

Figure 3.9 depicts the breaker failure condition that results when 62FC times out.

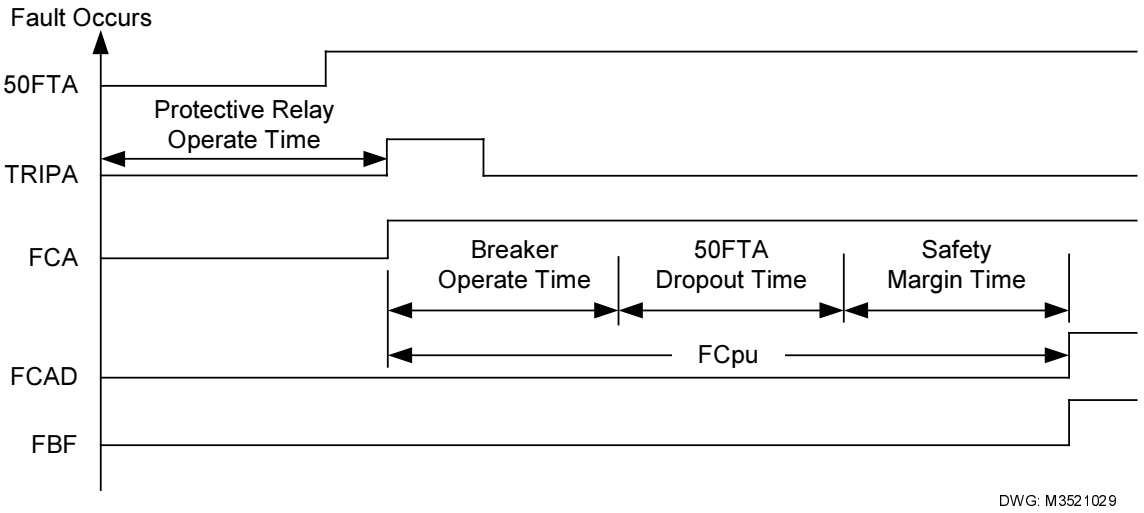

Figure 3.9: Scheme 2 Breaker Failure Timing

Scheme 3 (Fault Current)

Scheme 3 (FTLOG=3) provides breaker failure protection logic for single-breaker applications. It also may be used for multiple-breaker applications where sequential/delayed tripping is acceptable. This scheme requires the continuous assertion of both the 50FT fault current detector and the trip input to time for a breaker failure.

The logic shown in Figure 3.10 protects the system from a breaker failure during a fault. This scheme is applicable to single breaker configurations. When a fault occurs, 50FTA asserts, and the protective relay asserts the relay TRIPA input. The AND gate output goes high, and the 62FC timer starts. If the TRIPA input and 50FTA element remain asserted until 62FC expires, Relay Word bit FBF asserts.

In Scheme 3, the trip input must remain asserted while current flows in the protected breaker. Scheme 3 resets when either the TRIPA input deasserts or the 50FTA element drops out.

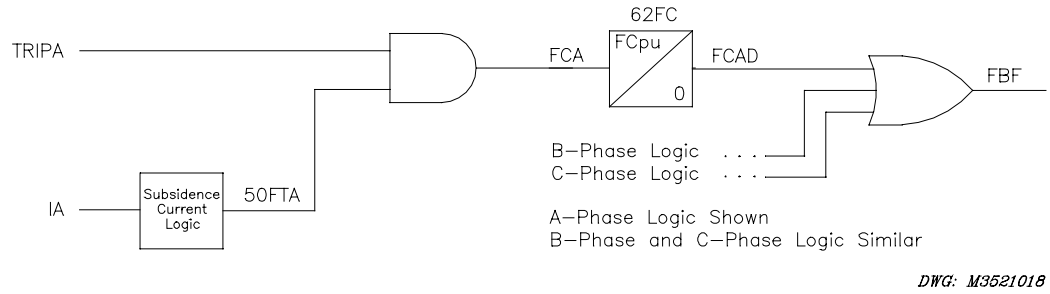

Figure 3.10: A-Phase Failure to Trip for Fault Logic, Scheme 3

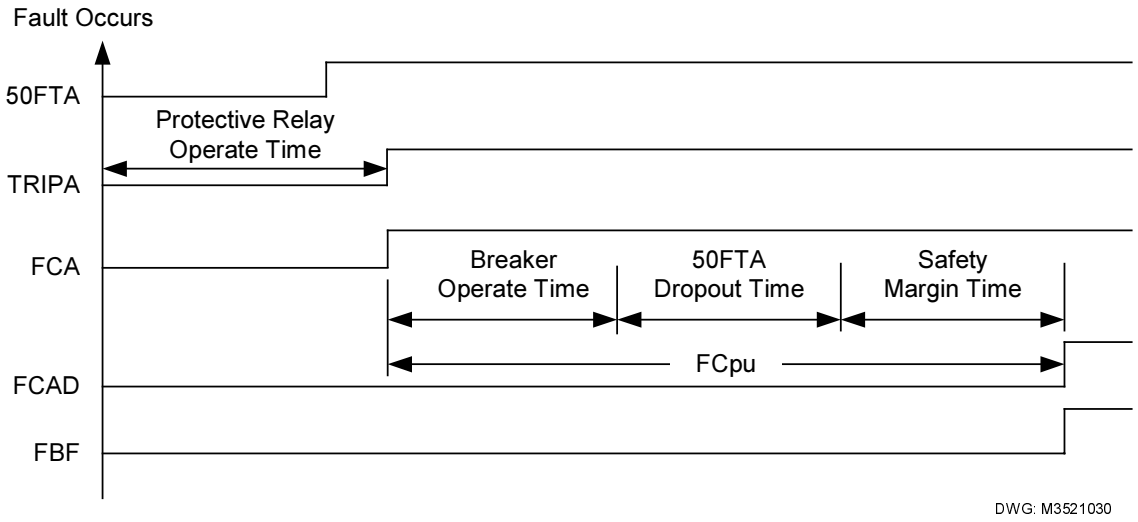

Figure 3.11: Scheme 3 Breaker Failure Timing

Scheme 4 (Fault Current)

Scheme 4 (FTLOG=4) provides breaker failure protection for breaker-and-a-half and ring-bus breaker applications. The scheme also can be used for single-breaker applications. This scheme adds a latch and dropout timer to the pickup timer (represented by a single symbol) of Scheme 5 to allow for a pulsed trip input. The 62TT timer latches the trip input when the TRIPA input asserts for at least a quarter-cycle. The 62TT timer output (TTAD) remains deasserted for time TTpu, after which it asserts for time TTdo. Relay Word bit FBF asserts if 50FTA asserts while the 62TT timer output is asserted. The 62TT breaker failure timer resets when the 62TT timer dropout time (TTdo) expires. This timing scheme provides consistent breaker failure clearing times between adjacent breakers. This logic is necessary in multiple-breaker applications because the fault current may be below the fault current threshold for one breaker until the adjacent breaker clears.

The Scheme 4 logic, shown in Figure 3.12, protects the system from a breaker failure during a fault. This scheme is applicable to single breaker, ring-bus, and breaker-and-a-half bus configurations.

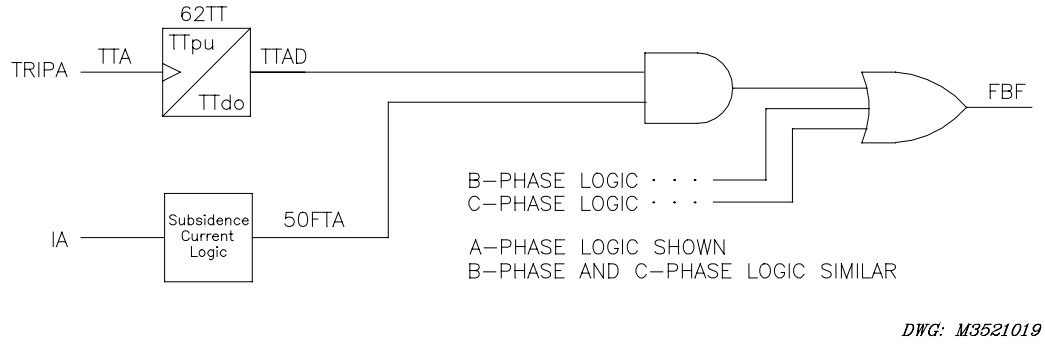

Figure 3.12: A-Phase Failure to Trip for Fault Logic, Scheme 4

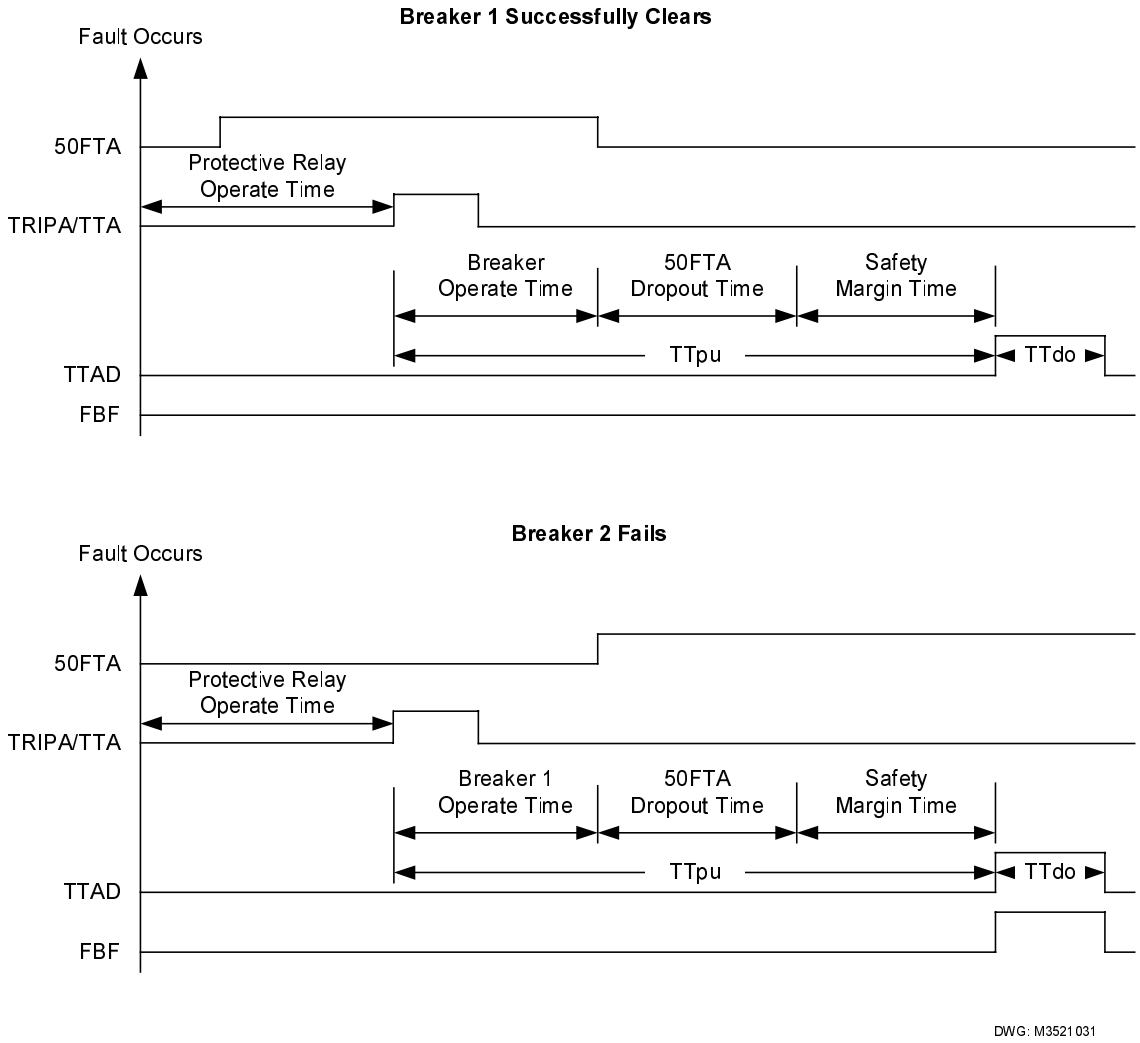

Figure 3.13: Scheme 4 Breaker Failure Timing

Scheme 5 (Fault Current)

Scheme 5 (FTLOG=5) provides breaker failure protection for breaker-and-a-half and ring-bus breaker applications. The scheme also can be used for single-breaker applications. The 62FC timer starts as soon as the trip input asserts to provide consistent breaker failure clearing times between adjacent breakers. This logic is necessary in multiple-breaker applications because the fault current may be below the fault current threshold for one breaker until the adjacent breaker clears.

The logic shown in Figure 3.14 protects the system from a breaker failure during a fault. Scheme 5 is intended for use in single breaker, breaker-and-a-half, and ring-bus arrangements.

When the TRIPA input is asserted, the 62FC timer starts. If 50FTA is asserted when the 62FC timer expires, the Relay Word FBF bit asserts. If the TRIPA input is deasserted or the 50FTA element drops out before 62FC expires, the logic resets and FBF does not assert.

This scheme is similar to Scheme 3 because the TRIPA input must remain asserted while current still flows in the protected breaker.

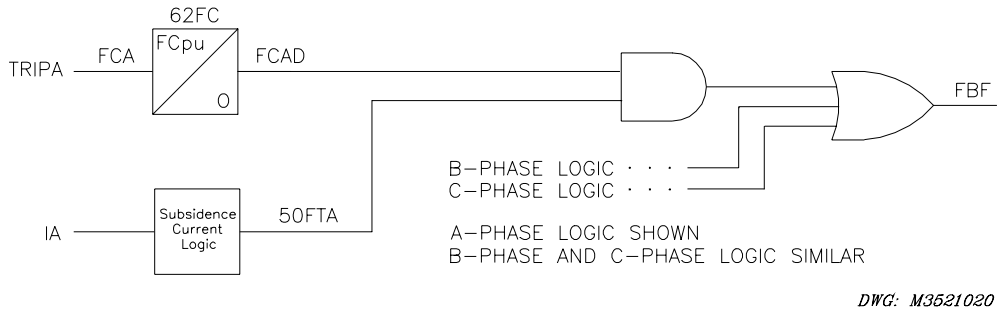

Figure 3.14: A-Phase Failure to Trip for Fault Logic, Scheme 5

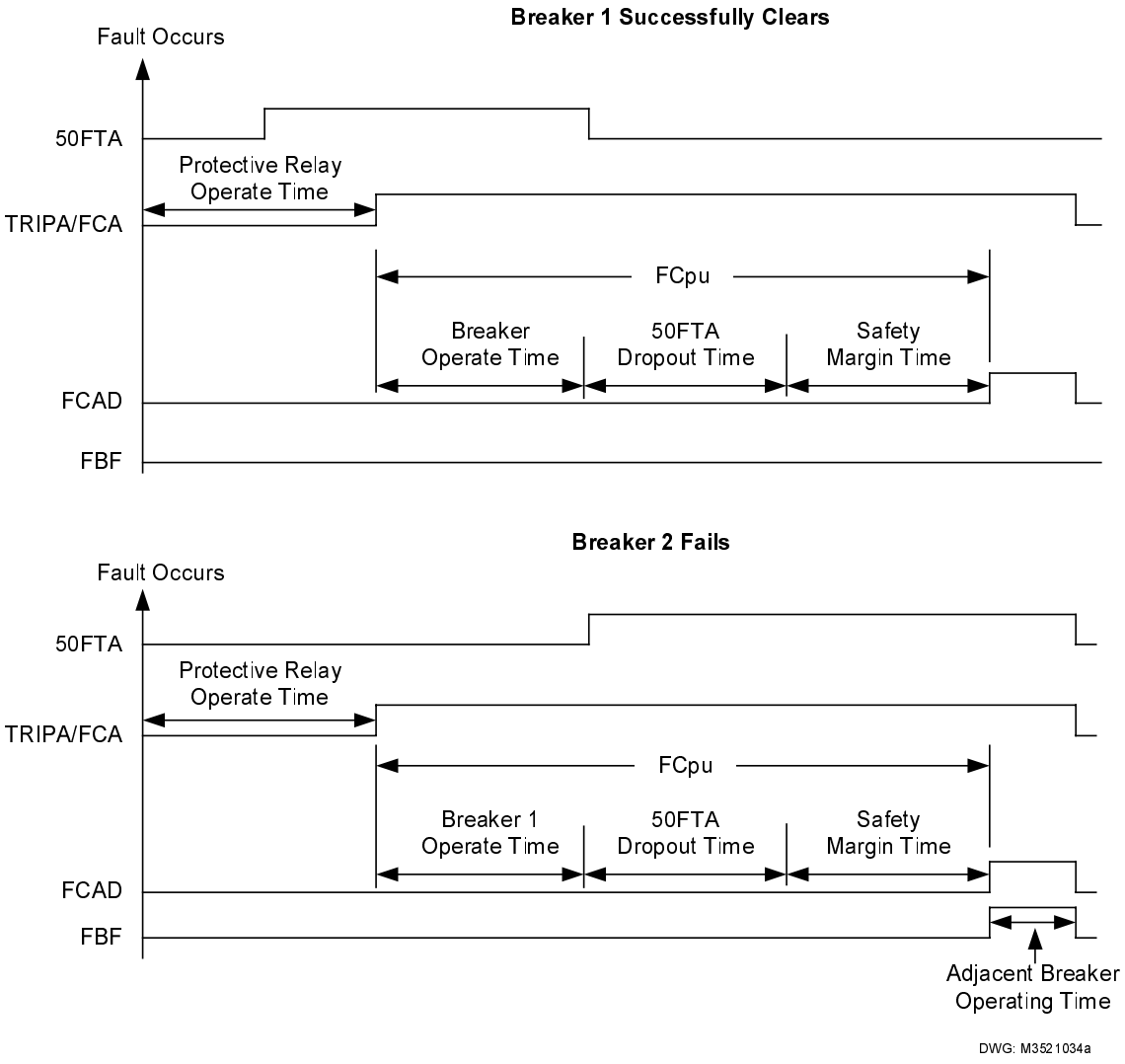

Figure 3.15: Scheme 5 Breaker Failure Timing

Setting Description

Trip Inputs (TRIPA, TRIPB, TRIPC)

Use **SET G <ENTER>** to associate the breaker failure initiate logic inputs (TRIPA, TRIPB, TRIPC) with physical inputs.

Any optoisolated input can be used to control the logic inputs. For example, if IN101 is used to initiate an A-phase breaker fail condition from the protective relay, set TRIPA = IN101. Repeat this for each trip input. The same input may be used for all three trip input conditions if single-pole tripping is not used. The trip input settings are actually SELOGIC control equations. Use any combination of Relay Word bits according to the SELOGIC control equation criterion in ***Section 5: Control Logic***.

Fault Detector (50FT)

Range: 0.50–45.00 A in 0.01-A steps (5 A)
0.10–9.00 A in 0.01-A steps (1 A)

Use **SET <ENTER>** to access the 50FT setting, needed for all fault condition breaker failure schemes. This setting selection is based on the minimum fault current for which the scheme must operate. The fault current logic operates each time the breaker is called on to trip phase current greater than the 50FT setting. Note that the 50FT setting for Scheme 4 must be greater than the maximum load current. The 50FT element is the only overcurrent element that includes the subsidence current logic discussed earlier in this section.

The SEL-352 Relay does not discriminate between phase faults and ground faults. Fault discrimination is based strictly on phase current magnitude. Breaker operations for ground faults with current duties above the 50FT setting are protected under the failure-to-break fault current logic. A separate 50N fault detector is available for customizing your scheme.

RMS Overcurrent (50RMS) (SEL-352-2 Relay)

Range: 0.50–45.00 A in 0.10-A steps
0.10–9.00 A in 0.02-A steps

Use the 50RA, 50RB, 50RC, or 50R elements to detect an RMS overcurrent condition on a per-pole or three-phase basis. The 50R elements can be used to block tripping when the RMS current exceeds some percentage of the maximum interrupt rating for the breaker. You may then transfer the trip to adjacent breakers with higher fault duty.

Set 50RMS to the value at which the element should pick up. See Figure 3.16. This feature is only available in the SEL-352-2 Relay.

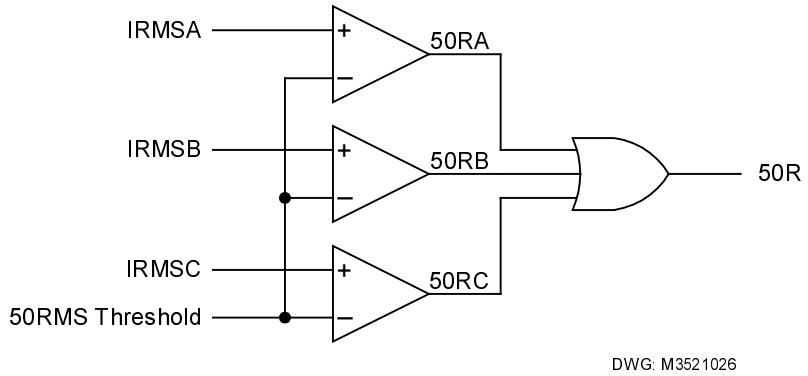

Figure 3.16: RMS Overcurrent Condition Detection

Fault Current Logic Enable (FTLOG)

Range: OFF, 1–5, CUSTOM

Use **SET <ENTER>** to access the FTLOG setting. Enable one of five schemes, select custom, or disable fault current breaker failure protection.

Set FTLOG = OFF if you do not want fault current breaker failure protection. If you need logic for your application different from that provided by any one of the five schemes, set FTLOG = CUSTOM. When you select CUSTOM, all fault current settings are shown including the SELOGIC control equations. Modify these settings to meet your specific application needs.

Fault Clearing Pickup Time (FCpu)–Schemes 1, 2, 3, and 5

Range: 0–8191 cycles in 1/8-cycle steps

Use **SET <ENTER>** to access the fault clearing pickup setting (FCpu). This setting determines the time delay before the 62FC timer expires and asserts the FCAD timer output.

The recommended setting for FCpu is the nominal breaker operate time, plus the 50FT dropout time, plus a safety margin.

Trip Timer Pickup Time (TTpu)–Scheme 4

Range: 0–8191 cycles in 1/8-cycle steps

Use **SET <ENTER>** to access this setting. It determines the time delay before the 62TT timer expires and asserts the TTAD timer output.

The recommended setting for TTpu is the nominal breaker operate time, plus the 50FT dropout time, plus a safety margin.

Trip Timer Dropout Time (TTdo)–Scheme 1

Range: 0–8191 cycles in 1/8-cycle steps

Use **SET <ENTER>** to access this setting. The TTdo setting controls the assertion time of the 62TT timer output (TTAD). During this time, the breaker failure logic cannot be reset.

Set TTdo longer than the maximum breaker operate time but at least one cycle less than the FCpu setting. The TTdo setting should be similar to your SlowTr setting. A recommended TTdo setting is 125 percent to 150 percent of the nominal breaker operating time if manufacturer data are not available.

Setting TTdo longer than the maximum breaker operate time ensures that 62FC does not reset before assertion of the fault current detector after an adjacent breaker clears in a multiple breaker application. When two breakers serve one piece of equipment, the fault current detector (50FT) may only pick up on one breaker. Once that breaker trips, the other breaker fault current detector will pick up.

Setting TTdo at least one cycle behind the FCpu setting ensures that 62FC has an opportunity to reset if there is no breaker failure.

Trip Timer Dropout Time (TTdo)–Scheme 4

Range: 0–8191 cycles in 1/8-cycle steps

Use **SET <ENTER>** to access this setting. It determines the duration of FBF assertion and, therefore, the duration of the trip output to your lockout relay.

Set the TTdo timer to one cycle or longer.

Setting Calculations

This section contains setting calculations for an example SEL-352 Relay breaker failure application for fault current conditions. Only settings necessary for this specific application are referenced. Note that you will need different settings for different scheme selections. Please select relay settings appropriate to your application. Refer to ***Section 7: Setting the Relay*** for a complete list of settings.

The output of the fault current breaker fail protection is the assertion of the FBF Relay Word bit. This bit must be used in control logic for energizing an external lockout relay. Refer to ***Lockout Relay Control*** in ***Section 4: Close Logic***.

Fault Detector (50FT)

For our example, system conditions necessitate clearing of Zone 1, three-phase faults by the fault current breaker protection scheme if the protected breaker fails.

When you select the 50FT element setting, account for fault study errors and then account for possible error in the current element measurement. By calculating the worst-case measurement error and subtracting that value from the relay setting, you ensure that the element operates for the current level your protection scheme specifies.

In the example, minimum Zone 1 three-phase fault duty after accounting for fault study errors, I_{3ph}, equals:

$$I_{3ph} = \frac{5456 \text{ A primary}}{600} = 9.09 \text{ A secondary}$$

The 50FT element accuracy specification for a nominal 5 A relay is ±0.025 A secondary ±5% of setting (±0.005 A ± 5% of setting for 1 A I_{nom}.) Thus, the worst-case error for a setting of 9.09 A secondary is:

$$\begin{aligned} \text{50FT error} &= 0.025 \text{ A} + \left(0.05\right) \cdot \left(9.09 \text{ A}\right) \\ &= 0.479 \text{ A secondary} \end{aligned}$$

To ensure that 50FT asserts for all Zone 1, three-phase faults, we set the 50FT element:

$$\begin{aligned} \text{50FT} &= 9.09 \text{ A} - 0.479 \text{ A} \\ &= 8.61 \text{ A secondary} \end{aligned}$$

Fault Logic Enable (FTLOG)

Select the best scheme for your application based on the bus configuration of the protected breaker, operating considerations listed, and timing requirements.

Because the example protected breaker is in a single-breaker installation, any of the five available schemes may be used. We selected Scheme 2 based on the simplicity of the scheme and the fact that the trip input may be deasserted once the breaker failure scheme initiates.

Fault Clearing Pickup Time (FCpu)

For the example application, all Zone 1, three-phase faults must clear within 8.5 cycles to maintain system stability. Thus, total fault clearing time (Tt) is 8.5 cycles. Nominal tripping time of local breakers (Tbl) and remote breakers (Tbr) is 2 cycles. Transfer trip channel time to the remote breaker (Tc) is 0.5 cycle. Operating time of the line protective relay (Tpr) for a 3-phase fault near the Zone 1 boundary is 2 cycles. Specified reset time of the 50FT overcurrent element T50 is less than 0.75 cycle. The FCpu time and safety margin (Ts) are calculated as follows:

$$Ts = Tt - (Tpr + Tbl + T50 + Tbr + Tc) \text{ cycles}$$

$$Ts = 8.5 - (2.0 + 2.0 + 0.75 + 2.0 + 0.5) \text{ cycles}$$

$$Ts = 1.25 \text{ cycles}$$

You can now use the following equation to calculate FCpu:

$$FCpu = Tbl + T50 + Ts = 4.0 \text{ cycles}$$

Note that auxiliary relay operate times are not separated from breaker operate times. If the high current interrupting output contacts are used to trip breakers directly, then you do not need to consider auxiliary relay operate times.

LOAD OR LINE-CHARGING CURRENT CONDITIONS

Application Description

Breaker failure protection during load conditions is completely independent from the fault current protection. Use this protection in addition to the fault current protection as a second level of breaker failure protection or by itself.

The output of the load current protection is the assertion of the LPF (pending failure) or LBF (breaker failure) Relay Word bit. These bits must be used in control logic for energizing an external alarm, retripping the breaker, or asserting a lockout relay. Refer to ***Lockout Relay Control*** in ***Section 4: Close Logic***.

The SEL-352 Relay provides two different protection schemes for failure of the breaker to interrupt load or line-charging current. While the schemes share elements and timers, each is independent. You may enable only one protection scheme at a time or customize the logic.

Both schemes require that the breaker is closed and that the relay receive a trip input. The two schemes differ in how they determine a closed breaker condition. Refer to ***Operating Characteristic*** for an operational description and logic diagram of each scheme. Setting considerations for each scheme follow.

Scheme 1 and Scheme 2 are essentially the same, except Scheme 2 adds logic that determines if a breaker has failed based on the 52A breaker status inputs. This scheme primarily is used when load or line-charging current is not high enough to pick up 50LD.

Operating Characteristic

Scheme 1 (Load Current)

Scheme 1, shown in Figure 3.17, determines a closed breaker condition by comparing the phase current with the 50LD setting. Because this logic is very sensitive, the trip input must be asserted for two consecutive quarter-cycles before this logic acknowledges the input. This feature provides the necessary security against incidental trip input assertions.

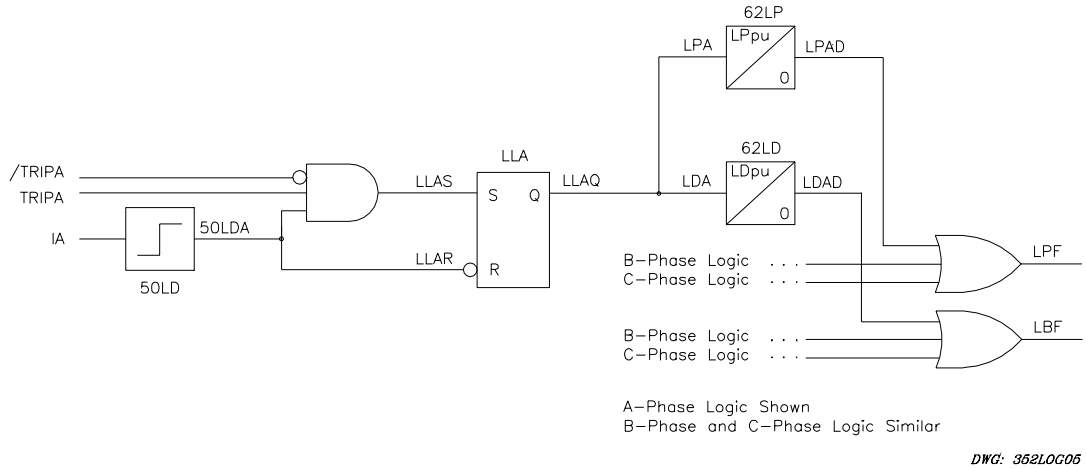

Figure 3.17: A-Phase Failure to Trip Load or Line-Charging Current Logic, Scheme 1

Scheme 2 (Load Current With 52a Backup)

If there are conditions under which the protected breaker could be called to trip, while current is below the 50LD overcurrent element setting, you may want to use Scheme 2. Scheme 2 (Figure 3.18) is identical to Scheme 1 (Figure 3.17), except that it adds 52A supervised breaker failure timers APpu and AFpu. An application where this function might be required is when the protected circuit breaker is connected to a generator-transformer unit.

In this instance, the circuit breaker could be issued a trip signal while the generator is idling. Under these conditions, current through the protected breaker is nearly zero. You can set the SEL-352 Relay to operate the 86 lockout relay if the relay 52A input is not deasserted after a settable time delay.

If any other breaker failure condition is detected based on assertion of the 86BFT bit, the 52A logic of Scheme 2 is disabled.

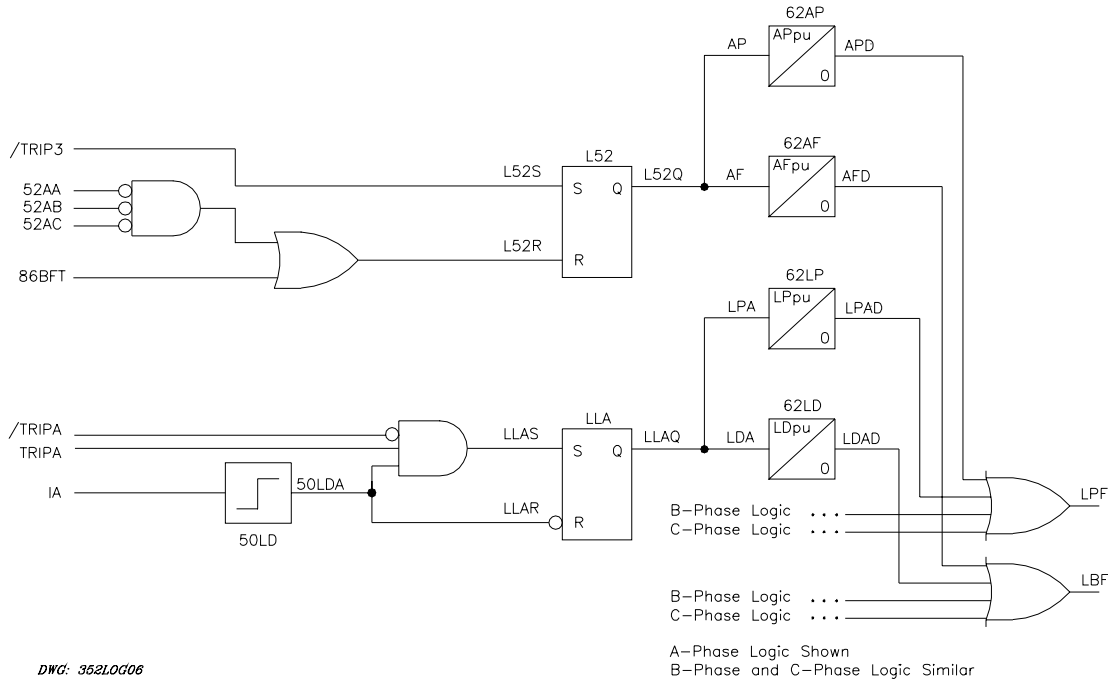

Figure 3.18: Failure to Trip Load or Line-Charging Current Logic, Scheme 2

Setting Description

Trip Inputs (TRIPA, TRIPB, TRIPC)

Use **SET G <ENTER>** to associate the breaker failure initiate logic inputs (TRIPA, TRIPB, TRIPC) with physical inputs. Both load current protection schemes use the three programmable inputs: TRIPA, TRIPB, and TRIPC.

Any optoisolated input can be used to control these Relay Word bits. For example, if IN101 is used to indicate an A-phase trip initiate from another relay, set TRIPA = IN101. If IN104 is used to indicate breaker status, set 52AA = IN104. Repeat this for each programmable input. The

same input may be used for all three conditions if single-pole tripping is not used. The programmable input settings are actually SELOGIC control equations. Use any combination of Relay Word bits according to the SELOGIC control equation criteria in ***Section 5: Control Logic***.

Breaker Status (52AA, 52AB, 52AC)

Scheme 2 also uses the three programmable inputs: 52AA, 52AB, and 52AC. Use **SET G <ENTER>** to associate these with physical inputs.

Load Detector (50LD)

Range: 0.10–45.00 A in 0.01-A steps (5 A)
0.02–9.00 A in 0.01-A steps (1 A)

Use **SET <ENTER>** to access the 50LD overcurrent element. This element is used in the failure-to-trip load current breaker protection scheme. The 50LD element should pick up when the protected breaker is closed. This scheme detects failures of the breaker to open when breaker current is lower than the 50FT setting, such as load-breaking operations.

If the protected breaker is in a ring-bus or breaker-and-a-half arrangement, set 50LD to pick up for line-charging current of the shortest line serviced by that breaker.

Charging current for a given line can be calculated using the following equation:

$$I_c = Vg \cdot Bc \text{ A primary}$$

where Vg is the line-to-ground voltage and Bc is the total line capacitive susceptance. Multiply the line capacitive susceptance by the line length if it is specified on a per-unit basis.

For the example application, line-charging current I_c is 350 A primary or 0.58 A secondary.

The 50LD element accuracy specification for a nominal 5 A relay is ±0.025 A secondary ±5% of setting (±0.005 ± 5% for I_{nom} of 1 A.) The error figure is calculated with the method used for 50FT. The maximum error for a setting of 0.58 A secondary is ±0.054 A secondary. To ensure that 50LD picks up any time the protected breaker is closed, the 50LD element should be less than the result of the following equation:

$$50LD = 0.58 \text{ A} - 0.054 \text{ A} = 0.53 \text{ A secondary}$$

The relay also uses the 50LD element in the flashover protection logic. If you intend to use the breaker pole flashover protection logic, please refer to the flashover logic descriptions before finalizing your 50LD setting selection.

When the protected breaker is part of a ring-bus or breaker-and-a-half installation, load current may be very low due to unequal current distribution between the two breakers. Failure-to-trip load current logic may still be used to protect the breaker. Because current application may be sequential, scheme timing is uncertain in ring-bus or breaker-and-a-half installations.

Ground Current Detector (50N)

Range: 0.10–45.00 A in 0.01-A steps (5 A)
0.02–9.00 A in 0.01-A steps (1 A)

The 50N ground current detector is not used in any of the default logic or scheme selections. It is available for custom applications. The 50N setting is compared against a calculated 3•I0, which is simply the vector sum of all three current inputs. Under balanced conditions, the result of this calculation is zero. Consider normal system unbalance when using this element. Some systems can have as much as 10 percent to 15 percent unbalance. As either load or the number of faults increases, so does the amount of unbalance calculated.

Set the 50N so that it will not pick up for normal operating conditions because of system unbalance. For detecting faults, a setting of 50 percent or less of the calculated ground current provides margin for differences in ground impedance.

Load Current Logic Enable (LDLOG)

Range: OFF, 1, 2, CUSTOM

Use **SET <ENTER>** to access the LDLOG setting. Enable, modify, or disable load current protection.

If you do not want load current protection, set LDLOG = OFF. If you need logic for your application different from that available with either of the two schemes, set LDLOG = CUSTOM. When CUSTOM is selected, all load current settings are shown including the SELOGIC control equations. Modify these settings to meet your specific application needs.

Load Current Timers (LPpu, LDpu)–Schemes 1 and 2

Range: 0–16383 cycles in 1/4-cycle steps

Use **SET <ENTER>** to access the LPpu and LDpu timers. These are breaker pending failure and failure timers, respectively, for the failure-to-trip load current breaker protection scheme.

The time delay of this protection scheme is typically set longer than fault current conditions due to lower current duties associated with this type of breaker failure operation. Extending the time delay allows more time for a slow but operative breaker to clear a low-current fault. A disadvantage in the extended time delay is that a fault does remain on longer if the breaker actually fails. You must weigh these considerations when selecting time delays for this scheme. Please note that some breakers actually take more time to break low amounts of current. Consult the manufacturer of the protected breaker for details.

The timing of this protection scheme is nearly identical to that of Scheme 2 of the fault current logic shown in Figure 3.9. The difference is that pending failure bit LPF is provided with this scheme. Consider using the LPF bit to retrip the protected breaker through a second trip coil.

The recommended setting for LDpu is the nominal breaker operate time, plus the 50FT dropout time, plus a safety margin. Calculate the safety margin by subtracting all conditions required to isolate the fault during a breaker failure condition from the maximum acceptable fault clearing time. The safety margin will be longer in this case than for the fault current logic because the total acceptable time to clear the fault at these lower fault duties is longer.

The LPpu setting value is based on the breaker operate time and the time calculated for LDpu. If using the LPpu to energize a second trip coil, the LPF bit should assert in enough time to let the breaker operate before tripping the lockout relay with the LBF bit. The recommended setting for LPpu is LDpu minus the nominal breaker operate time and some margin.

52A Pending Failure and Breaker Failure (APpu, AFpu)–Scheme 2

Range: 0–16383 cycles in 1/4-cycle steps

Use **SET <ENTER>** to access the APpu and AFpu timers. These are 52A supervised pending failure and breaker failure timers, respectively, for the failure-to-trip load current breaker protection scheme.

The time delay settings should be selected based on the maximum time permissible to operate the protected equipment under low- or zero-current conditions. A slightly larger safety margin should be considered for this logic than is allowed for the breaker failure timers described above. The longer safety margin can allow for possible differences in expected and actual breaker auxiliary contact operating times.

The recommended settings for APpu and AFpu are two cycles longer than the LPpu and LDpu respectively. The two cycles allow for a slow 52A response time.

Setting Calculations

Pending Failure and Breaker Failure (LPpu, LDpu)

In our example application, Scheme 1 is selected because our conditions do not require the 52A supervised breaker failure logic. Ten cycles are allowed to clear faults with current duties below 5456 A primary. Local and remote breaker operating times are considered identical to those used in selecting the FCpu setting. Operating time of line protective relay Tpr is two cycles. Specified reset time of the 50LD overcurrent element T50 is less than 1.55 cycles. Safety margin time is defined as Ts and calculated below.

$$Ts = Tt - (Tpr + Tbl + T50 + Tbr + Tc) \text{ cycles}$$

$$Ts = 10.0 - (2.0 + 2.0 + 1.55 + 2.0 + 0.5) \text{ cycles}$$

$$Ts = 1.95 \text{ cycles}$$

$$LDpu = Tbl + T50 + Ts = 5.5 \text{ cycles}$$

We set the pending failure timer LPpu to retrip the protected breaker more than two cycles before tripping the lockout relay:

$$LPpu = 3.25 \text{ cycles}$$

THERMAL PROTECTION OF CLOSE AND TRIP RESISTORS

Application Description

If the protected breaker is equipped with trip and close resistors, and three-phase potentials are available on both sides of the breaker, you can use the relay thermal protective elements to protect breaker resistors. Occasionally, a trip or close resistor can be left in service following a breaker operation. The relay model calculates the energy accumulated in the resistor and trips the protected breaker or 86 lockout relay when resistor energy reaches a preset level. See Figure 3.19 for a logic diagram of the thermal logic.

The output of the thermal protection is the assertion of the TTF (trip thermal failure) or CTF (close thermal failure) Relay Word bit. These bits must be used in control logic for energizing an external alarm retripping the breaker or asserting a lockout relay. Refer to ***Lockout Relay Control*** in ***Section 4: Close Logic***. Other useful Relay Word bits are 26TFA, 26TPA, 26CFA, and 26CPA, which are the energy accumulation comparisons to the trip and close failure and pending failure settings.

Operating Characteristic

The logic shown in Figure 3.19 is designed to protect the trip and close resistors in A-phase of the circuit breaker. Logic for B-phase and C-phase is similar. The relay uses independent thermal models to calculate the energy dissipated in each of the six sets of resistors.

Use the **HEAT** command to track or reset thermal model resistor energy.

The logic uses one input, ΔVA, calculated from other relay logic. The input ΔVA is the voltage difference across the breaker after steady-state voltage differences have been removed. See Figure 3.20 for the voltage nulling logic diagram.

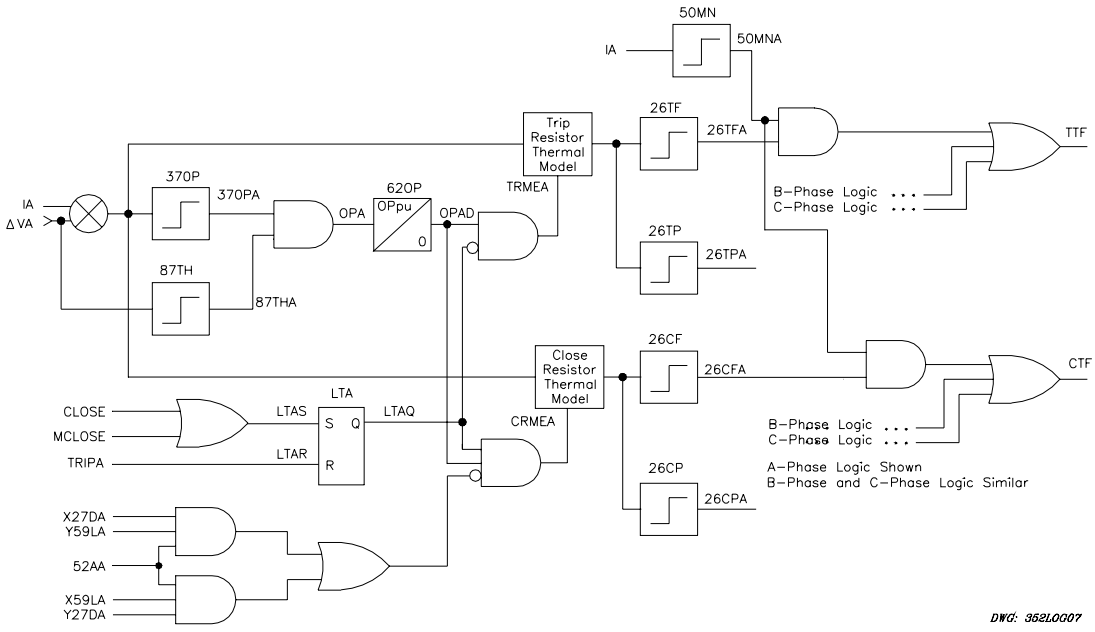

Figure 3.19: Trip and Close Resistor Thermal Protection Logic

Voltage Nulling

Figure 3.20 shows the voltage nulling circuit used by the SEL-352 Relay. This circuit removes steady-state voltage differences across the circuit breaker. The maximum nulling is based on the Kmag and Kang settings. This logic is fixed and cannot be customized.

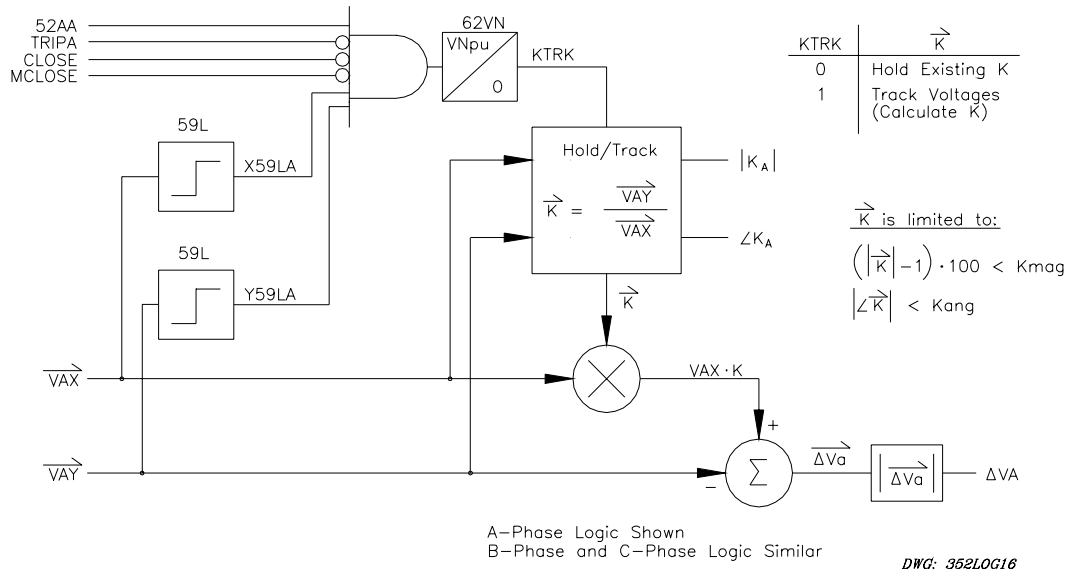

Figure 3.20: A-Phase Voltage Nulling Logic

Setting Description

Trip Inputs (TRIPA, TRIPB, TRIPC)

Use **SET G <ENTER>** to associate the breaker failure initiate logic inputs (TRIPA, TRIPB, TRIPC) with physical inputs.

Close Signals (CLOSE, MCLOSE)

Use the **SET G <ENTER>** command to select either an automatic close (CLOSE) or manual close (MCLOSE).

Any optoisolated input can be used to control these Relay Word bits. For example, if IN101 is to be used to indicate an A-phase trip initiate from another relay, set TRIPA = IN101. If IN105 is used to indicate an automatic close from another device, set CLOSE = IN105. Repeat this for each programmable input. The same input may be used for all three trip conditions if single-pole tripping is not used. The programmable input settings are actually SELOGIC control equations. Use any combination of Relay Word bits according to the SELOGIC control equation criteria in ***Section 5: Control Logic***.

Breaker Status (52AA, 52AB, 52AC)

Access the three programmable breaker status inputs (52AA, 52AB, 52AC) with **SET G <ENTER>**.

Phase Overpower (37OP)

Range: 0.10–3400.00 W in 0.01-W steps (5 A)
0.02–680.00 W in 0.01-W steps (1 A)

Use **SET <ENTER>** to access the 37OP element setting. This setting establishes the power level above which the model is heating and below which the model is cooling.

Negative-Sequence Overvoltage (47Q)

Range: 2.0–140.0 V in 0.1-V steps

The negative-sequence overvoltage element (47Q) is not used in the predefined thermal logic. When the negative-sequence voltage (V_2) for the X- or Y-side voltages exceeds the 47Q setting, Relay Word bits X47Q or Y47Q assert, respectively. These two bits are inputs to a logical OR gate whose output is Relay Word bit 47Q. Note that the 47Q voltage setting is in terms of V_2, not $3V_2$.

Thermal Model Voltage Threshold (87TH)

Range: 1.0–150.0 V in 0.1-V steps

Use **SET <ENTER>** to access the 87TH setting. SEL-352 Relay calculates a per-phase difference voltage and compares this to the 87TH setting. The calculation includes error nulling, discussed later in this section.

The value compared to the 87TH setting is the transient voltage difference across the breaker prior to voltage nulling. When trip or close resistors are stuck in service, a difference voltage is measured across the breaker pole. Set the 87TH so it will pick up for stuck resistors.

Voltage Nulling Delay (VNpu)

Range: 0.00–240.00 minutes in 0.01-minute steps

Use **SET <ENTER>** to access the VNpu setting. This setting defines the delay before the system returns to a steady-state condition after switching operations.

The thermal logic, flashover logic (Scheme 1), and the potential transformer disagreement alarm logic all consider calculations of the voltage nulling logic. Potential transformers on either side of a breaker typically will not have identical measurements due to potential transformer physical differences. The differences between the potential transformers can appear as difference voltage across the breaker. The voltage nulling logic eliminates the difference between the two measurements for steady-state conditions. Refer to Figure 3.20 for a logic diagram of the logic.

The voltage difference is nulled when all of the following conditions have been true for a settable time:

- Breaker is closed for the particular phase
- No trip input is received for the particular phase
- No close input is received
- Both X- and Y-side voltages are live for the particular phase

The output of the logic includes the adjusted difference voltage, a magnitude of the amount of error that is nulled, and an angle of the amount of error that was nulled.

A recommended voltage nulling delay setting is VNpu = 10 minutes.

Maximum Magnitude Nulling (Kmag)

Range: 0.0–30.0% in 0.1% steps

Use **SET <ENTER>** to access the Kmag setting and establish a limit to the amount of acceptable voltage nulling. Kmag is set in percent and is compared to the absolute value of 1–(VAY/VAX). When this limit is reached, the voltage nulling remains at that threshold, and the potential transformer disagreement (PTD) alarm asserts. Tracking continues when the nulling drops below Kmag again.

Select the Kmag setting based on the accuracy of your potential measurement device and actual field measurements during steady-state conditions. A recommended setting is Kmag = 5%.

Maximum Phase Error to Null (Kang)

Range: 0.0–15.0° in 0.1° steps

Use **SET <ENTER>** to access the Kang setting and establish a limit to the acceptable angle of voltage nulling. Kang is set in degrees and is compared to the absolute value of the angle difference between VAX and VAY. When this limit is reached, the voltage nulling remains at that threshold and the potential transformer disagreement (PTD) alarm asserts. Tracking continues when the nulling drops below Kang again.

Select the Kang setting based on the accuracy of your potential measurement device and actual field measurements during steady-state conditions. A recommended setting is Kang = 10°.

Thermal Logic Enable (THLOG)

Range: OFF, ON, CUSTOM

Use **SET <ENTER>** to access the THLOG setting. Enable, modify, or disable the thermal logic for protecting the breaker trip and close resistors.

Set THLOG = ON to enable the thermal logic for protecting the breaker trip and close resistors. Refer to Figure 3.19 for a logic diagram of the scheme.

If the breaker does not have trip and close resistors, or if you do not want thermal protection, set THLOG = OFF. If you need logic for your application different from that available with either of the two schemes, set THLOG = CUSTOM. When CUSTOM is selected, all thermal settings are shown including the SELOGIC control equations. Modify these settings to meet your specific application needs.

Some examples of custom applications include using current and voltage separately to supervise the thermal elements for the trip and close resistors, respectively. Another application entirely different from the thermal logic is use of the settings to develop a synchronism checking element that is based on a difference voltage and a timer. Refer to ***Section 4: Close Logic*** for a description of this application.

Overpower Pickup (OPpu)

Range: 0–16383 cycles in 1/4-cycle steps

Use **SET <ENTER>** to access the OPpu time delay pickup timer setting. This setting delays heating of the resistor thermal models for a settable time following 37OP and 87TH assertions. This time delay allows thermal elements to ride through switching transients produced by capacitively coupled voltage transformers (CCVT).

Close Pending Failure (26CP)

Range: 0.001–1000.000 J in 0.001-J steps (5 A)
0.002–200.000 J in 0.001-J steps (1 A)

Use **SET <ENTER>** to access the 26CP setting and establish the threshold at which the relay asserts an alarm for pending close resistor failure.

Close Failure (26CF)

Range: 0.010–1000.000 J in 0.001-J steps (5 A)
0.002–200.000 J in 0.001-J steps (1 A)

Use **SET <ENTER>** to access the 26CF setting and establish the threshold at which the relay asserts an alarm for close resistor thermal failure.

Trip Pending Failure (26TP)

Range: 0.010–1000.000 J in 0.001-J steps (5 A)
0.002–200.000 J in 0.001-J steps (1 A)

Use **SET <ENTER>** to access the 26TP setting and establish the threshold at which the relay asserts an alarm for pending trip resistor failure.

Trip Failure (26TF)

Range: 0.010–1000.000 J in 0.001-J steps (5 A)
0.002–200.000 J in 0.001-J steps (1 A)

Use **SET <ENTER>** to access the 26TF setting and establish the threshold at which the relay asserts an alarm for trip resistor thermal failure.

Cooling Time Constants (CRTC, TRTC)

Range: 1–1140 minutes in 1-minute steps

As soon as the difference voltage across the breaker drops below the 87TH setting, or the power across the breaker drops below the 37OP setting, the relay models breaker resistor cooling. Use **SET <ENTER>** to access the CRTC and TRTC settings and use these to define the close and trip resistor cooling time constants, respectively.

Blown Potential Supervision (59L, 27D)

Range: 10.0–120.0 V in 0.1-V steps (59L)
1.0–120.0 V in 0.1-V steps (27D)

The 59L and 27D elements supervise the thermal logic. If one side of the closed breaker (on a per-phase basis) is energized (59L) and the other side is dead (27D), the thermal logic is disabled because a blown potential fuse condition exists. Without the voltage supervision, the thermal logic may misoperate.

Refer to the Controlled Closing logic in ***Section 4: Close Logic*** for 59L and 27D setting recommendations.

Setting Calculations

Thermal Model of Trip and Close Resistors

The output of the thermal models is a number in Joules calculated from either the heating or the cooling equation. When power is applied greater than the 37OP setting from the OPpu pickup time, the model is heating. Before the OPpu time expires, or if the power applied is less than the 37OP setting, the model is cooling.

When the model is heating, calculate the energy by integrating the power with respect to time. If a constant power is applied, the energy is simply the power multiplied by the time.

$$\text{Energy}(t) = \int (\Delta VA \cdot IA) \cdot dt$$

When the model is cooling, the energy is decaying exponentially based on the following equation:

$$\text{Energy}(t) = \text{Energy}(t_0) \cdot e^{\frac{-t}{RTC}}$$

where:

Energy(t_0) is the initial energy

t = Seconds

RTC= Resistor time constant setting (CRTC, TRTC)

Phase Overpower (37OP)

Select a 37OP element setting so the element asserts when the minimum line current is flowing through the minimum breaker resistance possible while resistors are in circuit. The 37OP element setting is based on single-phase power dissipated in any breaker pole.

Calculate the minimum breaker resistance with resistors in circuit when the trip and close resistors are inserted in parallel.

For the example breaker:

$$R_{TRIP} = 2 \cdot 110\ \Omega = 220\ \Omega$$

$$R_{CLOSE} = 2 \cdot 35\ \Omega = 70\ \Omega$$

$$R_{MIN} = \frac{220 \cdot 70}{220 + 70}\ \Omega \text{ primary}$$

$$= 53\ \Omega \text{ primary}$$

Line-charging current is 350 A primary, so the minimum resistor in circuit voltage is:

$$V_{MIN} = \frac{350\ A \cdot 53\ \Omega}{4300} = 4.3\ V \text{ secondary}$$

Line-charging current times minimum resistor in circuit voltage across the breaker yields the minimum power for which 37OP should be required to assert.

$$P_{MIN} = \frac{350\ A}{600} \cdot 4.3\ V = 2.5\ W \text{ secondary}$$

Consider 37OP element accuracy when selecting a setting. Element accuracy is specified: 37OP ±2.25 mW ±10.25% of measured power ±2.63% of measured voltage ±9.45% of measured current. At 37OP pickup, the maximum error is calculated:

$$\Delta P_{MIN} = 2.25\ mW + 10.25\% \cdot (P_{MIN}) + [2.63\% \cdot V_{MIN} + 9.45\% \cdot I_c]\ W$$

$$\Delta P_{MIN} = 2.25\ mW + 10.25\% \cdot (2.5\ W) + [2.63\% \cdot 4.3 + 9.45\% \cdot 0.58]\ W$$

$$\Delta P_{MIN} = 2.25\ mW + 256\ mW + 113\ mW + 54.8\ mW$$

$$\Delta P_{MIN} = 426\ mW$$

To ensure that the 37OP element asserts under minimum resistor in circuit power and maximum error conditions, we select a 37OP element setting:

$$37OP = 2.5\ W - 0.426\ W = 2.07\ W \text{ secondary.}$$

Thermal Model Voltage Threshold (87TH)

Initially, set 87TH so the element asserts when the minimum line current is flowing through the minimum breaker resistance possible while resistors are in circuit.

The minimum breaker resistance as calculated for 37OP with resistors in circuit is found when the trip and close resistors are inserted in parallel.

For the example breaker:

$$R_{TRIP} = 2 \cdot 110\ \Omega = 220\ \Omega$$

$$R_{CLOSE} = 2 \cdot 35\ \Omega = 70\ \Omega$$

$$R_{MIN} = \frac{220 \cdot 70}{220 + 70}\ \Omega \text{ primary}$$

$$= 53\ \Omega \text{ primary}$$

Line-charging current is 350 A primary; thus the minimum resistor in circuit difference voltage across the breaker is:

$$V_{MIN} = \frac{350\ \text{A} \cdot 53\ \Omega}{4300} = 4.3\ \text{V secondary}$$

To make sure the 87TH picks up for this minimum difference voltage condition, set 87TH = 4.3 or less. If differential measurements immediately after a successful close operation pick up the 87TH element longer than the OPpu time, the SEL-352 Relay will incorrectly indicate heating of the resistors. The 87TH setting should be raised if this condition exists.

Overpower Pickup (OPpu)

For the example protected breaker, we select an OPpu setting as follows:

$$62OP = 3 \text{ cycles}$$

If you are unsure of the amount of time necessary to ride through the transients, use the SEL-352 Relay event report to see how long the 87TH and 37OP bits are asserted after a switching operation. Refer to ***Section 10: Event Reports and SER*** for a description of the event reports.

Close Resistor Energy

Next, calculate the energy capacity of the close resistors. In the example breaker, the close resistors consist of 28 ceramic disks that have a volume per disk of 225 cm^3 and a maximum thermal capacity of 700 J/cm^3. Maximum thermal stress per head is calculated as follows:

$$TS_{MAX} = 28 \text{ disks} \cdot 225\ cm^3 \cdot 700\ J/cm^3$$

$$TS_{MAX} = 4.41 \text{ MJ primary per breaker pole}$$

$$TS_{SEC} = \frac{4.41\ \text{MJ primary}}{CTR \cdot PTR} = 1.71\ \text{J secondary}$$

Thermal failure settings should prevent a normal close operation from adding enough energy to damage resistors after thermal failure elements assert.

Close Pending Failure (26CP)

Setting the relay conservatively, we select the close resistor pending failure element 26CP to assert when the thermal model reaches 65 percent of the maximum thermal stress calculated above:

$$26CP = 65\% \cdot TS_{SEC} = 1.11 \text{ J secondary}$$

Close Failure (26CF)

We select the close resistor thermal failure element 26CF to assert when the thermal model reaches 85 percent of the maximum thermal stress calculated above:

$$26CF = 85\% \cdot TS_{SEC} = 1.45 \text{ J secondary}$$

Trip Resistor Energy

Next, calculate the energy capacity of the trip resistors. In the example breaker, the trip resistors consist of 88 ceramic disks that have a volume per disk of 225 cm^3 and a maximum thermal capacity of 700 J/cm^3. The maximum thermal stress per head is calculated as follows:

$$TS_{MAX} = 88 \text{ disks} \cdot 225 \text{ cm}^3 \cdot 700 \text{ J/cm}^3$$

$$TS_{MAX} = 13.86 \text{ MJ primary per breaker pole}$$

$$TS_{SEC} = \frac{13.86 \text{ MJ primary}}{CTR \cdot PTR} = 5.37 \text{ J secondary}$$

Thermal failure settings should prevent a normal trip operation from adding enough energy to damage resistors after thermal failure elements assert.

Trip Pending Failure (26TP)

Setting the relay conservatively, we select the trip resistor pending failure element 26TP to assert when the thermal model reaches 65 percent of the maximum thermal stress calculated above:

$$26TP = 65\% \bullet TS_{SEC} = 3.49 \text{ J secondary}$$

Trip Failure (26TF)

We select the trip resistor thermal failure element 26TF to assert when the thermal model reaches 85 percent of the maximum thermal stress calculated above:

$$26TF = 85\% \bullet TS_{SEC} = 4.56 \text{ J secondary}$$

Cooling Time Constants (CRTC, TRTC)

The circuit breaker manufacturer should be able to provide data regarding resistor cooling time constants. If not, you can calculate the constants as follows. Assume that cooling from 200°C to near ambient temperature takes four hours, or three time constants (95 percent cooled). This implies a cooling time constant equal to the value determined by the following equation:

$$CRTC = \frac{240 \text{ minutes}}{3} = 80 \text{ minutes}$$

For the example, 80-minute cooling time constants were selected for CRTC and TRTC.

If you select an inaccurate cooling time constant, the resistor energy models may not be realistic for some time after breaker operations. For instance, if the cooling time constant is too short, a breaker resistor may actually contain more energy than is modeled and cause pending failure and failure energy levels to be less conservative than intended.

FLASHOVER CONDITIONS

Application Description

Breaker failure protection during flashover conditions is completely independent from the other protection logic. Use this protection in addition to the other protection or by itself.

When an open breaker pole flashes over, the following conditions can be used to detect the failure:

- One per unit system voltage can be measured across the breaker pole before the flashover occurs.
- Once the flashover starts, voltage drops and current flows.

Because these two criteria may also describe breaker close operations, the flashover protection scheme should be disabled during breaker operations and for several cycles after.

The relay provides two schemes for detection of circuit breaker flashover. Scheme 1 uses potential measurements from both sides of the breaker to detect flashover. Scheme 2 uses a potential measurement on only one side of the breaker to detect flashover.

Operating Characteristic

Scheme 1 (Flashover, Six Potential Transformers)

Scheme 1 uses the voltage across the circuit breaker, derived from PTs on both sides of the breaker, and the current through the breaker to detect flashover. If PTs are only available on one side of the circuit breaker, the second scheme may be used to detect breaker flashover.

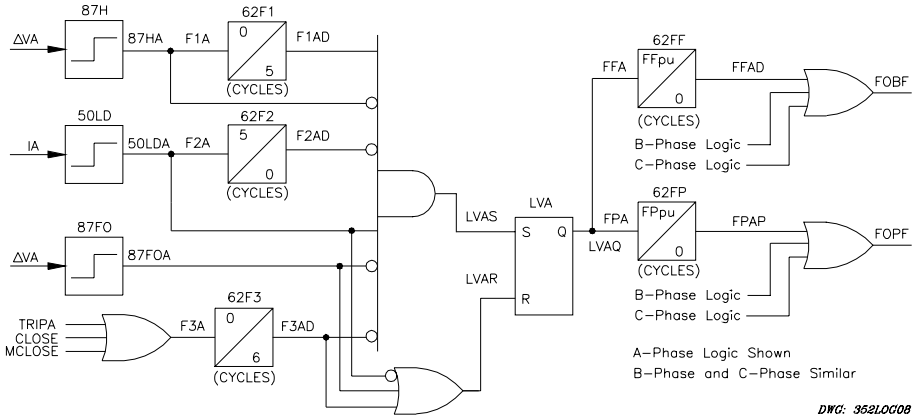

Figure 3.21: Flashover Condition Logic, Scheme 1–Six PTs

Scheme 2 (Flashover, Three Potential Transformers)

Scheme 2 uses the voltage on one side of the circuit breaker and the current through the breaker to detect flashover. This logic also needs the breaker monitor input.

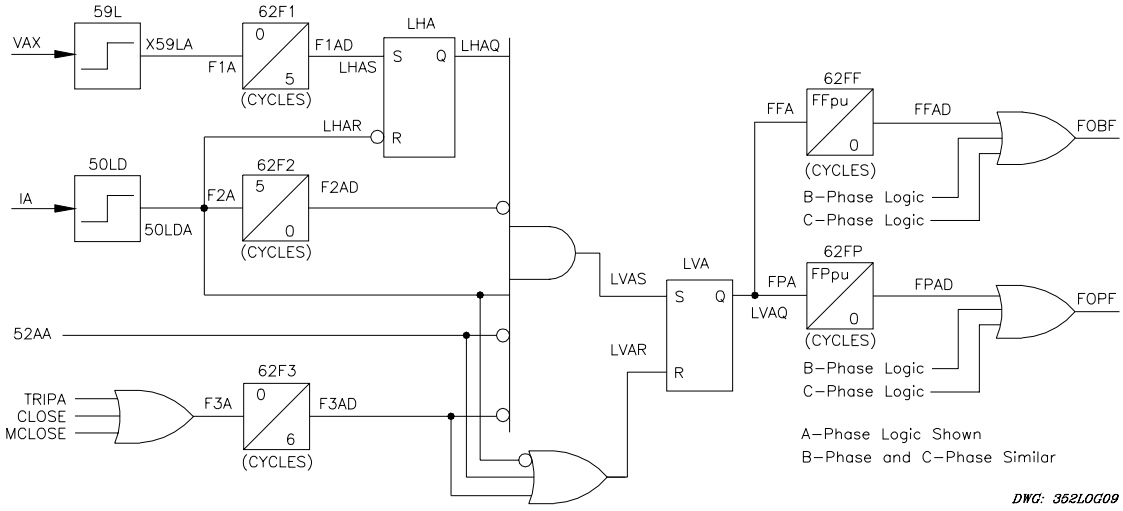

Figure 3.22: Flashover Condition Logic, Scheme 2–Three PTs

Setting Description

The 62FP and 62FF flashover timers start if the breaker is open and current exceeds the 50LD setting. The breaker is considered open based on a low set difference voltage setting 87FO (Scheme 1) or based on the 52AA, 52AB, and 52AC breaker status inputs (Scheme 2). The initial state of the voltages prior to the flashover also supervise the logic. Scheme 1 must have a difference voltage, 87TH, that exists and then suddenly (within 5 cycles) drops below the 87TH setting. For Scheme 2, the X-side voltage must be considered live (59L). The timers will continue to run and declare a pending failure or failure condition unless the current drops out, the breaker closes, a trip input occurs, or a close input occurs.

The output of the flashover protection is the assertion of the FOPF (pending failure) and/or FOBF (breaker failure) Relay Word bit(s). These bits must be used in control logic for asserting an external alarm, retripping the breaker, or energizing a lockout relay. Refer to ***Lockout Relay Control*** in ***Section 4: Close Logic***.

Trip Inputs (TRIPA, TRIPB, TRIPC)

Use **SET G <ENTER>** to associate the breaker failure initiate logic inputs (TRIPA, TRIPB, TRIPC) with physical inputs. Both flashover protection schemes use these three programmable inputs.

Any optoisolated input can be used to control these Relay Word bits. For example, if IN101 is used to indicate an A-phase trip condition from another relay, set TRIPA = IN101. If IN104 is used to indicate breaker status, set 52AA = IN104. Repeat this for each programmable input. The same input may be used for all three conditions if single-pole tripping is not used. The programmable input settings are actually SELOGIC control equations. Use any combination of Relay Word bits according to the SELOGIC control equation criteria in ***Section 5: Control Logic***.

Breaker Close Signal (CLOSE, MCLOSE)

Use **SET G <ENTER>** to determine whether the relay logic uses an automatic (CLOSE) or manual close (MCLOSE) signal. Both flashover protection schemes use these two programmable inputs.

Breaker Status (52AA, 52AB, 52AC)

Scheme 2 also uses the three programmable inputs: 52AA, 52AB, and 52AC, each of which you access with **SET G <ENTER>**.

High Set Differential Voltage (87H)

Range: 1.0–150.0 V in 0.1-V steps

Use **SET <ENTER>** to access the 87H setting. Use this setting, in Scheme 1 only, to indicate that a difference voltage exists across the breaker prior to current flowing in the breaker. In order for flashover to occur, a difference voltage must exist across the breaker.

A recommended setting is 87H = 57 V to pickup when one line side of the breaker is dead for a nominal 67V system.

If you use Scheme 2, accept the default 87H setting or use the 87H Relay Word bit in other custom logic for another application.

Flashover Differential (87FO)

Range: 1.0–150.0 V in 0.1-V steps

Use **SET <ENTER>** to access the 87H setting, which the relay uses in Scheme 1 only. Set 87FO to indicate that the difference voltage has collapsed to almost zero. When a flashover occurs, the voltage difference across the breaker drops to the amount of current times the arc resistance.

If the breaker uses trip and close resistors, set the 87FO element just less than the voltage measured across the breaker when resistors are left in service. This setting makes the flashover logic more secure during close operations.

For the example breaker, V_{MIN}, was calculated as:

$$V_{MIN} = 4.3 \text{ V secondary}$$

The accuracy specification of the 87FO element is ±0.09 V ±5% of settings, so:

87FO
maximum error $= 0.09 \text{ V} + (0.05) \bullet 4.3 \text{ V} = 0.3 \text{ V secondary}$

To ensure that 87FO asserts when a resistor is stuck in service

$$87FO = (4.3 - 0.3) = 4.0 \text{ V secondary}$$

A recommended setting is 87FO = 4 V.

If you use Scheme 2, accept the default 87FO setting or use the 87FO Relay Word bit in other custom logic for another application.

Overvoltage (59H/59L)

Range: 1.0–130.0 V in 0.1-V steps (59H)
10.0–120.0 V in 0.l-V steps (59L)

Use **SET <ENTER>** to access the overvoltage 59H and 59L settings, of which only the 59L setting finds use in the flashover logic. The 59H setting is not used for the flashover logic, but is a setting used as a security check in the controlled close logic for the synchronism supervision.

Scheme 1 does not use an overvoltage element. Scheme 2 of the flashover logic uses the 59L setting, but this setting is actually set in the controlled close logic to indicate a live bus or line.

Set 59H to indicate an overvoltage condition. A recommended setting is 59H = 100 V for a nominal 67V system.

The 59L Relay Word bit must be picked up prior to the flashover condition. Use the same criteria to set the 59L for the flashover logic as for the live bus or line conditions. A recommended setting is 59L = 57 V.

Flashover Scheme Selection (FOLOG)

Range: OFF, 1, 2, CUSTOM

Use **SET <ENTER>** to access the FOLOG setting. Select one of two predefined flashover schemes, select a custom scheme, or disable flashover protection.

The SEL-352 Relay provides two different protection schemes for breaker flashover conditions. Refer to Figure 3.21 and Figure 3.22 for logic diagrams of each scheme. Setting considerations for each scheme follow.

If you do not want flashover protection, set FOLOG = OFF. If your application requires different logic than that available from either of the two schemes, set FOLOG = CUSTOM. When CUSTOM is selected, all flashover settings are shown including the SELOGIC control equations. Modify these settings to meet your specific application needs.

Scheme 1 is designed for applications that have voltage measurements on both sides of the breaker. Scheme 2 is designed for applications where voltages are only available on one side of the breaker, but the breaker status input is also necessary.

Flashover Pending Failure (FPpu)

Range: 0–16383 cycles in 1/4-cycle steps

Use **SET <ENTER>** to access the FPpu setting and determine the delay before the 62FP timer expires and asserts the timer output FPAD. Assertion of this output results in assertion of the FOPF (pending failure) Relay Word bit.

Set flashover pending failure timer setting FPpu at some value shorter than the FFpu setting. The value for FPpu is based on the breaker operate time and the time calculated for FFpu. If you use the FPpu to energize a second trip coil, the FOPF bit should assert in enough time to let the breaker operate before tripping the lockout relay with the FOBF bit.

Flashover conditions require that the breaker is open as indicated by the 87FO element (Scheme 1) or the 52A status (Scheme 2). By tripping the breaker prior to energizing the lockout relay, you avoid clearing the bus for an incorrect indication of an open breaker. This FOPF trip output must not energize the TRIPA, TRIPB, or TRIPC inputs, or the flashover logic is defeated.

The recommended setting for FPpu is the FFpu time minus the nominal breaker operate time and some margin, FPpu = 25 cycles.

Flashover Failure (FFpu)

Range: 0–16383 cycles in 1/4-cycle steps

Use **SET <ENTER>** to access the FFpu setting and determine the delay before the 62FF timer expires and asserts the timer output FFAD. Assertion of this output results in assertion of the FOBF (breaker failure) Relay Word bit.

Set flashover failure timer setting FFpu based on the disruptive effects of breaker flashover on load and generation equipment and system stability. A recommended setting is FFpu = 30 cycles.

Load Detector (50LD)

Range: 0.01–45.00 A in 0.01-A steps (5 A)
0.02–9.00 A in 0.01-A steps (1 A)

The flashover logic uses the load current detector 50LD setting, but you set the value for this setting along with the load current protection logic. Use **SET <ENTER>** to access the 50LD setting and establish the level of current above which the 62FP and 62FF flashover timers will start if the breaker is open.

Set the 50LD (in settings for the load current protection logic) based on the same criteria as outlined for the load current protection logic earlier in this section.

CURRENT UNBALANCE PROTECTION

Application Description

The relay uses current unbalance logic to detect unbalance among the three-phase current magnitudes and to indicate failed closing of one or two breaker poles.

Operating Characteristic

Figure 3.23 shows the logic that detects unbalanced current conditions, which indicate that one or two breaker poles failed to close.

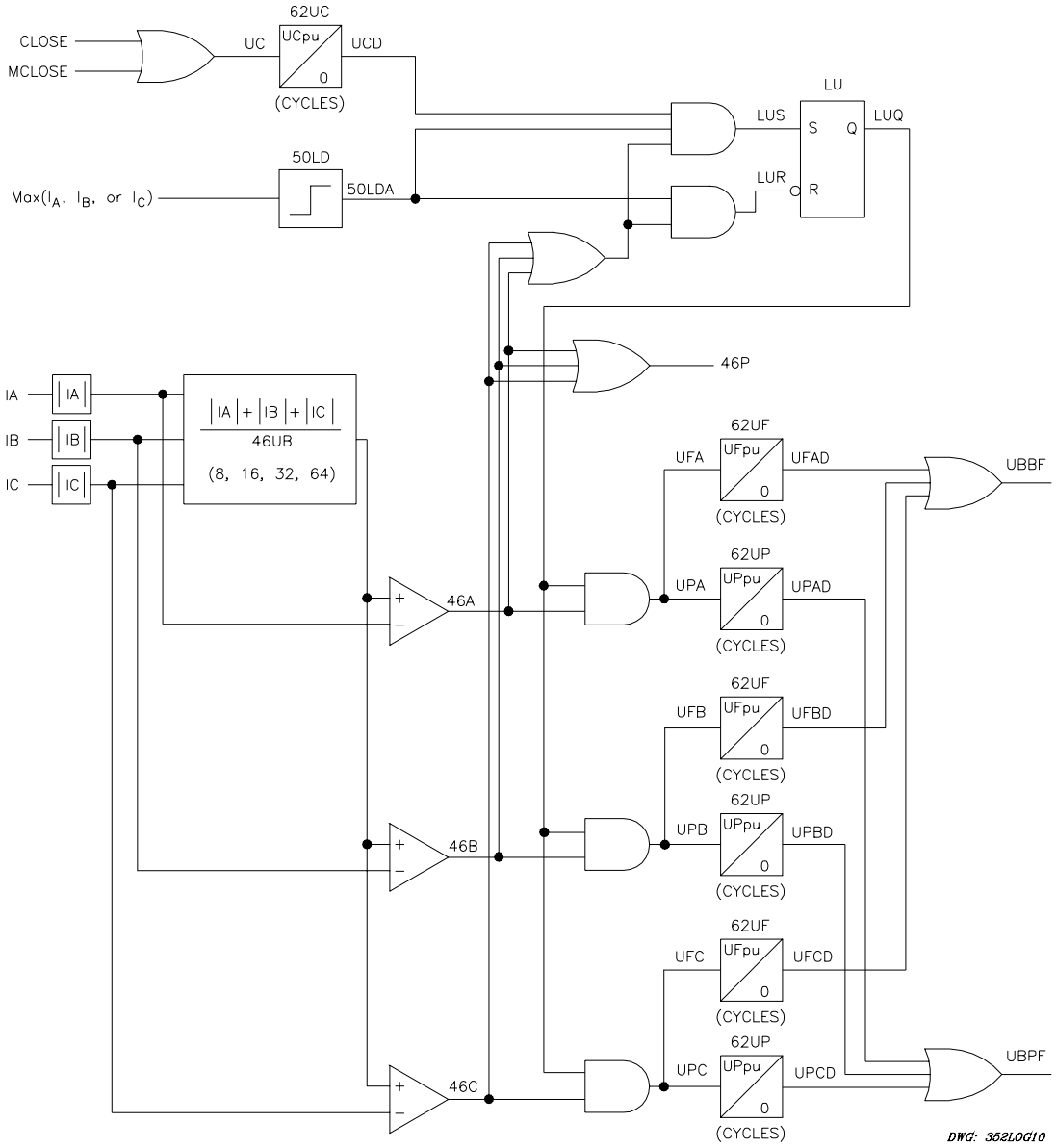

Figure 3.23: Current Unbalance, Failure to Close Logic

Setting Description

Breaker Close Signals (CLOSE, MCLOSE)

Use **SET G <ENTER>** to access the automatic and manual breaker close signals and determine which signal the relay will use in the current unbalance logic.

Any optoisolated input can be used to control these Relay Word bits. For example, if IN101 is used to indicate a close condition from another device or control switch, set CLOSE = IN101. The programmable input settings are actually SELOGIC control equations. Use any combination of Relay Word bits according to the SELOGIC control equation criteria in ***Section 5: Control Logic***.

Phase Current Unbalance Ratio (46UB)

Range: 8, 16, 32, 64

Use **SET <ENTER>** to access the 46UB setting. This setting defines the divisor the relay uses to determine whether an unbalance exists between the three-phase current magnitudes.

Phase Current Unbalance Enable (UBLOG)

Range: OFF, ON, CUSTOM

Use **SET <ENTER>** to access the UBLOG setting. Enable, modify, or disable the phase current unbalance logic to detect open conductors.

Set UBLOG = ON to enable the phase current unbalance logic. If you do not need phase current unbalance logic, set UBLOG = Off. If you need logic for your application different from that available with the default logic, set UBLOG=CUSTOM and modify logic settings to meet your specific application needs.

Close Input (UCpu)

Range: 0–16383 cycles in 1/4-cycle steps

Use **SET <ENTER>** to access the UCpu setting and define the close input timer pickup time.

Set the UCpu timer higher than the nominal closing time of the protected breaker. The timer may be set the same as the SlowCl setting. A recommended setting is 125 percent to 150 percent of timing tests. For the example breaker, assuming a closing time of four cycles, we select a setting:

UCpu = 6 cycles

The margin, in this case an additional two cycles, allows for possible pole scatter upon closure.

Unbalance Pending Failure (UPpu)

Range: 0–16383 cycles in 1/4-cycle steps

Use **SET <ENTER>** to access the UPpu setting and define the pending failure timer pickup time.

Set the current unbalance pending failure timer (UPpu) shorter than the UFpu setting. A recommended setting is UPpu = 50 cycles. The setting for UPpu is based on the breaker trip time and the time calculated for UFpu. If you use the UPpu to trip the breaker, the UBPF bit should assert in enough time to let the breaker trip before tripping the lockout relay with the UBBF bit. The recommended setting for UPpu is the UFpu time minus the nominal breaker trip time and some margin.

Unbalance Breaker Failure (UFpu)

Range: 0–16383 cycles in 1/4-cycle steps

Use **SET <ENTER>** to access the UFpu setting and define the breaker failure time delay.

When you set the failure time delay, consider the disruptive effects of current unbalance that may be caused by pole discordance (all three phases not closed simultaneously) on load or generation equipment and system stability. There may be a limit to the amount of time the system can withstand single phasing when the breaker carries maximum load. A recommended setting for the example breaker is UFpu = 60 cycles.

Setting Calculations

Phase Current Unbalance Ratio (46UB)

Increasing the 46UB setting decreases the ratio the relay uses to determine whether an unbalance exists between the three-phase current magnitudes. Lower unbalance ratio settings make the relay more sensitive to current unbalance. An example follows.

Assume 46UB = 8 and 1 per-unit current flows in each breaker pole upon closure. If A-phase and B-phase breaker poles close while the C-phase pole remains open, the relay makes the following comparisons:

$$\text{Ia} = 1 \text{ pu} > \frac{|\text{I}_a| + |\text{I}_b| + |\text{I}_c|}{8}$$

$$\text{Ia} = 1 \text{ pu} > \frac{1+1+0}{8}$$

$$\text{Ia} = 1 \text{ pu} > \frac{2 \text{ per–unit current}}{8}$$

$$\text{Ib} = 1 \text{ pu} > \frac{2 \text{ per–unit current}}{8}$$

$$\text{Ic} = 0 \text{ pu} < \frac{2 \text{ per–unit current}}{8}$$

The setting 46C asserts because C-phase current is less than the sum of phase current magnitudes divided by 46UB. C-phase current must rise above 0.25 per unit before 46C drops out. If 46UB equals 64, 46C drops out when C-phase current reaches 0.031 per unit. Thus, higher 46UB settings permit greater phase current unbalance.

For the example protected breaker, 46UB = 16.

Application Guideline

You can use the current unbalance logic to detect open conductors. The sensitivity of the detection depends on load conditions and the location of the open conductor.

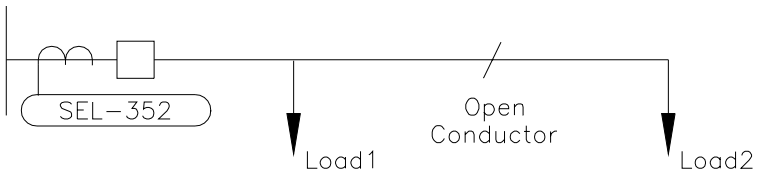

Figure 3.24: Single-Line Diagram for Open Conductor Condition

Individual breaker poles may not close because of mechanical problems (called pole discordance). The SEL-352 Relay current unbalance logic is designed to detect this condition. In addition to this detection, use the current unbalance logic to detect open conductor conditions. An open conductor is detected if a minimum amount of current flows through at least one phase with less than a certain percentage of the load between the relay and the open conductor. The current requirement is the minimum measurement and calculation capabilities of the relay for this logic. The limit to the percent of load between the open conductor and the relay depends on the 46UB setting.

For example, if there is no load between the relay and the open conductor, the loading on the open conductor phase will be zero. This is easy to detect. If there is load between the open conductor and the relay, the loading on the open conductor phase will be greater than zero at the relay. The relay can still detect the open conductor if this tapped load is less than the specified percent of the total load as seen by the relay.

The following settings represent the most sensitive pole-discordance and open conductor detection. The pole-discordance logic has a pending failure alarm condition and a breaker failure trip condition for all close operations. By setting the UBLOG setting to CUSTOM, the pending failure condition can be modified to monitor all unbalance conditions.

```
46UB = 8                              (most sensitive)
UBLOG = CUSTOM                        (changes to SELOGIC control equations are required)
UCpu = 6                              (same as current unbalance considerations)
UPpu = 1800                           (pickup time in cycles for open conductor detection)
UFpu = 60                             Default

UC = CLOSE + MCLOSE                   Default
LUS = UCD*50LD*(46A + 46B + 46C)      Default
LUR = !50LD + !(46A + 46B + 46C)      Default

UPA = 50LD*46A                        (A-phase open conductor detection)
UPB = 50LD*46B                        (B-phase open conductor detection)
UPC = 50LD*46C                        (C-phase open conductor detection)

UFA = LUQ*46A                         Default
UFB = LUQ*46B                         Default
UFC = LUQ*46C                         Default

UBPF = UPAD + UPBD + UPCD             Default
UBBF = UFAD + UFBD + UFCD             Default
```

Set the UBPF bit to assert an alarm or trip the breaker. Table 3.3 gives the amount of tapped load in percent of total load that may exist between the relay location and the open conductor for the relay to still detect the open conductor. The 50LD setting determines the amount of total load necessary for the logic to work. For a single open conductor condition, if 50LD is set to 0.1 A, phase current must be greater than the values in the secondary current column.

Table 3.3: Open Conductor Detection Specifications

46UB Setting	% Tapped Load	Secondary Current (Amps)*
8	25	0.13/phase
16	12	0.14/phase
32	5	0.18/phase
64	3	0.23/phase

*On a 5 A basis. Divide values by 5 for 1 A relay.

LOSS-OF-DIELECTRIC DETECTION

Application Description

Many breakers use pressurized air or gas as a dielectric and to help interrupt the electrical arc when tripping. If the amount of gas pressure is insufficient, the breaker may fail. Many breakers that rely on air or gas for such applications have pressure monitors, so the breaker will not attempt to operate under possible failure conditions. These pressure monitors can be connected to the SEL-352 Relay for sophisticated monitoring, reporting, and breaker failure tripping.

Operating Characteristic

The output of the loss-of-dielectric detection logic is a pending failure indication, LODPF, and a failure condition indication, LODBF. Use the pending failure output to trip the breaker before the gas pressure decreases to a level where the breaker could fail. Use the failure condition to trip the lockout relay and isolate the breaker. ***Section 4: Close Logic*** provides the logic diagram for this logic. Refer to Figure 3.25 for a timing diagram of the loss-of-dielectric detection logic.

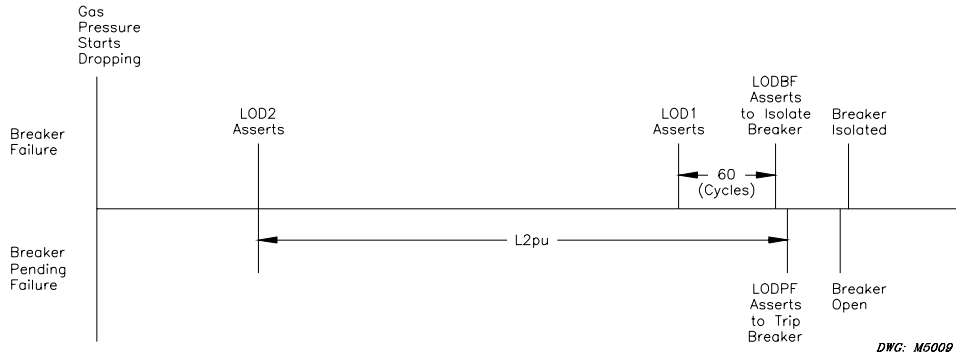

Figure 3.25: Loss-of-Dielectric Detection Timing

Figure 3.26 shows the default loss-of-dielectric logic used in the SEL-352 Relay. Assign LOD1 and LOD2 to inputs connected to pressure switches used to measure the dielectric gas pressure of the circuit breakers. Assign LODCT to inputs connected to a switch monitoring the dielectric pressure of the CTs.

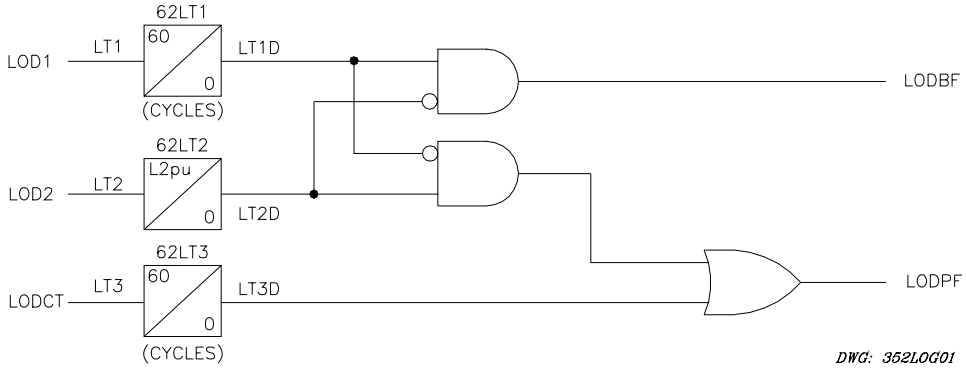

Figure 3.26: Loss-of-Dielectric Detection Logic

Setting Description

Dielectric Pressure Level Indicators (LOD1, LOD2, LODCT)

Use **SET G <ENTER>** to access and set the dielectric pressure level indicators. Use any optoisolated input to control these Relay Word bits. For example, if IN101 is used to indicate the first level of pressure, set LOD1 = IN101. Repeat this for each input. The input settings are actually SELOGIC control equations. Use any combination of Relay Word bits according to the SELOGIC control equation criteria in ***Section 4: Relay Logic***.

Two inputs are used to monitor two separate breaker gas pressure thresholds. A pressure device that monitors the breaker should apply control voltage to the SEL-352 Relay input when the pressure drops below the preset value. The high threshold asserts LOD2, and the low threshold asserts LOD1.

As pressure drops below the high threshold (LOD2), the L2pu timer starts timing. If the L2pu timer expires before the low threshold (LOD1) is reached, a pending failure is declared (LODPF). If the transition from the high to the low threshold is faster than the L2pu time (less 60 cycles), a breaker failure is declared (LODBF).

The LODCT input is used to monitor current transformer gas pressure. A pressure monitoring device should apply control voltage to the LODCT input when the pressure drops below the preset value. After 60 cycles of this low pressure condition, a pending failure is declared (LODPF).

Loss-of-Dielectric Logic Enable (DELOG)

Range: OFF, ON, CUSTOM

Use **SET <ENTER>** to access the DELOG setting. Enable, modify, or disable loss-of-dielectric logic.

Set DELOG to ON to enable the loss-of-dielectric detection logic. Modify the default logic by setting DELOG = CUSTOM. When set to CUSTOM, all settings are shown including the SELOGIC control equations. Use these settings for a modified loss-of-dielectric detection logic, or use it for an entirely different application. The default setting is DELOG = OFF.

One variation of the logic may be to only indicate a failure condition if the breaker is called upon to trip and the pressure is low. To do this set DELOG = CUSTOM, and LODBF = LT1D*!LT2D*TRIP3. This way, the lockout relay is tripped instantaneously if the pressure is low and a trip initiation is received. An output contact could also be used to assert an alarm by setting it as follows: OUT205 = LT1D*!LT2D.

Leak Timer (L2pu)

Range: 0–16383 cycles in 1/4-cycle steps

Use **SET <ENTER>** to access the L2pu setting and determine the delay between detection of a drop in pressure below the high threshold (LOD2) and declaration of a pending failure (LODPF).

Set L2pu based on the preset pressure threshold and the minimum amount of pressure necessary to trip the breaker. The pending failure bit LODPF should have enough time to trip the breaker before the pressure drops below the second threshold.

For example, a breaker that has a nominal pressure of 400 psi and pressure level thresholds at 80 percent and 50 percent, may be set to trip the breaker after 5 seconds of decreased pressure, but breaker isolation will occur if the pressure drops to the low threshold faster than 5 seconds.

LOD2 will assert and start the L2pu timer at 320 psi. With L2pu set at 300 cycles, the breaker is tripped after 5 seconds of decreased pressure. If the pressure gets to 200 psi, which asserts LOD1, the 60 delay timer starts. After 60 cycles, the breaker is isolated through the lockout relay if 5 seconds have not expired.

BREAKER ALARM LOGIC

Application Description

The BALRM bit indicates dangerous or abnormal conditions related to operation of the circuit breaker. The BALRM (Breaker Alarm) setting defines which breaker monitoring conditions assert the BALRM bit.

Operating Characteristic

When the BALRM bit asserts, the relay records the alarm in the breaker alarm report and the bit remains asserted for one second.

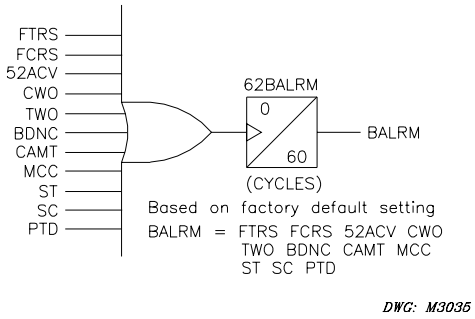

Figure 3.27: Breaker Alarm (BALRM) Logic

Remove any undesired breaker alarm condition from the BALRM setting to simplify the breaker alarm report. The breaker alarms cannot be modified individually. See ***Section 10: Event Reports and SER*** for information on the breaker alarm report using the **BRE** command.

FTRS:	Failed CB trip resistors put in service	CAMT:	Current after MOD Trip
FCRS:	Failed CB close resistors put in service	MCC:	MOD contradicts current
52ACV:	52A contradicts voltage	ST:	Slow trip
CWO:	Current while open	SC:	Slow close
TWO:	Trip while open	PTD:	Potential Transformers Disagree
BDNC:	Breaker did not close		

Set a programmable output contact to close for indication when the relay detects a breaker alarm condition. For example, set OUT101 = BALRM.

The following items explain conditions that cause BALRM assertion.

Failed CB Trip Resistors Put in Service

The FTRS bit asserts if any trip resistor thermal failure bit asserts and 86RS bit or close input assertion occurs.

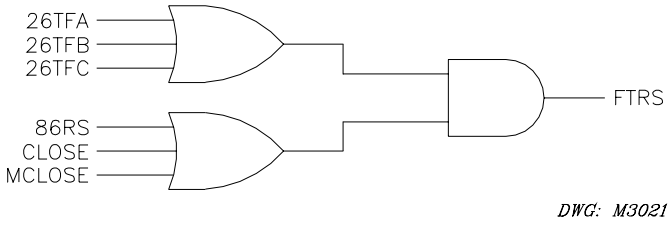

Figure 3.28: Failed CB Trip Resistors Put in Service

Failed CB Close Resistors Put in Service

The FCRS bit asserts if any close resistor thermal failure bit asserts and 86RS bit or close input assertion occurs.

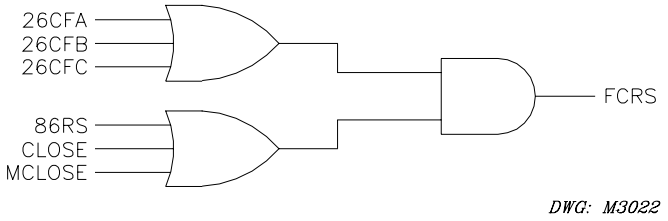

Figure 3.29: Failed CB Close Resistors Put in Service

52A Contradicts Voltage

The 52ACV bit asserts if the 87TH overvoltage bit picks up when a 52A bit asserts as long as a trip or close operation has not occurred for five cycles.

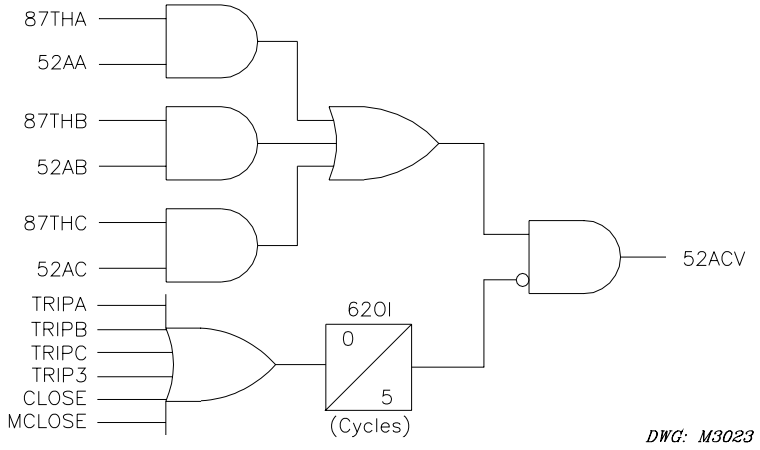

Figure 3.30: 52A Contradicts Voltage

Current While Open

CWO asserts if any 50LD element picks up when a 52A is not asserted, as long as a trip or close operation has not occurred for five cycles.

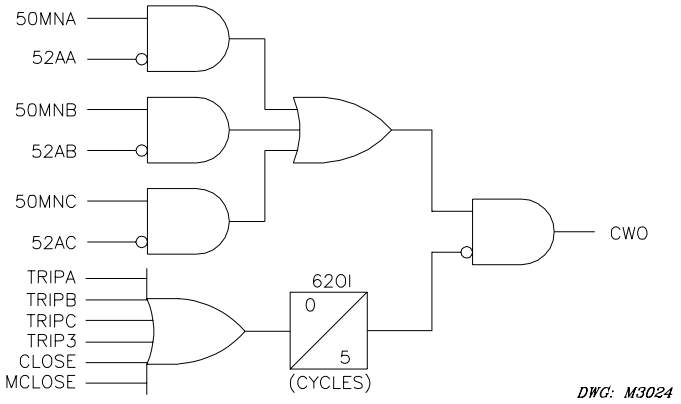

Figure 3.31: Current While Open

Trip While Open

TWO asserts if a trip input asserts while the 87FO element for that phase is picked up.

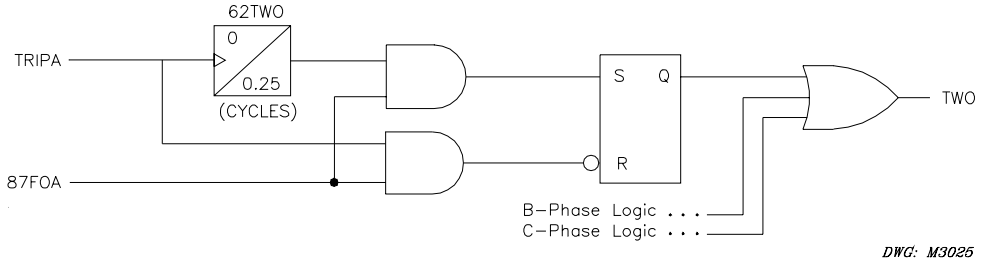

Figure 3.32: Trip While Open

Breaker Did Not Close

BDNC asserts if the 52A status still indicates an open breaker three seconds after the close output element (CCA) asserts. When the breaker status finally indicates a closed breaker, the three-second timer resets.

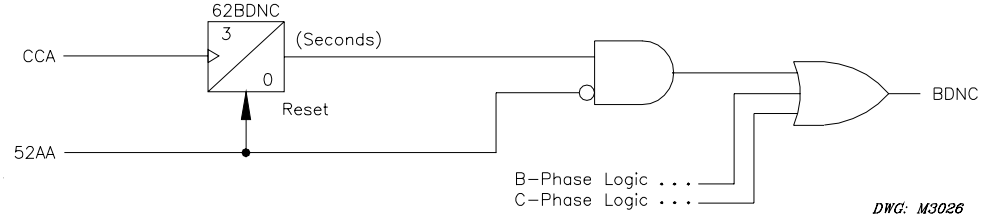

Figure 3.33: Breaker Did Not Close

Current After MOD Trip

CAMT asserts if any phase 50MN element is picked up or if the MOD status MODST input is asserted when the 62M3 timer of the lockout relay control logic expires.

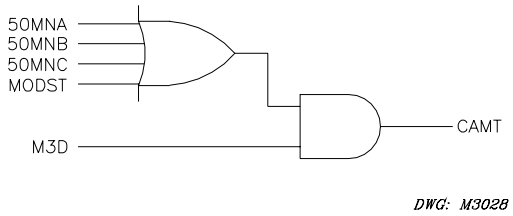

Figure 3.34: Current After MOD Trip

MOD Contradicts Current

MCC asserts if any phase 50MD element is picked up and the MOD Status (MODST) input does not assert, indicating that the MOD is open.

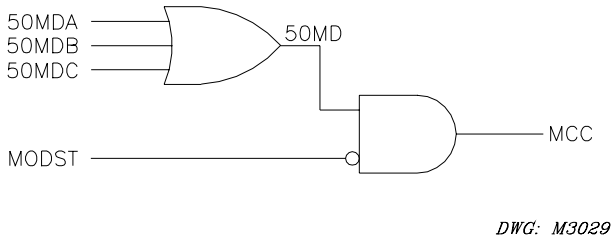

Figure 3.35: MOD Contradicts Current

Slow Trip

ST asserts if the A-, B-, or C-phase 50MN element is still picked up when SlowTr time expires following the A-, B-, or C-phase trip input assertion, respectively. The SlowTr timer resets when 50MNA drops out.

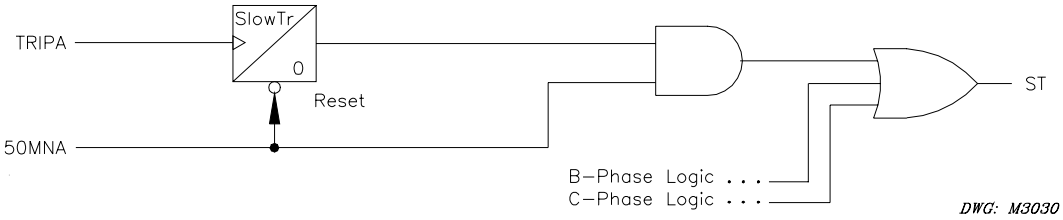

Figure 3.36: Slow Trip

Slow Close

SC asserts if the 52AA bit does not indicate a closed breaker Tclose time following the respective phase close input assertion. The SlowC1 timer resets when 52AA asserts.

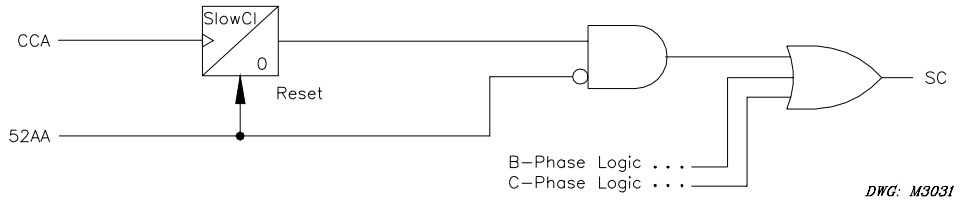

Figure 3.37: Slow Close

Potential Transformers Disagree

The PTD bit asserts if the voltage nulling constant K (see ***Voltage Nulling***) exceeds the Kmag or Kang setting.

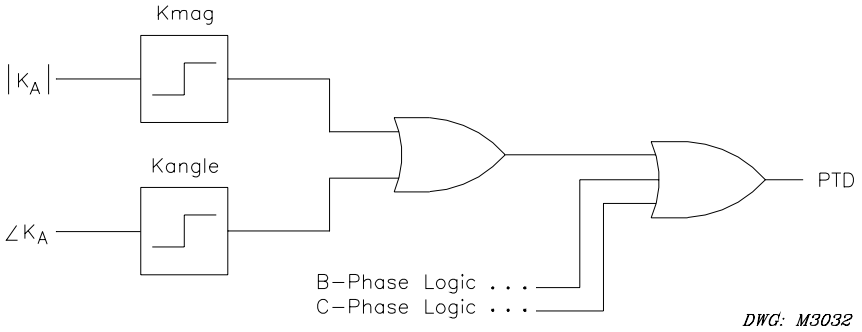

Figure 3.38: Potential Transformers Disagree

To disable any of the above breaker monitors, remove the element from the BALRM setting list.

TABLE OF CONTENTS

FIGURES

SECTION 4: CLOSE LOGIC

BREAKER CONTROL OVERVIEW

Manual and automated breaker control through the SEL-352 Relay has many advantages: consolidated wiring, sequential event records, no auxiliary relay required, and flexible logic, which all reduce total installation and operation costs.

All SEL-352 Relay output contacts and optoisolated inputs are programmable, except for the ALARM output contact. Set the SEL-352 Relay inputs and outputs to control the connected equipment appropriately.

CONTROLLED CLOSING

Application Description

Two controlled closing schemes are provided for reducing system transients. Each scheme supports automatic and manual closing.

Use Scheme 1 for staggered closing of independent breakers to reduce transients when you do not have PTs on both sides of your breaker or do not know your breaker operation time. Set the staggered close times to a time greater than the transient time but less than the time the system can tolerate a single-pole condition.

Use Scheme 2 for synchronized and point-on-wave closing when PTs are available on both sides of your breaker. Synchronized closing is used when both sides of a breaker are live. The logic determines when the two sides are in phase and closes the breaker at that time to minimize transients. Point-on-wave closing is used when one side of the breaker is live and the other is dead. The logic accommodates negative, zero, and positive trapped charge due to capacitor banks, etc., to minimize the voltage across the breaker at closing.

Operating Characteristic

Scheme 1 (Staggered Close)

Scheme 1 of the controlled closing logic is intended for breakers that have separate close coil circuits for each pole. When closing all breaker poles at the same time, differences in where poles close on the voltage waveform can cause transients that can cause system damage or degradation. This scheme can limit the amount and severity of transients by staggering the close operation of each individual pole.

Set the pickup time for each phase timer, selecting the delay for each individual phase. Figure 4.1 illustrates this logic for A-phase. B-phase logic and C-phase logic are similar.

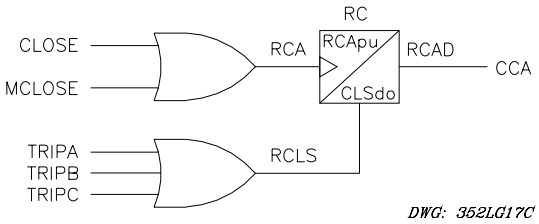

Figure 4.1: Staggered Close Logic, A-Phase

The left side of Figure 4.2 illustrates the latched timer symbol used in Figure 4.1 and other figures in this section. This symbol represents the logic on the right side of the figure.

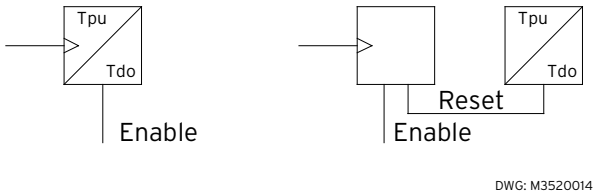

Figure 4.2: Latched Timer

Scheme 2 (Synchronism Checking, Point-On-Wave)

Scheme 2 of the controlled closing logic has two major parts: synchronized and point-on-wave closing. A block diagram of this logic is shown in Figure 4.3. Point-on-wave closing requires separate close coil circuits for each pole. When you close all breaker poles at the same time, differences in where poles close on the voltage waveform can cause transients that can cause system damage or degradation. This scheme detects various line conditions and voltage zero crossings to determine the optimum time to close each pole. Synchronized closing is a three-pole operation.

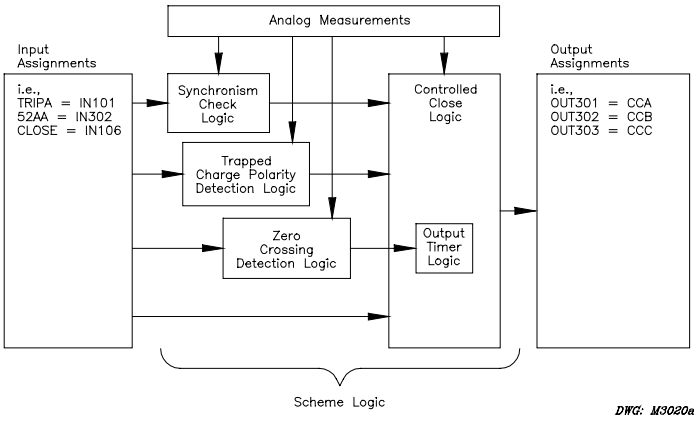

Figure 4.3: Controlled Close–Scheme 2 Block Diagram

An OR gate combines the synchronized and point-on-wave closing logic. Both sets of logic are necessary to fully address closing for all system conditions: live line and dead bus, dead line and live bus, live line and live bus, dead line and dead bus.

Synchronism Checking

Figure 4.4 shows the synchronism controlled close logic used in the SEL-352 Relay. Outputs 25C and 25M are used by the synchronism controlled close logic shown in Figure 4.5 and are available in the Relay Word. Note that the angle calculation is based on the slip frequency and the nominal closing time of the breaker, Tclose. The VnX and VnY voltages and X59Hn, X59Ln, and Y59Ln elements appear with the "n" in Figure 4.4. The SYNCP setting programs n as phase A, B, or C.

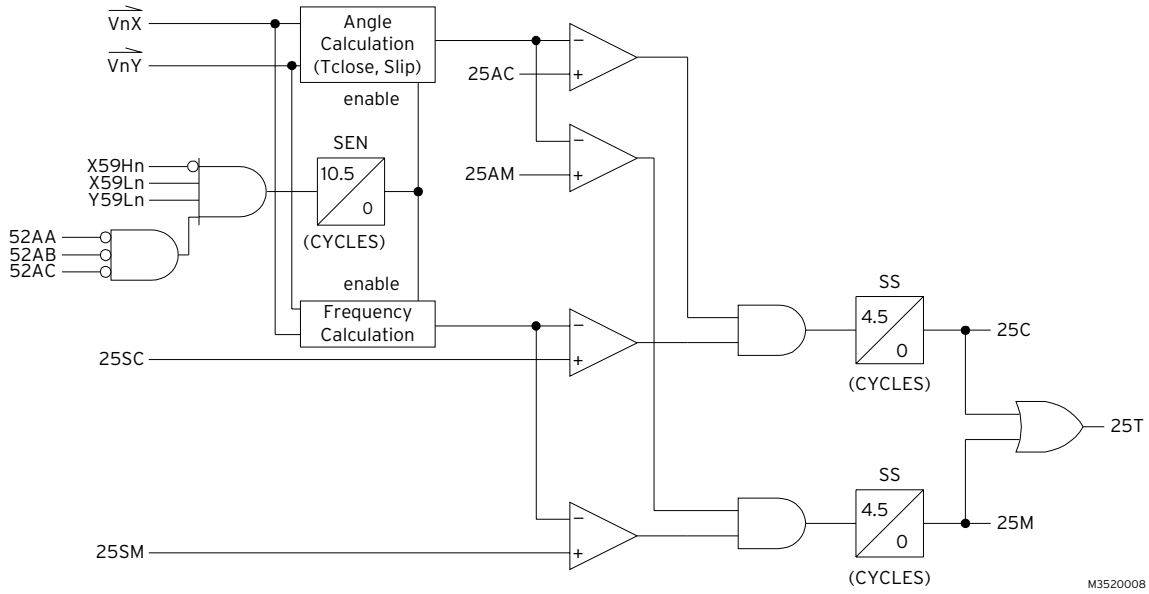

Figure 4.4: Synchronism Logic

Synchronism check output SCTD is combined with the point-on-wave outputs CTA, CTB, and CTC on a per-phase basis to form outputs CCA, CCB, and CCC, respectively. Figure 4.9 illustrates this combination for the A-phase logic. Note that RCLS (reset close) resets the close timers if any of the TRIPn inputs assert.

If you are trying to use the synchronism check logic for reclosing, there are at least two methods of using it without the point-on-wave logic. One method is to set CLSLOG=2, CLSA = CLSB = CLSC = any unused output, and PCApu = PCBpu = PCCpu = ZCApu = ZCBpu = ZCCpu = 0. Finally, set OUT301 = OUT302 = OUT303 = 0 and use SCTD in an output SELOGIC® control equation. A second method is to set CLSLOG=CUSTOM, ZCNA = ZCNB = ZCNC = ZCPA = ZCPB = ZCPC = PCNA = PCNB = PCNC = PCPA = PCPB = PCPC = 0, and only change the settings normally associated with Scheme 2.

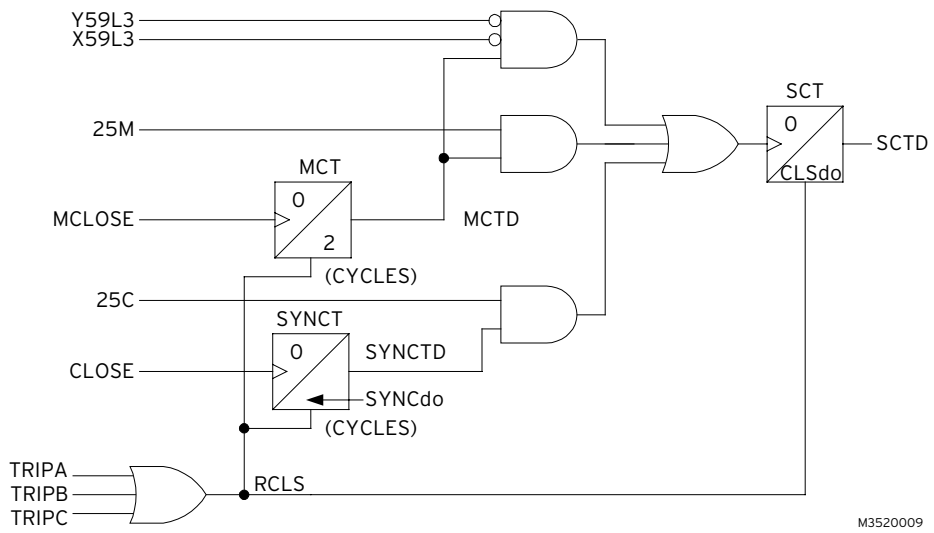

Figure 4.5: Synchronism Controlled Close Logic

Point-On-Wave

Point-on-wave closing reduces transients on the system during closing. Many factors cause transients. Closing a breaker at a certain point on the voltage waveform can reduce transients. Four conditions may exist when closing into de-energized equipment: the equipment has a standing positive voltage charge remaining (called trapped charge), the equipment has a standing negative voltage charge remaining, the equipment is completely de-energized (no trapped charge), or the equipment has a standing ac voltage on it from coupling or equipment resonance.

The accuracy of the point-on-wave closing depends greatly on breaker closing consistency. Breakers vary in tolerance depending on breaker type and manufacturer. Consult the breaker manufacturer for close time tolerances. Breaker closing times vary according to ambient temperature changes, control voltage level, age of the breaker, and time since last operation. The SEL-352 controls none of these factors, but calculates the instant to issue the close pulse to the breaker based on the above information. The location of this point can cause close time variation.

If a breaker closes into a dead line with the system voltage at a peak, the breaker will pre-strike (conduct before poles physically contact). If the voltage is at a zero crossing, the breaker will not conduct until the heads actually contact. This time difference between the pre-strike and the actual contact of the heads can account for breaker close time variation.

Trapped Charge Detection

The logic shown in Figure 4.6 monitors the voltage input channels for A-phase. B-phase logic and C-phase logic are similar.

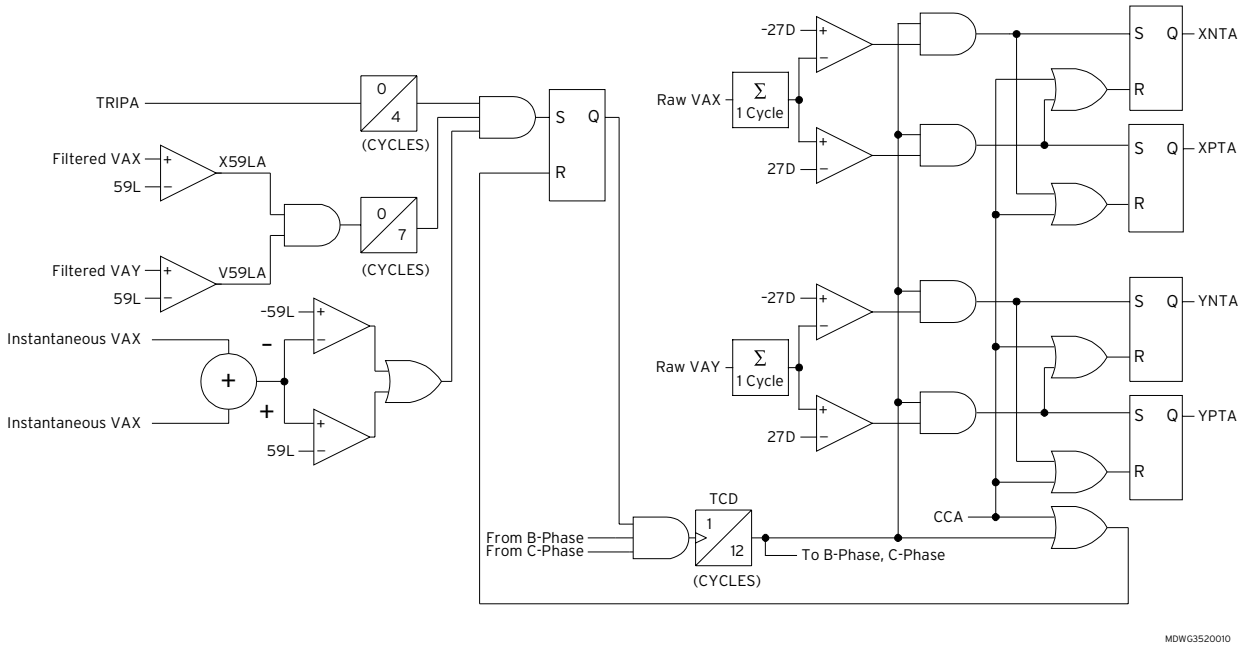

Figure 4.6: Trapped Charge Detection Logic, A-Phase

After a breaker opens, some voltage may still exist on the de-energized equipment. When the breaker closes again, the system voltage may be 180° out of phase from the trapped charge. If the trapped charge is a positive 1 pu and the breaker closes at a negative peak, there will be 2 pu across the breaker poles as the breaker closes. Closing at a positive peak minimizes the voltage across the breaker. The SEL-352 Relay detects the trapped charge polarity and closes the breaker accordingly.

Use the trapped charge detection for closing at voltage peaks for breakers with close time variations less than or equal to ±4 ms. If a breaker has an expected variation of ±4 ms and it operates at the edge of its error band, the breaker will close at a zero crossing instead of a peak. The voltage difference across the breaker will be equivalent to the amount of trapped charge. This closing scenario is still more desirable than random closing.

If the relay detects a positive trapped charge on one of the phases, it asserts the XPT (X-side, positive trapped charge) Relay Word bit for that phase for the X side and YPT bit for the Y side. If the relay detects a negative trapped charge, it asserts the XNT bit for that phase for the X side and YNT bit for the Y side. The point-on-wave controlled close logic shown in Figure 4.8 uses these Relay Word bits.

If the trapped charge detection logic detects no trapped charge, the SEL-352 Relay Default Scheme 2 controlled close logic will close the breaker at a negative going zero crossing. A closing at a zero crossing minimizes the likelihood of pre-strike, reducing breaker wear.

Zero Crossing Detection

Use the zero-crossing closing for breakers with close time variations less than or equal to ±2 ms. If a breaker has an expected variation of ±2 ms, and it operates at the edge of its error band, the breaker will close at 0.7 pu instead of at zero. The voltage difference across the breaker will

vary randomly between 0.7 pu and 0. This closing scenario is still more desirable than random closing, which could produce as much as 1-pu voltage difference.

Some applications have a higher 27D setting to indicate a dead line. Dead-line indication is desired even if the coupled or resonating voltage is high. The trapped charge detection logic will detect the voltage and recognize that it is ac and not trapped charge. Closing the breaker at a zero crossing is the most desirable for this case.

The logic determines the existence of trapped charge and the charge polarity by taking a one-cycle average of the measured voltages as the breaker poles open. If the measured values are sinusoidal, the average is zero. The measured average is compared to the 27D setting. A measured average larger than the 27D setting indicates positive trapped charge. An average less than the negative of the 27D setting indicates negative trapped charge.

Figure 4.7 shows the X-side voltage zero-crossing detector logic. The Y-side logic is similar. The logic determines whether there is a positive- or negative-going zero crossing. Outputs of this logic are used in the controlled closed output timer logic shown in Figure 4.9. These outputs trigger the ZCN, ZCP, PCN, and PCP timers, synchronizing them with the power system.

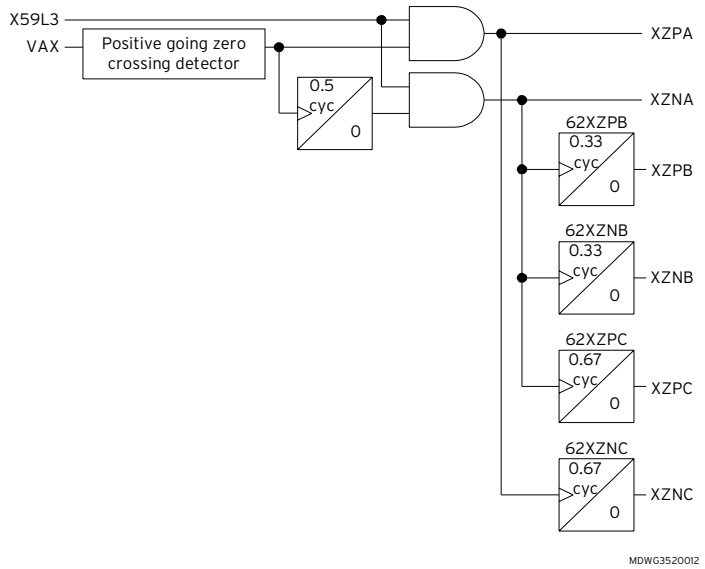

Figure 4.7: Voltage Zero-Crossing Detection Logic, X-Side

Controlled Close Logic

The outputs from this logic initiate the controlled closing timers. This logic combines the outputs of the X- and Y-side trapped charge logic with CLOSE and MCLOSE.

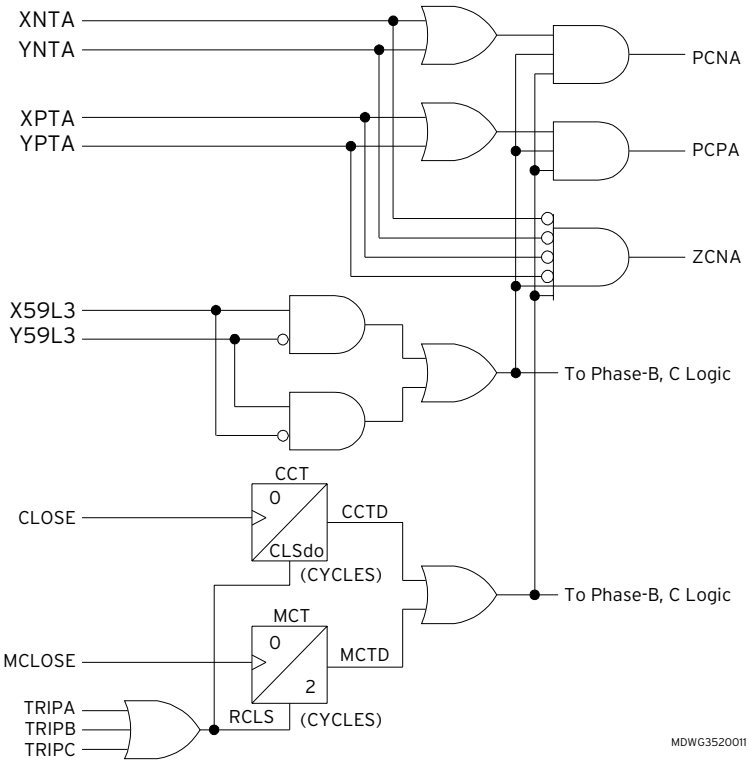

Figure 4.8: Point-On-Wave Controlled Close Logic, A-Phase

Controlled Close Output Timers

These timers are initiated by the zero-crossing and point-on-wave controlled close logic.

You cannot modify the output timer logic shown in Figure 4.9; however, you can turn the timers off. The CLSA, CLSB, and CLSC settings pick which outputs have timer logic associated with them, defaulting to OUT301, OUT302, and OUT303, respectively. The pickup times of timers in this figure are accurate to ±200 microseconds. Each phase has independent timer settings to enable the user to stagger the closing time of each phase.

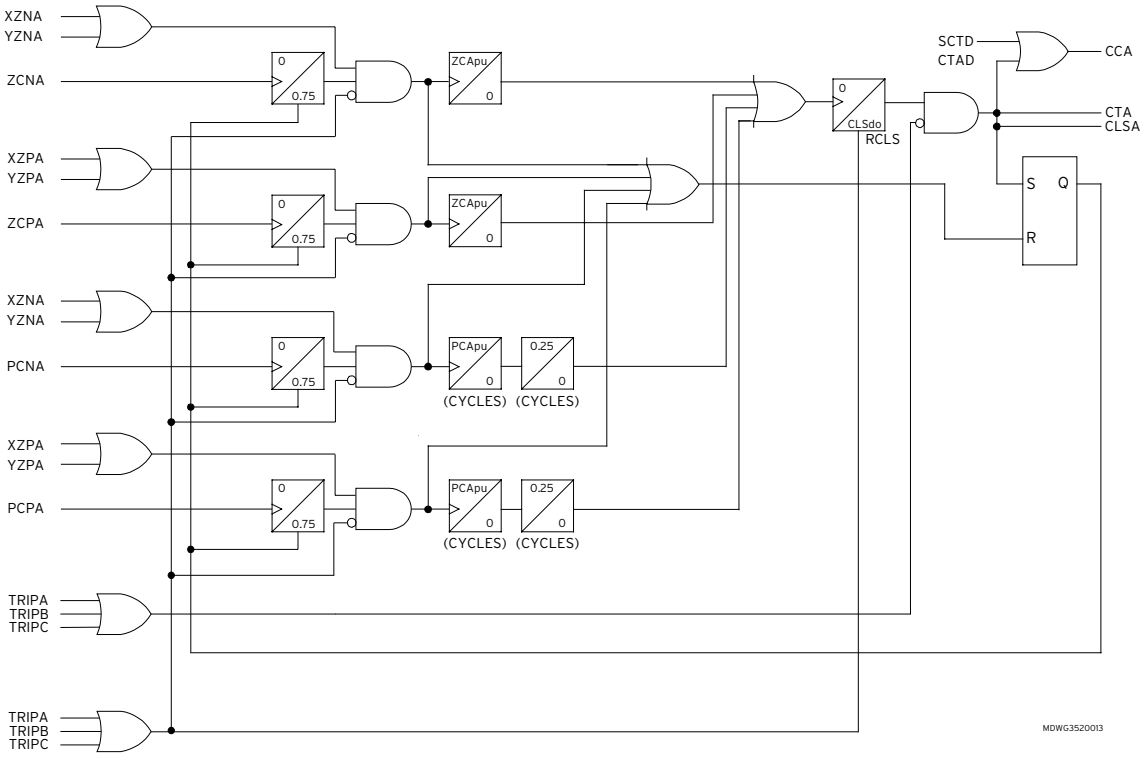

Figure 4.9: Controlled Close Output Timers, A-Phase

Setting Description

Trip Inputs (TRIPA, TRIPB, TRIPC)

Use the **SET G <ENTER>** command to associate the three programmable trip inputs (TRIPA, TRIPB, TRIPC) with physical inputs. These inputs block the controlled closing logic when asserted.

Breaker Close Signals (CLOSE, MCLOSE)

Use the **SET G <ENTER>** command to associate CLOSE or MCLOSE with a physical input, control bit, or remote bit. CLOSE and MCLOSE indicate a close initiation from another device or a manual close input condition. Use any optoisolated input to control these Relay Word bits. For example, if IN101 is to be used to indicate a close initiation, set CLOSE = IN101. The input settings are actually SELOGIC control equations. Use any combination of Relay Word bits according to the SELOGIC control equation criteria in ***Section 5: Control Logic***.

Live Line/Bus Voltage (59L)

Range: 10.0–120.0 V in 0.1-V steps

Use the **SET <ENTER>** command to program the 59L setting and the settings described below. Set 59L for the X- and Y-side voltage to indicate energized equipment. The recommended setting is 57 V for a nominal 67 V application.

Dead Line/Bus Under Voltage (27D)

Range: 1.0–120.0 V in 0.1-V steps

Set 27D for the X-and Y-side voltage to indicate dead (de-energized) equipment. The recommended setting is 10 V for a nominal 67 V application. Applications, where mutual coupling or capacitive coupling from parallel lines or other phases exists, will require a higher setting. In these cases, set the 27D setting to 120 percent of the voltage caused by coupling. Verify that a single contingency for the thermal logic does not drop the voltage below the 27D setting. When voltage drops below the 27D setting, the thermal logic is disabled. See ***Thermal Logic*** in ***Section 3: Breaker Logic.***

Controlled Closing Scheme Selection (CLSLOG)

Range: OFF, 1, 2, CUSTOM

Use either of two provided controlled closing schemes and modify either of these to meet your specific application. Enable a staggered close scheme for single-pole closing by setting CLSLOG = 1. Each pole is delayed by a timer so that transients may be reduced during the close operation. Enable a complete point-on-wave closing, synchronism checking, live-line dead-bus closing, and dead-line live bus closing by setting CLSLOG = 2.

Set CLSLOG = CUSTOM to modify the close logic. When set to CUSTOM, all settings are shown including the SELOGIC control equations. Use these settings for a modified close logic or for an entirely different application.

Close Dropout (CLSdo)

Range: 0–16383 cycles in 1/4-cycle steps

Set the close dropout time CLSdo to a value that makes certain the breaker close coil has been energized, and that the breaker has had time to close. When standard output contacts on the SEL-352 Relay energize the close coil, you must use an auxiliary breaker contact to interrupt the close coil current. The CLSdo timer holds the SEL-352 Relay output contact closed for the specified time. A recommended setting is the same as the SlowCl setting. Based on the default setting of SlowCl = 83, set CLSdo = 5 cycles.

If the high current interrupting contacts are used, the only concern for setting CLSdo is that the close coil must be energized long enough to close the breaker. The auxiliary contact may also be removed from the circuit if the close coil current is within the specified capabilities of the output contacts. Refer to ***Section 2: Installation***. When the high current interrupting contacts are not available, apply an SEL-9501 across a standard output contact to give the contact greater interrupt capability. Contact the factory for more information about the SEL-9501 Contact Arc Suppressor.

Staggered Close Timer Pickups (RCApu, RCBpu, RCCpu)–Scheme 1

Range: 0–16383 cycles in 1/4-cycle steps

Three timers provide staggered closing of the individual poles. You can set these timers independently. You must decide the following information about your system to determine appropriate timer settings:

- Which pole should close first?
- How long can the system accept a single-pole open/close condition?
- How long do the transient conditions persist?

Assuming that you selected A-phase as the first pole to close with a system that can accept a 3-cycle single-pole condition. In this case, voltage transients exist for less than 1 cycle, and the timer settings would be as follows:

Set RCApu = 0 to close A-phase instantaneously after the close input is received. Set RCBpu = 1.33 cycles to close one cycle later plus the 120° phase shift of B-phase. Set RCCpu = 2.67 cycles to close one more cycle later plus a second 120° phase shift. All timer settings are from the instant the close input is received. These settings would close all three phases at the same point on the corresponding voltage waveform. A single-pole condition would exist from the time A-phase physically closed to the time C-phase physically closes. This period is 2.67 cycles, assuming each pole takes the same amount of time to close after close coil energization. This 2.67 cycles is less than the 3-cycle requirement for the system and, in this case, the voltage transients decay in 1 cycle, which is less than the stagger times of 1.33 cycles between phases.

Maximum Slip Frequency for Control Close (25SC)–Scheme 2

Range: 0.005–0.500 Hz in 0.001-Hz steps

Two synchronizing elements provide separate automatic and manual close operation control. Set 25SC to the maximum allowable slip frequency for automatic close conditions (CLOSE input). The slip frequency is set in hertz (cycles/second). For timing considerations, a slip of 0.1 Hz is equivalent to 0.6° per power system cycle. An acceptable slip is dependent on the application. For synchronizing two parts of the same system, the slip will be very close to zero. Set 25SC in this case to 0.03 Hz.

The slip frequency setting determines the minimum angle setting allowed for 25AC, so do not set 25SC to its highest value just to desensitize the synchronism supervision. If 25SC equals 0.5, the minimum angle for 25AC is 16°.

Maximum Control Close Angle (25AC)–Scheme 2

Range: 32•25SC to 90° (min = 1) in 0.1° steps

Two synchronizing elements provide separate automatic and manual close operation control. Set 25AC to the maximum allowable angle difference for automatic close conditions (CLOSE input). The SEL-352 Relay will close an output contact based on the slip frequency and breaker close time so that the two systems are somewhere within the window. If the two systems are slipping by at a consistent rate, the SEL-352 Relay will initiate the close so that the breaker

closes on the leading edge of the window. For synchronizing two parts of the same system, the angle difference will be very close to zero. Set 25AC in this case to 10° or less.

The minimum 25AC setting is dependent on the 25SC setting. The minimum 25AC setting is 32•25SC. This limitation is due to the 4.5-cycle synchronizing security check. The synchronous conditions must be true for 4.5 cycles before the breaker can close. The faster the slip frequency, the greater the angle change in 4.5 cycles. The setting limitation makes sure a successful close is possible with the given settings.

Maximum Slip Frequency for Manual Close (25SM)–Scheme 2

Range: 0.005–0.500 Hz in 0.001-Hz steps

Two synchronizing elements are provided to separate automatic and manual close operation control. Set 25SM to the maximum allowable slip frequency for manual close conditions (MCLOSE input). The slip frequency is set in hertz (cycles/second). For timing considerations, a slip of 0.1 Hz is equivalent to 0.6° per power system cycle. An acceptable slip is dependent on the application. For synchronizing two parts of the same system, the slip will be very close to zero. Set 25SM in this case to 0.03 Hz.

The slip frequency setting determines the minimum angle setting allowed for 25AM, so do not set 25SM to its highest value just to desensitize the synchronism supervision. If 25SM is set to 0.5, the minimum angle for 25AM will be 16°.

Maximum Manual Close Angle (25AM)–Scheme 2

Range: 32•25SM to 90° (min = 1) in 0.1° steps

Two synchronizing elements are provided to separate automatic and manual close operation control. Set 25AC to the maximum allowable angle difference for manual close conditions (MCLOSE input). The SEL-352 Relay will close an output contact based on the slip frequency and breaker close time so that the two systems are somewhere within the window. If the two systems are slipping by at a consistent rate, the SEL-352 Relay will initiate the close so that the breaker closes on the leading edge of the window. For synchronizing two parts of the same system, the angle difference will be very close to zero. Set 25AC in this case to 30° or less.

The minimum 25AM setting is dependent on the 25SM setting. The minimum 25AM setting is 32•25SM. This limitation is due to the 4.5-cycle synchronizing security check. The synchronous conditions must be true for 4.5 cycles before the breaker can close. The faster the slip frequency, the greater the angle change in 4.5 cycles. The setting limitation makes sure a successful close is possible with the given settings.

Synchronizing Phase (SYNCP)–Scheme 2

Range: A, B, C

This setting determines whether the synchronism check logic uses Vx, Vy voltages and X59H, X59L, and Y59L elements from A-phase, B-phase, or C-phase.

Synchronism Timer Dropout (SYNCdo)–Scheme 2

Range: 0–99999 cycles in 1/4-cycle steps

The SEL-352 Relay looks for synchronous conditions for a certain time after the CLOSE input is received. Set SYNCdo to the time desired.

When determining the setting, consider the allowable slip and method of indicating a closed breaker. The SYNCdo time needs to be long enough to allow the systems to slip past each other one complete revolution. If the breaker does not close, the relay can generate a second close pulse if the SYNCdo time has not expired.

Scheme 2 logic disables the synchronizing element once the breaker closes based on the auxiliary inputs. Refer to the synchronism check logic diagram in ***Section 5: Control Logic***. If auxiliary inputs are not available or are not reliable, you must consider another method for disabling the synchronism check element to avoid getting two close pulses.

For systems expecting zero slip, set SYNCdo = 2 cycles.

Point-On-Wave Timer Pickup (PCApu, PCBpu, PCCpu)–Scheme 2

Range: 0.00–40.00 ms in 0.01-ms steps

Set these pickup timers based on the delay you want to accommodate breaker closing time in the point-on-wave closing. The SEL-352 Relay output contact closes within 200 µs if one of the fast outputs is used. The contact closes at the point on the wave that the logic designates. Positive and negative peak closing logic uses these timers.

The logic closes the output contact at a positive peak for logic detection of a positive trapped charge, and it closes the output contact at a negative peak for a negative trapped charge. These timers provide the delay for the breaker close time and any offset to move the closing point to another point on the wave.

Zero-Crossing Timer Pickup (ZCApu, ZCBpu, ZCCpu)–Scheme 2

Range: 0.00–40.00 ms in 0.01-ms steps

Set these pickup timers based on the delay you want to accommodate breaker closing time in the point-on-wave closing. The SEL-352 Relay output contact closes within 200 µs if one of the fast outputs is used. The contact closes at the point on the wave that the logic designates. The positive and negative going zero-crossing closing logic uses these timers.

The default logic closes the output contact at a negative going zero crossing for failure of the logic to detect any trapped charge. The positive going zero-crossing element is not used. These timers provide the delay for the breaker close time and any offset to move the closing point to another point on the wave.

Controlled Close Output Timers (CLSA, CLSB, and CLSC)–Scheme 2

Set CLSA, B, and C to the output contact that will provide the point-on-wave closing. It is recommended that three of the fast, high current interrupting output contacts be used for point-

on-wave closing. These are available on Interface Board 5. See ***Section 2: Installation***. The logic and output contact operations occur in 200 µs or less. This output contact assignment is different from the standard output contact assignments (OUT101 = 86BFT). The point-on-wave logic directly controls the output contact hardware specified by the close settings CLSA, B, and C. The standard output assignments also control the output contacts, but only every 1/8 cycle. CLSA, B, and C control the outputs immediately. The default settings are OUT301, OUT302, and OUT303.

Setting Calculation

Point-On-Wave Timer Pickup (PCApu, PCBpu, PCCpu)–Scheme 2

Detection of a positive trapped charge causes the logic to close the relay output contact at a positive peak. For negative trapped charge, the logic closes the output contact at a negative peak. The PCApu timer provides the delay for the breaker close time and any offset to move the closing point to another point on the wave.

For example, with a Tclose (nominal closing time of the breaker) time of 33 ms (2 cycles) and a setting of PCApu = 0, the breaker will close at the appropriate peak 2 cycles after the output contact closes. However, if the Tclose time is 29 ms (1.75 cycles), the breaker would close 1/4 cycle before the peak.

To set PCApu for breaker and offset times that are not multiples of 1 cycle, subtract the fractional part from 1 cycle and set PCApu to this number. For example, the 1.75-cycle breaker requires a PCApu setting of 1 minus the fractional part of 1.75 (0.75), which equals 0.25 (1–0.75 = 0.25). PCApu is set in ms; therefore, PCApu = 4.17 ms for a nominal 60 Hz system.

An offset may be included in the timer as well. For example, a breaker that nominally closes in 38.9 ms but has a tolerance of ±0.5 ms for temperature variation, and +1/–2 ms for control voltage variation, needs an offset to provide the best closing results. The total error band is +1.5/–2.5 ms. This error band should be centered around the point of closing. It needs to shift 0.5 ms in the positive direction. Set PCApu = [1 – fractional part of (38.9/16.67)] • 16.67 + 0.5 = 11.61 ms.

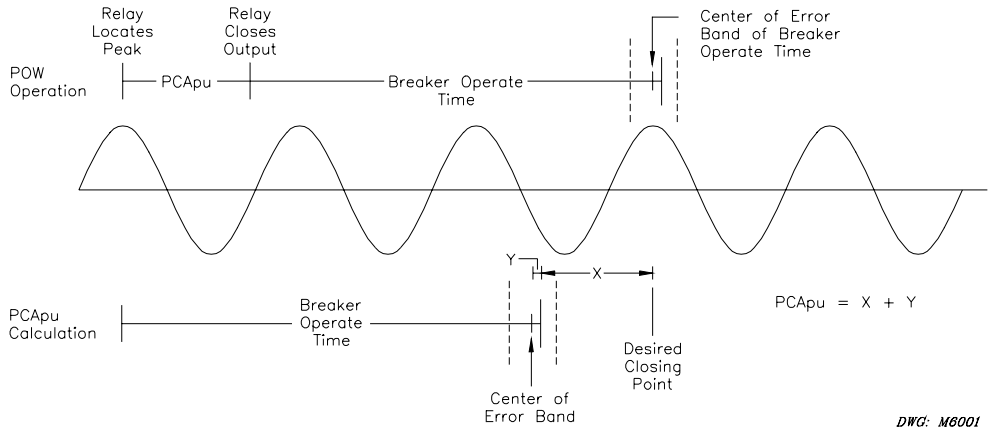

Figure 4.10: Point-On-Wave Timer Calculation

X = [1 – fraction of (Nominal Breaker Close Timer / 16.67)] • 16.67

$$Y = \text{Adjustment for centering error band} = \frac{\left|\text{NegError}\right| + \left|\text{PosError}\right|}{2}$$

If the negative error is greater than the positive error, Y is positive.

If the positive error is greater than the negative error, Y is negative.

Setting of the B-phase timer is similar to that for the A-phase timer. The relay performs the adjustment for the 120° phase shift between A-phase and B-phase. Refer to the A-phase calculations. If all three phases are to close at the same point on their corresponding voltage waveform, and within the same cycle interval, set all three timers to the same value. This will result in A-phase closing first, B-phase second, and C-phase third. If you want a different order, add a 1-cycle offset to the phase that needs to be delayed.

Setting of the C-phase timer is similar to that for the A-phase timer. The relay performs the adjustment for the 240° shift between A-phase and C-phase. Refer to the A-phase calculations. If all three phases are to close at the same point on their corresponding voltage waveform, and within the same cycle interval, set all three timers to the same value. This will result in A-phase closing first, B-phase second, and C-phase third. If you want a different order, add a 1-cycle offset to the phase that needs to be delayed.

Zero-Crossing Timers Pickup (ZCApu, ZCBpu, ZCCpu)–Scheme 2

The logic closes the relay output contact at a negative going zero crossing when it detects no trapped charge. The positive going zero-crossing element is not used. ZCApu provides the delay for the breaker close time and any offset to move the closing point to another point on the wave.

For example, with a Tclose (nominal closing time of the breaker) time of 33 ms (2 cycles), and a setting of ZCApu = 0, the breaker will close at the zero crossing 2 cycles after the output contact closes. However, if the Tclose time is 29 ms (1.75 cycles), the breaker would close 1/4 cycle before the zero crossing.

The zero-crossing timers work like the peak-crossing timers. Refer to Figure 4.10 for a timing diagram. The difference is that the output of the relay occurs at the zero crossing instead of the peak.

Setting of the B-phase timer is similar to that for the A-phase timer. The relay performs the adjustment for the 120° shift from A-phase to B-phase. Refer to the A-phase calculations. If all three phases are to close at the same point on their corresponding voltage waveform, and within the same cycle interval, set all three timers to the same value. This will result in A-phase closing first, B-phase second, and C-phase third. If you want a different order, add a 1-cycle offset to the phase you need to delay.

Setting of the C-phase timer is similar to that for the A-phase timer. The relay performs the adjustment for the 240° shift from A-phase to C-phase. Refer to the A-phase calculations. If all three phases are to close at the same point on their corresponding voltage waveform, and within the same cycle interval, set all three timers to the same value. This will result in A-phase closing

first, B-phase second, and C-phase third. If you want a different order, add a 1-cycle offset to the phase you need to delay.

RETRIPPING

Application Description

The SEL-352 Relay default logic provides two retripping schemes. Scheme 1 is an instantaneous retrip and Scheme 2 is a time-delayed, current-supervised retrip. Use the **SET** command to modify these schemes for your application.

Retripping is a cost-effective, secondary attempt to open a circuit breaker prior to breaker failure protection resulting in clearing of the entire bus and remote breakers. Many conditions may cause a breaker to fail to respond to a trip signal. Faulty breaker mechanical components, open trip coil, shorted trip coil, failed auxiliary contact, low battery dc, and open trip coil circuit are all possible conditions that may cause a breaker not to open. Some of these conditions will require that all adjacent breakers be opened, but some of the conditions may only require another trip signal. Some breakers have multiple trip coils that are energized with a retrip signal. A retrip signal provides partial redundancy for the trip coil circuitry. A separate tripping dc and trip coil provide full tripping circuit redundancy.

Retripping also provides security during inadvertent breaker failure initiation. If the trip input is inadvertently asserted, the retrip logic will attempt to trip the breaker prior to clearing the bus.

Operating Characteristic

Scheme 1 (Instantaneous Retrip)

Relay Word elements RTA, RTB, and RTC simply follow the input assignments TRIPA, TRIPB, and TRIPC, respectively.

Scheme 2 (Delayed Retrip)

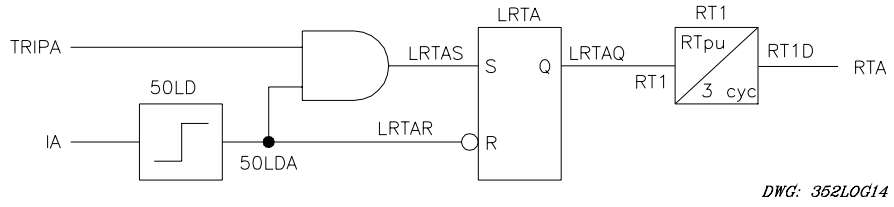

Figure 4.11: Circuit Breaker Retrip Logic (Scheme 2), A-Phase

Setting Description

Trip Inputs (TRIPA, TRIPB, and TRIPC)

Use the **SET G <ENTER>** command to associate the three programmable breaker failure initiate logic inputs (TRIPA, TRIPB, TRIPC) with physical inputs. Use any optoisolated input to control these Relay Word bits. For example, if IN101 is used to indicate A-phase trip initiation, set TRIPA = IN101. Repeat this for each input. The input settings are actually SELOGIC control equations. Use any combination of Relay Word bits according to the SELOGIC control equation criteria in ***Section 5: Control Logic***.

Retripping Scheme Selection (RTPLOG)

Range: OFF, 1, 2, CUSTOM

Set RTPLOG to 1 to enable the instantaneous retrip logic. As soon as one of the trip inputs is received, the SEL-352 Relay asserts the retrip outputs RTA, RTB, and RTC. Put these Relay Word bits in an output contact equation such as OUT305 = RTA + RTB + RTC for three-pole retrip applications. Use three output contacts, one for each retrip bit, for single-pole retripping. No other settings are required.

Set RTPLOG to 2 to enable the time-delayed retrip logic. As soon as one of the trip initiation inputs is received and current is flowing through the breaker, a timer is started. When the timer expires and the current has not dropped out, the retrip outputs will assert. Again, as in Scheme 1, set the retrip bits to an output contact.

Modify the default logic by setting RTPLOG = CUSTOM. When set to CUSTOM, all settings are shown including the SELOGIC control equations. Use these settings for a modified retrip logic, or use it for an entirely different application. The default setting is RTPLOG = 1.

Load Detector (50LD)

Range: 0.10–45.00 A in 0.01-A steps (5 A)
0.02–9.00 A in 0.01-A steps (1 A)

The delayed retripping logic uses the load current detector 50LD setting, but you set the value for this setting along with the load current protection logic. Use **SET <ENTER>** to access the 50LD setting.

Set the 50LD (in settings for the load current protection logic) based on the same criteria as outlined for the load current protection logic in ***Section 3: Breaker Logic***.

Retrip Timer Pickup (RTpu)

Range: 0–16383 cycles in 1/4-cycle steps

The RTpu timer setting defines the time interval between receipt of the trip initiation and assertion of the retrip bits RTA, RTB, and RTC. Consider the nominal breaker trip time, the retrip circuit, and the FCpu setting (timer for breaker failure during fault conditions).

Our example uses Scheme 1 because of the lack of margin between the first attempt at tripping the breaker and the breaker failure timer. A two-cycle breaker with a four-cycle breaker failure setting does not leave enough time to initiate a time-delayed retrip. In our example, the instantaneous retrip could be a completely redundant trip coil and circuit. Use time-delayed retripping if there is adequate margin between the first trip and breaker failure tripping. If there is not enough margin, use instantaneous retripping.

LOCKOUT RELAY CONTROL

Application Description

After detecting a breaker failure condition, all adjacent breakers must open to clear the fault if one existed, the breaker must be isolated, and then the system must be restored appropriately. There are many methods for accomplishing this, but two examples follow:

Example 1

1. Relay trips all adjacent breakers through a lockout auxiliary relay
2. Operator isolates the failed breaker with manual disconnects
3. Operator manually resets the lockout relay
4. Operator restores the system by closing breakers

Example 2

1. Relay trips all adjacent breakers through a lockout auxiliary relay
2. Relay trips motor-operated disconnects to isolate the breaker
3. Relay electrically resets the lockout relay
4. Automated reclosing restores the system

The two examples describe a range of control from a mostly manual system to a fully automated system. The SEL-352 Relay lockout relay control supports either of these schemes and variations of these schemes. To modify Scheme 1 or 2 for your application, use the **SET** command.

Operating Characteristic

Lockout relay trip and reset logic is provided for installations with and without automatic breaker isolation schemes.

Use Scheme 1 (Figure 4.12) for breaker failure tripping and “Safe to Reset Lockout Relay” conditions.

Use Scheme 2 (Figure 4.14) to automatically isolate the failed breaker with motor-operated disconnects (MOD). The SEL-352 Relay trips the MOD when current drops below a settable threshold. This scheme also can be used to indicate “Safe to Disconnect” conditions for manual disconnect switches.

Scheme 1 (No MOD Trip)

Figure 4.12 shows the logic used to assert the 86BFT output and the 86RS output in the Relay Word when MOD tripping is not used.

The 86BFT trip output asserts as soon as a trip condition occurs according to the M86T SELOGIC control equation. The M2 timer begins timing, waiting for the trip conditions to reset. After the trip conditions reset and the M2 timer has expired, the 86BFT trip output is reset (deasserted). After five seconds of the reset condition (no trip and no current), the 86RS output asserts to reset a lockout relay or provide a "safe to reset" indication. The M1 timer deasserts the 86RS output in one second. If a thermal failure of a trip or close resistor (CTF, TTF) exists, the 86RS output will not assert.

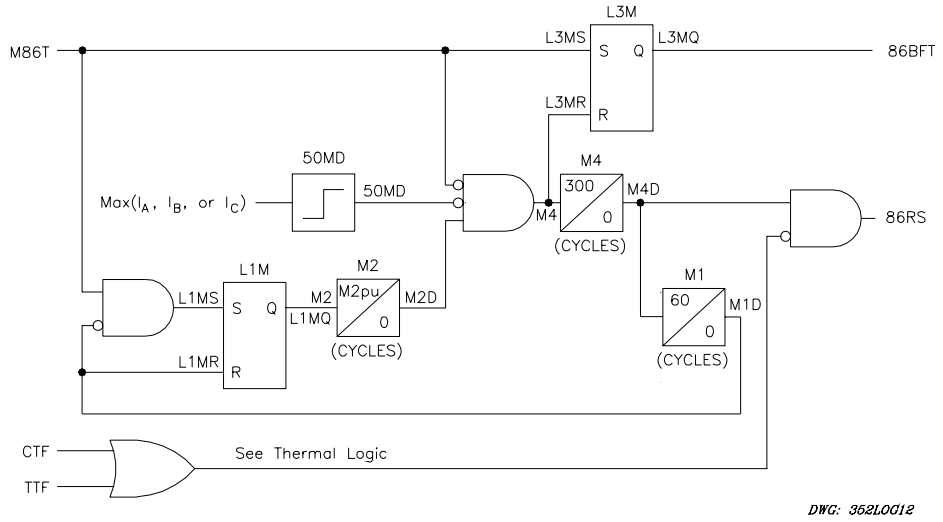

Figure 4.12: 86BF TRIP and Reset Logic (Scheme 1)

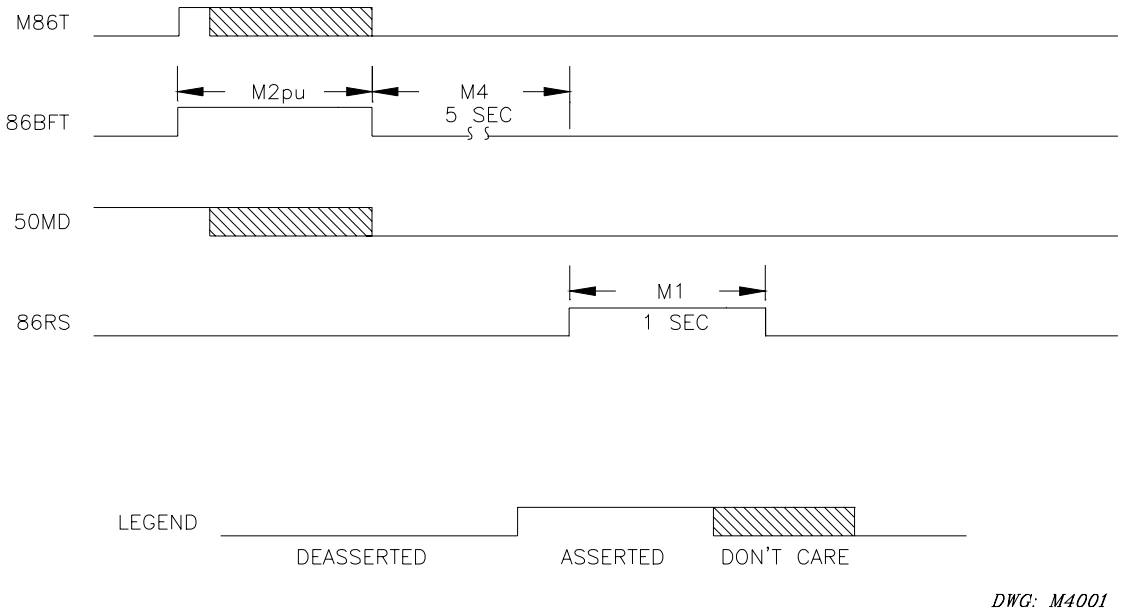

Figure 4.13: Lockout Relay Control Scheme 1 Timing Diagram

Scheme 2 (MOD Trip Used)

Figure 4.14 shows the logic used to assert the 86BFT output and the 86RS output in the Relay Word when MOD tripping is used.

The 86BFT trip output asserts as soon as a trip condition occurs according to the M86T equation. The M2 timer begins timing, waiting for the current to drop below the 50MD setting. After the current drops out and the M2 timer has expired, the MOD is tripped with the MDT output or it can be used to indicate a "safe to disconnect" condition. At the same time MDT asserts, the M3 timer starts timing, waiting for the MOD to open or the current to drop below the 50LD setting. After this occurs and the M3 timer expires, the 86BFT trip output is reset (deasserted). After five seconds of the reset condition (no trip and no current), the 86RS output asserts to reset a lockout relay or provide a "safe to reset" indication. One second after the 86RS asserts, the M1 timer deasserts the 86RS output and the MDT output.

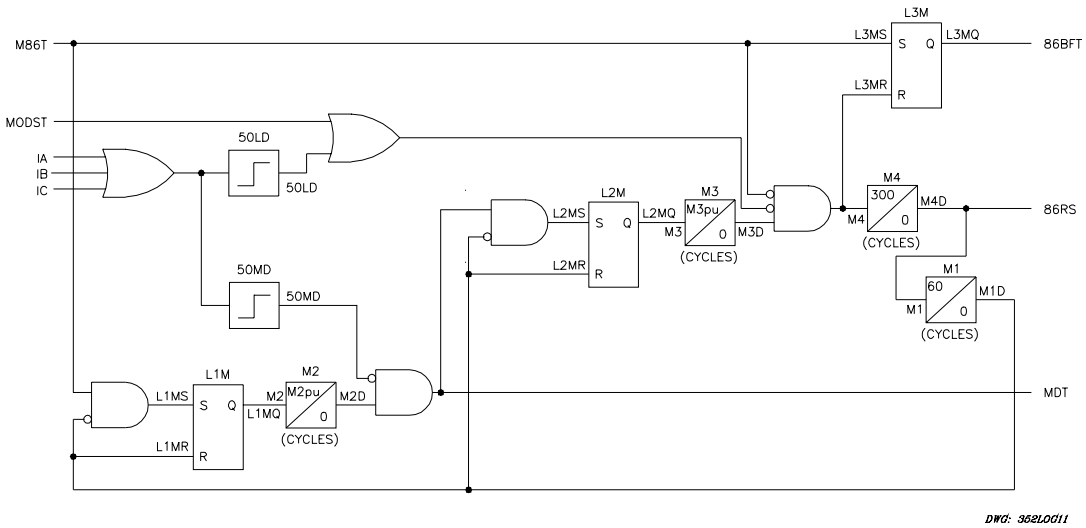

Figure 4.14: Lockout Relay Control and MOD Trip Logic (Scheme 2)

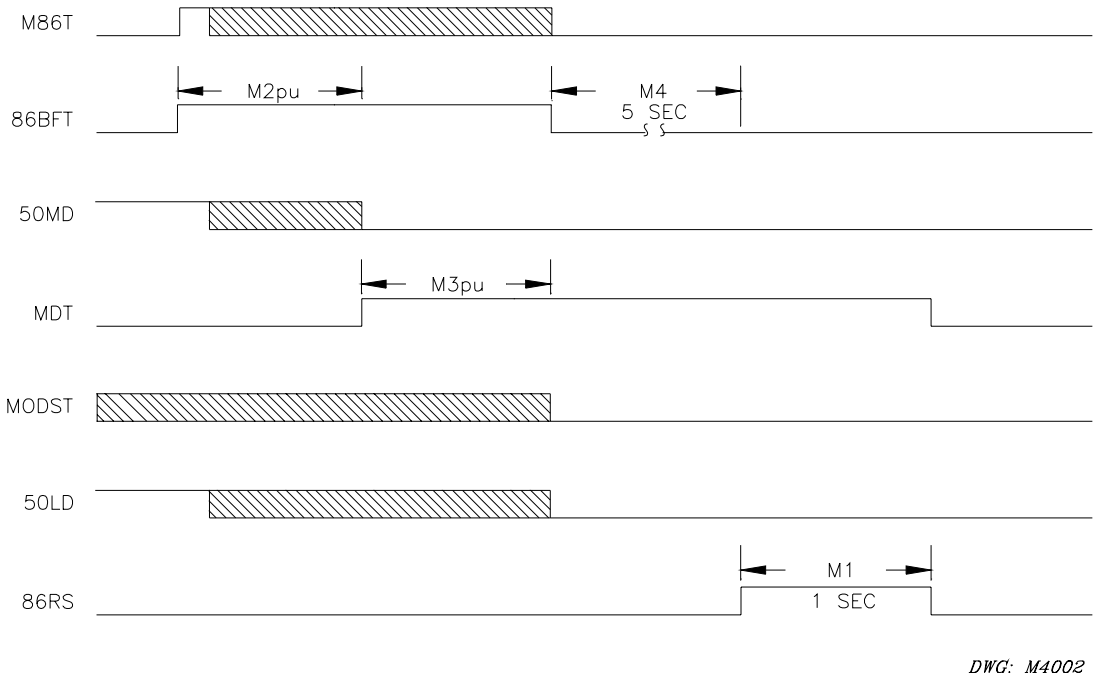

Figure 4.15: Lockout Relay Control Scheme 2 Timing Diagram

Setting Description

Motor-Operated Disconnect Input Status (MODST)–Scheme 2

Use the **SET G <ENTER>** command to define the Motor-Operated Disconnect Input Status (MODST). The lockout relay control logic uses one programmable input for Scheme 2 (MODST). Scheme 1 of the lockout relay control logic does not need any input definitions. Define MODST to indicate when the motor-operated disconnect is closed or open. This input works in the same way as the 52A input definitions. Use any optoisolated input to control the Relay Word bit MODST. For example, if IN101 is used to indicate that the MOD is closed, set MODST = IN101. When control voltage is applied to IN101, the SEL-352 Relay determines that the MOD is closed. The input settings are actually SELOGIC control equations. Use any combination of Relay Word bits according to the SELOGIC control equation criteria in ***Section 5: Control Logic***.

Breaker Failure Trip Mask (M86T)

Select which failures trip the lockout relay by setting the M86T equation accordingly. M86T is the mask (criteria) for asserting 86BFT (lockout relay breaker failure trip). The output of each protection logic scheme that is supposed to assert 86BFT must be set in M86T. For example, if only the fault current logic is intended to drive the lockout relay, then M86T = FBF. The Relay Word bit FBF is the output of the fault current breaker failure detection logic. No other logic would control the lockout relay with this setting.

- Decide which schemes should drive the lockout relay.
- Verify the output Relay Word bit for each scheme (See ***Section 5: Control Logic***).

- Set M86T using the SELOGIC control equation, i.e., M86T = FBF + LBF + FOBF + UBBF.

MOD Operating Current (50MD)

Range: 0.10–45.00 A in 0.01-A steps (5 A)
0.02–9.00 A in 0.01-A steps (1 A)

Set the 50MD overcurrent setting to pick up when the protected breaker current exceeds the current break rating of the isolating disconnects. The lockout relay will not reset until current has dropped below 50MD along with other conditions. A recommended setting is to require that all breakers are open, and that the failed breaker is isolated with no current flowing through it, 50MD = 0.1 A for a nominal 5 A relay, 0.02 A for a nominal 1 A relay.

Trip and Reset Logic Scheme Selection (TRLOG)

Range: OFF, 1, 2, CUSTOM

The SEL-352 Relay provides two lockout relay control schemes. Each scheme has a trip (86BFT) and reset (86RS) output. Scheme 2 also has an MOD trip output (MDT). All three of these Relay Word bits are used in output equations such as OUT301 = 86BFT.

Use the 86BFT output to energize a lockout relay or trip another breaker directly. Use the 86RS output to reset a lockout relay or indicate "OK to reset lockout relay." Use the MDT output to trip an MOD to isolate the failed breaker or use it for a "safe to disconnect" indication.

Timer 2 (M2pu)

Range: 0–8191 cycles in 1/8-cycle steps

Set M2pu long enough for breaker isolation and for the current to drop below the 50MD setting. Take into account the lockout relay operate time, the operate times of any additional auxiliary relays, the nominal tripping time of the slowest switching device to isolate the breaker, the time for the 50MD element to drop out, and some margin. A very conservative setting is M2pu = 600 cycles.

Refer to the logic diagrams and timing diagrams in ***Section 5: Control Logic***.

Timer 3 (M3pu)–Scheme 2

Range: 0–8191 cycles in 1/8-cycle steps

Scheme 2 uses a second timer, M3pu, to provide time for the MOD to completely open before the lockout relay is reset. Set M3pu longer than the time required for the MOD to completely open. A recommended setting is 120 percent of the MOD opening time, M3pu = 1.2 • 500 cycles = 600 cycles.

A breaker alarm called "Current After MOD Trip" uses the M3 output, current, and the MOD status indication (MODST) to alarm for slow MODs.

Refer to the logic diagrams and timing diagrams in ***Section 5: Control Logic.***

OUTPUT CONTACT

All relay logic must be programmed to an output contact for external indication and control. For example, the 86BFT bit is the output of the lockout relay control logic. To use this logic, program an output contact to follow the 86BFT bit (OUT101 = 86BFT).

Note that all outputs will return to their de-energized state (SELOGIC control equation = 0) for approximately 1 second when settings are saved.

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TABLES

FIGURES

SECTION 5: CONTROL LOGIC

This section describes relay elements and logic with figures and accompanying text. Details on setting ranges and default settings are listed in ***Section 7: Setting the Relay***.

SIGNAL PROCESSING

The relay filters the current and voltage channels and samples the signals 64 times per power system cycle. The relay stores the analog low-pass filtered samples for event reporting. The analog low-pass filter has a 3 dB cutoff at 1200 Hz. Refer to Figure 1.3 in ***Section 1: Introduction and Specifications*** for a graph of the analog low-pass filter. The microprocessor digitally filters each signal using a cosine digital filter, except for the 50FT elements where a half-cosine digital filter is used.

Frequency Tracking Specification

All SEL-352 Relay calculations and decisions are performed every 1/8 or 1/4 of a power system cycle depending on the logic. Refer to Table 5.5 for relay logic processing order and intervals.

The SEL-352 Relay NFREQ setting determines the nominal frequency of the system (50, 60 Hz). As the power system frequency fluctuates, the relay tracks to that frequency to determine processing intervals. With NFREQ = 50, the relay tracks over the range of 45–55 Hz. With NFREQ = 60, the relay tracks over the range of 55–63 Hz. If the system frequency goes beyond the tracking range, the relay stops tracking at that boundary until the system frequency returns.

The tracking frequency follows the A-phase voltage frequency of the voltage source that is greater than the 59L setting. If both X and Y voltage sources satisfy this criterion, the relay calculates an average frequency using both X and Y voltage input zero crossings.

The event reports display the tracking frequency at the time of trigger.

RELAY LOGIC OVERVIEW

The SEL-352 Relay is fully programmable for complete custom logic control but has selectable fixed logic for secure traditional breaker failure schemes. Minimal fixed logic settings make the relay easy to use. The optional custom logic provides flexibility when it is needed.

As an overview to the relay, consider relay function in four separate parts. Link the four parts together to make the relay complete. These four parts for overview purposes are the Input Assignments, Scheme Logic, Trip and Close Logic, and Output Assignments. Refer to Figure 5.1 for a block diagram of this overview. The Analog Measurements are part of the Scheme Logic.

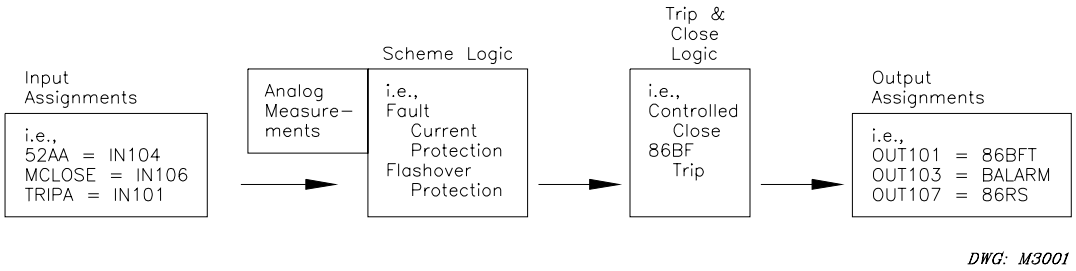

Figure 5.1: SEL-352 Relay Logic Overview Block Diagram

The relay outputs are all programmable except for the ALARM output contact. Therefore, the relay will only close and open output contacts according to the assignments you give them. These assignments usually are selected from the output of the Trip and Close Logic. The predefined Trip and Close Logic allows for easy application, but the logic also can be customized. The Trip and Close Logic gets information from the Scheme Logic, which also can be customized. Scheme Logic gets information from analog measurements and/or digital inputs. The relay continuously monitors all digital inputs. Assign digital inputs for specific functions.

As an example, the relay continuously monitors all digital inputs, but you can program the relay to use IN104 for a specific function. Any time IN104 changes state, we want the relay to know that the breaker has changed state (opened or closed). The Input Assignment would be 52AA=IN104 for A-phase. The fixed scheme logic in the relay uses 52AA to make protection decisions along with the analog measurements. The decision, or output of the fixed scheme logic, is used by the Trip and Close Logic. The decision, or output of the Trip and Close Logic, is the assertion or deassertion of Relay Word bits. The following discussion describes the Relay Word.

Up to this point, the relay has not done anything physical. It has processed data but not acted on the information. To program the relay to open or close an output contact, you must assign one of these Relay Word bits to an output contact like OUT101 = 86BFT, which says to close output contact labeled OUT101 when the breaker failure lockout trip asserts. This output would typically drive a lockout relay.

RELAY WORD BITS AND SELOGIC® CONTROL EQUATIONS

Relay Word Bits

The outputs of the logic in most of the figures in this section are Relay Word bits. Relay Word bits have label names (e.g., Y59L3, 50LD, etc.). They are logic points that can have a state of:

1 (logical 1) or 0 (logical 0)

depending on the operation of the associated logic. Logical 1 represents an element being picked up, timed out, or otherwise asserted. Logical 0 represents an element being dropped out or otherwise deasserted. All Relay Word bits are shown in Table 5.1. The asterisk (*) in the Relay Word is a placeholder for unused Relay Word bits. The Relay Word bits are arranged alphabetically in ***Appendix F: Relay Word*** with descriptions and Relay Word row locations.

Row 16 Relay Word bits (BCW, 50R, 50RA, 50RB, and 50RC) are only available in the SEL-352-2 Relay.

Table 5.1: Relay Word

Row	Relay Word Labels							
	Front-Panel Targets (not for use in SELOGIC Control Equations)							
0	EN	PF	86BFT	86RS	TRIP	CLOSE	52A	MOD
1	FAULT	LOAD	UBAL	FLASH	THERM	A	B	C
	General Elements							
2	Y59L3	X59L3	50LDC	50LDB	50LDA	50FTC	50FTB	50FTA
3	87THA	87FOA	Y27D3	X27D3	50N	50MDC	50MDB	50MDA
4	47Q	37OP	25T	46P	87THC	87FOC	87THB	87FOB
5	X59LC	X59HC	X27DB	X59LB	X59HB	X27DA	X59LA	X59HA
6	ZERO	Y27DC	Y59LC	Y27DB	Y59LB	Y27DA	Y59LA	X27DC
7	ONE	50MNC	50MNB	50MNA	87F	87H	87TH	X59H
8	25M	25C	46C	46B	46A	50MD	50LD	50FT
9	Y47Q	X47Q	37OPC	37OPB	37OPA	87HC	87HB	87HA
10	CCMD	TCMD	XNTC	XPTC	XNTB	XPTB	XNTA	XPTA
11	*	*	YNTC	YPTC	YNTB	YPTB	YNTA	YPTA
12	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1
13	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9
14	LB8	LB7	LB6	LB5	LB4	LB3	LB2	LB1
15	LB16	LB15	LB14	LB13	LB12	LB11	LB10	LB9
16	*	*	*	BCW	50R	50RC	50RB	50RA
17	*	*	IN106	IN105	IN104	IN103	IN102	IN101
18	IN208	IN207	IN206	IN205	IN204	IN203	IN202	IN201
19	IN216	IN215	IN214	IN213	IN212	IN211	IN210	IN209
20	IN308	IN307	IN306	IN305	IN304	IN303	IN302	IN301
21	IN316	IN315	IN314	IN313	IN312	IN311	IN310	IN309
22	MCLOSE	CLOSE	TRIP3	TRIPC	TRIPB	TRIPA	SS2	SS1
23	*	LODCT	LOD2	LOD1	MODST	52AC	52AB	52AA
	SELOGIC Control Equation SET A Elements							
24	L1CR	L1CS	L1BQ	L1BR	L1BS	L1AQ	L1AR	L1AS
25	*	T1CD	T1C	T1BD	T1B	T1AD	T1A	L1CQ
26	*	*	*	*	*	SAC	SAB	SAA
	Fault Current Protection Elements							
27	LFAR	LFAS	TTCD	TTC	TTBD	TTB	TTAD	TTA
28	*	LFCQ	LFCR	LFCS	LFBQ	LFBR	LFBS	LFAQ
29	*	*	FCCD	FCC	FCBD	FCB	FCAD	FCA
	Load Current Protection Elements							
30	LLCR	LLCS	LLBQ	LLBR	LLBS	LLAQ	LLAR	LLAS
31	LDA	LPCD	LPC	LPBD	LPB	LPAD	LPA	LLCQ
32	L52Q	L52R	L52S	LDCD	LDC	LDBD	LDB	LDAD
33	*	*	*	*	AFD	AF	APD	AP

				Resistor Thermal Protection Elements				
34	LTAR	LTAS	OPCD	OPC	OPBD	OPB	OPAD	OPA
35	*	LTCQ	LTCR	LTCS	LTBQ	LTBR	LTBS	LTAQ
36	*	*	CRMEC	CRMEB	CRMEA	TRMEC	TRMEB	TRMEA
37	*	KTRK	26TFC	26TFB	26TFA	26CFC	26CFB	26CFA
38	*	*	26TPC	26TPB	26TPA	26CPC	26CPB	26CPA
				Flashover Protection Elements				
39	F2AD	F2A	F1CD	F1C	F1BD	F1B	F1AD	F1A
40	F3BD	F3B	F3AD	F3A	F2CD	F2C	F2BD	F2B
41	LHBQ	LHBR	LHBS	LHAQ	LHAR	LHAS	F3CD	F3C
42	LVBR	LVBS	LVAQ	LVAR	LVAS	LHCQ	LHCR	LHCS
43	FPBD	FPB	FPAD	FPA	LVCQ	LVCR	LVCS	LVBQ
44	FFCD	FFC	FFBD	FFB	FFAD	FFA	FPCD	FPC
				Unbalance Protection Elements				
45	*	UPAD	UPA	LUQ	LUR	LUS	UCD	UC
46	UFBD	UFB	UFAD	UFA	UPCD	UPC	UPBD	UPB
47	*	*	*	*	*	*	UFCD	UFC
				Loss-of-Dielectric Protection Elements				
48	*	*	LT3D	LT3	LT2D	LT2	LT1D	LT1
				Controlled Close Elements				
49	MCT	RCCD	RCC	RCBD	RCB	RCAD	RCA	RCLS
50	PCPA	SCTD	SCT	SYNCTD	SYNCT	CCTD	CCT	MCTD
51	ZCPB	ZCNA	ZCPA	PCNC	PCPC	PCNB	PCPB	PCNA
52	*	SYNCEN	CTCD	CTBD	CTAD	ZCNC	ZCPC	ZCNB
				Breaker Alarm Elements				
53	CAMT	BPF	BDNC	TWO	CWO	52ACV	FCRS	FTRS
54	*	*	*	BALRM	PTD	SC	ST	MCC
				Circuit Breaker Retrip Elements				
55	LRTCR	LRTCS	LRTBQ	LRTBR	LRTBS	LRTAQ	LRTAR	LRTAS
56	*	RT3D	RT3	RT2D	RT2	RT1D	RT1	LRTCQ
				SELOGIC Control Equation SET B Elements				
57	L2CR	L2CS	L2BQ	L2BR	L2BS	L2AQ	L2AR	L2AS
58	L3CS	L3BQ	L3BR	L3BS	L3AQ	L3AR	L3AS	L2CQ
59	T2CD	T2C	T2BD	T2B	T2AD	T2A	L3CQ	L3CR
60	L4CR	L4CS	L4BQ	L4BR	L4BS	L4AQ	L4AR	L4AS
61	L5CS	L5BQ	L5BR	L5BS	L5AQ	L5AR	L5AS	L4CQ
62	T3CD	T3C	T3BD	T3B	T3AD	T3A	L5CQ	L5CR
63	L6CR	L6CS	L6BQ	L6BR	L6BS	L6AQ	L6AR	L6AS
64	L7CS	L7BQ	L7BR	L7BS	L7AQ	L7AR	L7AS	L6CQ
65	*	*	*	SBC	SBB	SBA	L7CQ	L7CR
				Logic Output Elements				
66	UBBF	UBPF	FOBF	FOPF	CTF	TTF	LBF	LPF
67	RTC	RTB	RTA	CCC	CCB	CCA	LODBF	LODPF
68	*	*	*	*	*	*	*	FBF

				86BF Trip and Reset Elements				
69	M2D	M2	L1MQ	L1MR	L1MS	M1D	M1	M86T
70	L3MQ	L3MR	L3MS	M3D	M3	L2MQ	L2MR	L2MS
71	*	MER	86BFT	86RS	MDT	M4D	M4	*
72	*	*	*	*	*	CTC	CTB	CTA
				Contact Output Elements and Display Points				
73	!ALARM	OUT107	OUT106	OUT105	OUT104	OUT103	OUT102	OUT101
74	OUT201	OUT202	OUT203	OUT204	OUT205	OUT206	OUT207	OUT208
75	OUT209	OUT210	OUT211	OUT212	OUT213	OUT214	OUT215	OUT216
76	OUT301	OUT302	OUT303	OUT304	OUT305	OUT306	OUT307	OUT308
77	OUT309	OUT310	OUT311	OUT312	OUT313	OUT314	OUT315	OUT316
78	DP8	DP7	DP6	DP5	DP4	DP3	DP2	DP1
79	DP16	DP15	DP14	DP13	DP12	DP11	DP10	DP9

SELOGIC Control Equations

SELOGIC control equation settings create much of the logic structure of the relay. Certain scheme settings fix the SELOGIC control equations to a predetermined logic implementation. Select a predetermined scheme by turning it "ON" or selecting the scheme number in the settings. After review of these default schemes, select "CUSTOM" to customize the schemes for specific applications, if necessary. The diagrams in this section detail the predefined logic in the relay. See ***Section 7: Setting the Relay*** for a list of the predetermined SELOGIC control equation settings that may be customized.

SELOGIC control equation settings are written in Boolean algebra logic, combining Relay Word bits or Analog Compares together with different operators. (Analog Compares are discussed later in this section.) Parentheses can also be used in SELOGIC control equation settings. Use more than one set of parentheses in a given SELOGIC control equation setting, but they cannot be "nested" (parentheses within parentheses). Operators in a SELOGIC control equation setting are processed as shown in Table 5.2:

Table 5.2: Processing Order of SELOGIC Control Equation Operators

Operator	Logic Function
( )	parentheses
!	NOT
/	rising-edge detect
\	falling-edge detect
*	AND
+	OR

The rising-edge detect (/) and falling-edge detect (\) operators sense a transition of a Relay Word bit from one state to another, and output a logical 1 for a single processing interval if the change is detected. The rising-edge detect senses changes from 0 to 1, the falling-edge detect from 1 to 0. The new state must be in effect for one-quarter cycle to be recognized as a state change. The rising- and falling-edge detect operators cannot be used with Analog Compares, and each counts as two operators toward the maximum number of 550 (Group Setting Class) or 50 (Global Setting Class).

In addition to standard Relay Word bits, fixed logic values are available for SELOGIC control equations:

ONE (logical 1) or ZERO (logical 0) or NA (logical 0)

If a SELOGIC control equation setting is set equal to ONE, it is always "asserted/on/enabled." If a SELOGIC control equation setting is set equal to ZERO or NA, it is always "deasserted/off/disabled."

SELOGIC Control Equation Analog Compares

The SEL-352 Relay is capable of interpreting SELOGIC control equations that contain a special type of element, the Analog Compare. Use these elements in any SELOGIC control equation in the same manner as a Relay Word bit, except that the "/" and "\" operators may not be used with Analog Compares. The Analog Compare outputs a logical 1 when the compare statement is true, and a logical 0 when it is false. A SELOGIC control equation Analog Compare has the following format:

NAME OP VALUE

where

NAME is one of the valid analog names (see below).
OP is an arithmetic operator (<, <=, >, >=).
VALUE is either a fixed numerical value or another NAME scaled in the same units.

Examples of Analog Compare statements are IA>2.2 or VAX>=VAY. An equation using an Analog Compare might be written as SAA = IA>2.2 + 50LD, for example. In the ***Limitations of SELOGIC Control Equations*** discussion that follows, an Analog Compare counts as two elements, in determining the size of a SELOGIC control equation.

The following is a list of valid SEL-352 Relay analog names and their ranges. The first list is updated every eighth cycle.

RMS current magnitudes (IRMSA, IRMSB, IRMSC) are only available in the SEL-352-2 Relay.

Table 5.3: Valid Analog Compare Quantities

Name	Description	Range 5 A	Range 1 A	Decimal Places
IMAX, IMIN, IA, IB, IC	Phase current magnitudes	0.1–45 A (secondary)	0.02–9 A (secondary)	2
IHA, IHB, IHC	Half-cosine filtered phase current magnitudes	0.5–45 A (secondary)	0.1–9 A (secondary)	2
3I0	Sequence current magnitudes	0.1–45 A (secondary)	0.02–9 A (secondary)	2
VXMAX, VXMIN, VYMAX, VYMIN, VAX, VBX, VCX, VAY, VBY,	Phase voltage magnitudes	1–120 V (secondary)	1–120 V (secondary)	1

Name	Description	Range 5 A	Range 1 A	Decimal Places
VCY				
V1X, V1Y, V2X, V2Y	Sequence voltage magnitudes	2–140 V (secondary)	2–140 V (secondary)	1
POWMAX, POWA, POWB, POWC	Power	0.1–3400 W (secondary)	0.02–680 W (secondary)	2
DVMAX, DVA, DVB, DVC	Voltage differential	1–150 V (secondary)	1–150 V (secondary)	1
26TA, 26TB, 26TC, 26CA, 26CB, 26CC	Resistor thermal elements	0.01–1000 J (secondary)	0.002–200 J (secondary)	3
IRMSA, IRMSB, IRMSC	RMS current magnitude	0.5–45.0 A (secondary)	0.1–9.0 A (secondary)	2

A second set of analog values is updated within two seconds of changing.

Name	Description	Range 5 A or 1 A	Decimal places
ENRGTA, ENRGTB, ENRGTC, ENRGCA, ENRGCB, ENRGCC	Total energy dissipated	0.1–500000 MJ (primary)	2
CURRTA, CURRTB, CURRTC, CURRCA, CURRCB, CURRCC	Total current interrupted	0.1–500000 kA (primary)	2
TRPA, TRPB, TRPC, CLSA, CLSB, CLSC	Total number of trip or close operations	0–65535	0

Limitations of SELOGIC Control Equations

Any single SELOGIC control equation setting is limited to 17 Relay Word bits that can be combined together with the SELOGIC control equation operators listed in Table 5.2. If this limit must be exceeded, use a SELOGIC control equation variable (SnVm) as an intermediate setting step.

For example, assume that the trip equation (SELOGIC control equation trip setting M86T) needs more than 17 Relay Word bits in the associated equation setting. Instead of placing all Relay Word bits into M86T, program some of them into the SELOGIC control equation setting SBA. Next use the resultant SELOGIC control equation variable output (Relay Word bit SnVm) in the SELOGIC control equation trip setting, M86T.

The SELOGIC control equation settings in the Group settings are limited to no more than 550 elements. In the Global settings, they are limited to no more than 50 elements. Table 5.4 summarizes this information.

An attempt to set the relay with more than 17 operands will result in the message "Maximum of 17 elements allowed in a SELOGIC equation." The relay will then prompt the user to reenter the equation. An attempt to save Group settings with more than 550 Relay Word bits or Global settings with more than 50 Relay Word bits will result in the message "Too many SELOGIC elements." The relay will then return to the first nonhidden SELOGIC control equations for editing.

SELOGIC control equation settings that are set directly to 1 (logical 1) or 0 (logical 0) also have to be included in these limitations–each such setting counts as one element.

Table 5.4: Maximums for SELOGIC Control Equations

	Group Setting Class	Global Setting Class
Relay Word bits per Equation	17	17
Relay Word bits per Setting Class (including Rising- or Falling-Edge Operators)	550	50
Equations per Setting Class	258	15

SELOGIC Control Equation Set A Example

Objective: Set all 38 digital inputs to trigger an event report with the MER SELOGIC control equation.

Limitation: MER can only accept 17 Relay Word bits.

Solution: Use general-purpose SELOGIC control equations SAA, SAB, and SAC to expand the equation.

SAA = IN101 + IN102 + . . . + IN106
SAB = IN201 + IN202 + . . . + IN216
SAC = IN301 + IN302 + . . . + IN316
MER = SAA + SAB + SAC

SELOGIC Control Equation Operators Example

Objective: Use parentheses to simplify SELOGIC control equations.

Solution: Put "OR" conditions inside parentheses.

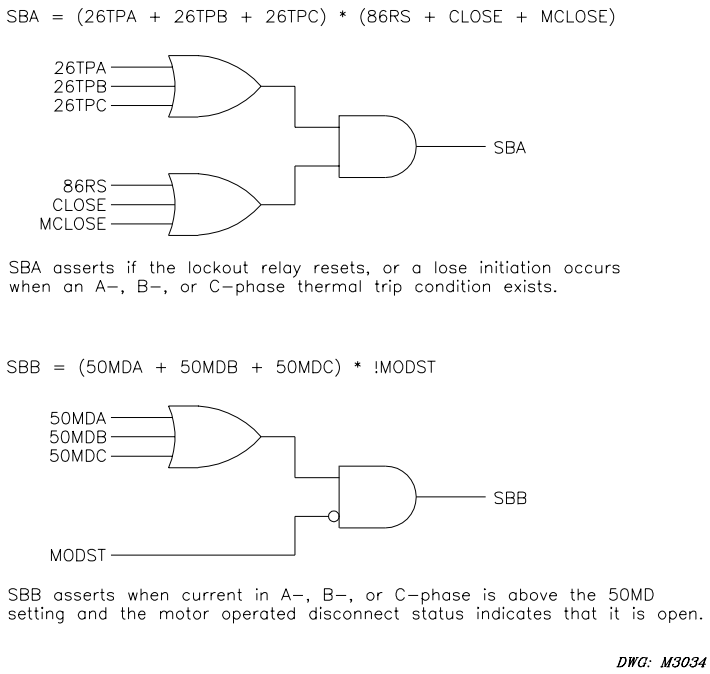

Figure 5.2: SELOGIC Control Equation Operators Example Diagrams

Processing Order and Processing Interval

The relay elements and logic are processed in the order shown in Table 5.5 (top to bottom). They are processed every 1/8 or 1/4 cycle depending on the logic element. Once a Relay Word bit is updated during a processing interval, it retains the state (logical 1 or logical 0) until it is updated again on the next 1/8- or 1/4-cycle pass.

Table 5.5: Processing Order of Relay Elements and Logic (top to bottom)

Relay Elements and Logic (see the Relay Word in Appendix F or Table 5.1)	Processing Interval
Targets (Relay Word Rows 0 and 1)	1/8 cycle
General Elements, Fixed Analog Comparisons (Relay Word Rows 2–11)	1/8 cycle
General Elements, Optoisolated Inputs (Relay Word Rows 17–21)	1/8 cycle
General Elements, Input Assignment Variables (Relay Word Rows 22–23)	1/8 cycle
General Elements, Remote Bits (Relay Word Rows 12 and 13)	1/8 cycle
General Elements, Local Bits (Relay Word Rows 14 and 15)	1/8 cycle
SELOGIC Control Equation SET A Elements (Rows 24–26)	1/8 cycle
Fault Current Protection Elements (Rows 27–29)	1/8 cycle
Load Current Protection Elements (Rows 30–33)	1/4 cycle
Resistor Thermal Protection Elements (Rows 34–38)	1/4 cycle

Relay Elements and Logic (see the Relay Word in Appendix F or Table 5.1)	Processing Interval
Flashover Protection Elements (Rows 39–44)	1/4 cycle
Unbalance Protection Elements (Rows 45–47)	1/4 cycle
Loss-of-Dielectric Protection Elements (Row 48)	1/4 cycle
Controlled Close Elements (Row 49–52)	1/4 cycle
Breaker Alarm Elements (Rows 53–54)	1/4 cycle
Circuit Breaker Retrip Elements (Rows 55–56)	1/4 cycle
SELOGIC Control Equation SET B Elements (Rows 57–65)	1/4 cycle
Logic Output Elements (Rows 66–68)	1/4 cycle
86BF Trip and Reset Elements (Rows 69–72)	1/8 cycle
Event Report Trigger (MER) (Row 71)	1/8 cycle
Contact Output Elements and Display Points (Rows 73–79)	1/8 cycle
Sequential Event Recorder Triggers (SER1–SER3) (not in Relay Word)	1/8 cycle

FIXED ANALOG COMPARISONS

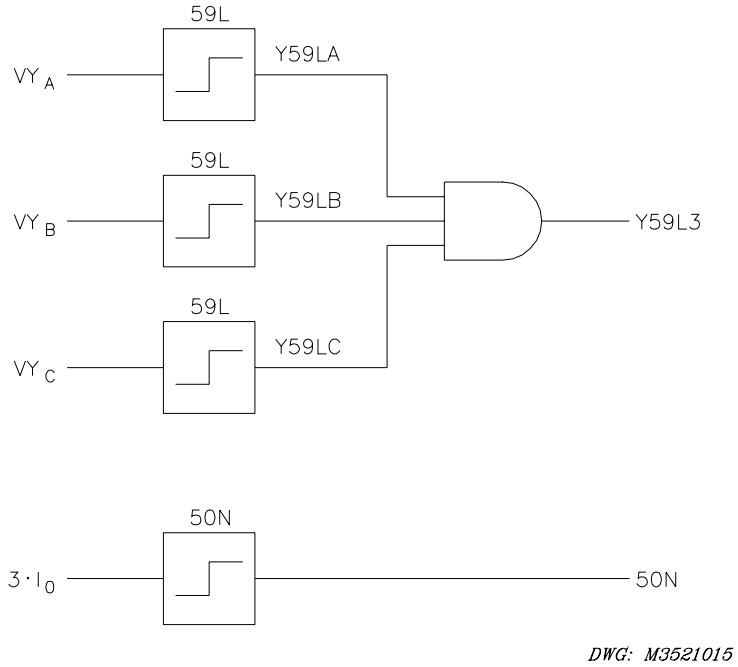

Figure 5.3: Analog Comparison Logic Examples

Many Relay Word bits assert based on a comparison of the analog input to a relay setting or the combination of analog quantities and/or settings. These comparisons are used throughout the relay logic and are represented in the logic diagrams by symbols similar to those in Figure 5.3.

Figure 5.3 shows that the Y-side A-, B-, and C-phase voltage inputs are compared to the 59L setting to determine the Y59LA, Y59LB, and Y59LC Relay Word bit status. If the A-phase RMS voltage exceeds the 59L setting, Y59LA becomes a logical 1. As soon as the magnitude of the voltage drops below the setting threshold, Y59LA returns to a logical 0. If Y59LA, Y59LB, and Y59LC pick up, the Y59L3 Relay Word bit asserts, indicating all three phases are high. Each of the general elements, other than the delay outputs, are processed every 1/8-cycle. Refer to ***Appendix F: Relay Word*** for a description of each individual Relay Word bit.

The analog comparison process has been expanded in this relay through the use of SELOGIC control equation Analog Compares, discussed earlier in this section.

OPTOISOLATED INPUTS

Relay Word bits IN101 through IN316 follow optoisolated inputs IN101 through IN316, respectively, if the input/output board configuration supports them. ***Section 2: Installation*** gives a description of the optional I/O boards that are available and the number of inputs they support. See Figure 5.4 for an example of an energized and de-energized optoisolated input and corresponding Relay Word bit states. Note the built-in pickup and dropout times of 0.125 cycles for energization or de-energization debounce. Use SELOGIC control equation timers for additional debounce time, if necessary.

There are no optoisolated input settings such as:

IN101 =
IN102 =

In Figure 5.4, optoisolated inputs IN101 and IN102 receive their function by how their corresponding Relay Word bits IN101 and IN102 are used in SELOGIC control equations such as in the input assignment variables. The optoisolated input elements are processed every 1/8 cycle.

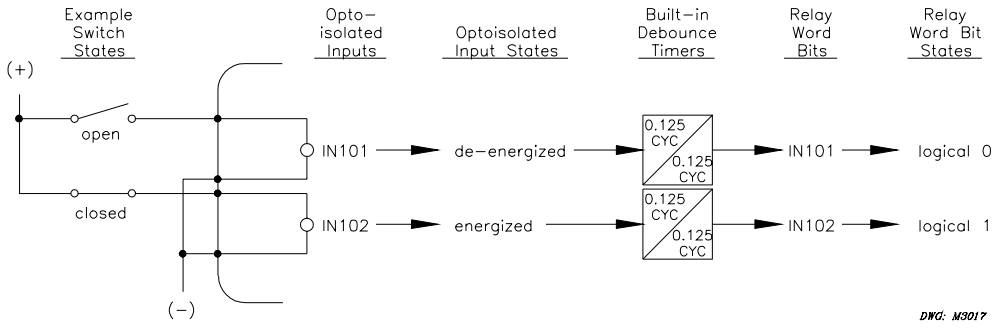

Figure 5.4: Example Operation of Optoisolated Inputs IN101 and IN102

INPUT ASSIGNMENT VARIABLES

Fifteen variables are available for assigning specific input functions. These variables are used in the default logic, but may be used for any function. See the **SET G** command in ***Section 8: Serial Port Communications and Commands***. The following input variables are available:

52AA	A-phase breaker status
52AB	B-phase breaker status
52AC	C-phase breaker status
MODST	Motor-operated disconnect status
LOD1	Loss-of-dielectric pressure (high-set)
LOD2	Loss-of-dielectric pressure (low-set)
LODCT	Loss of CT dielectric pressure
SS1	Setting group selector variable 1
SS2	Setting group selector variable 2
TRIPA	A-phase trip input
TRIPB	B-phase trip input
TRIPC	C-phase trip input
TRIP3	Three-phase trip input
CLOSE	Automatic close input
MCLOSE	Manual close input

The inputs assignment variables are SELOGIC control equations. Set them to NA if they are not used. Set them to follow a specific input, or set them to a combination of elements. Some examples follow:

MODST = NA	Always a logical 0
CLOSE = IN101	Input 101 asserts automatic closing
MCLOSE = IN102 + CCMD	Input 102 asserts manual closing or the CCMD bit asserts manual closing

52A, MODST

The 52AA, 52AB, 52AC, and MODST are used to indicate breaker and switch position. When the variable is asserted, the corresponding device is considered closed. When the variable is deasserted, the corresponding device is considered open. If a three-pole breaker is used with a single 52A input, 52AA, 52AB, and 52AC must all be set to that input.

52AA = IN104
52AB = IN104
52AC = IN104

LOD

LOD1 and LOD2 typically are connected to pressure switches used to measure the dielectric gas pressure of the circuit breakers. LODCT typically is connected to a switch monitoring the dielectric pressure of the CTs.

Multiple Setting Groups (SS1, SS2)

The setting group selector variables determine what setting group is active. If both of the variables are not assigned or both are deasserted, the setting group is selected by the **GROUP** command. The following table summarizes the use of the SS1 and SS2 variables:

Table 5.6: Setting Group Selector States

SS1	SS2	Active Setting Group
NA	NA	Last **GRO n** command issued
0	0	Last **GRO n** command issued
1	0	Setting Group 1
0	1	Setting Group 2
1	1	Setting Group 3

The setting group selector variables must be asserted or deasserted for the SET G setting TGR time in seconds before a setting group change is made.

TRIP

The trip variables are used to indicate that an external device has initiated tripping on a per-pole basis or that the three-phase variable can be used. TRIP3 is totally independent of the other trip variables.

CLOSE, MCLOSE

The two close variables are used to indicate that an external device has initiated closing. Two close variables are provided to separate automatic and manual close initiation.

LOCAL CONTROL SWITCHES (LB1—LB16)

Local control switches are used largely for the same purposes as the remote control switches, but are operated from the front-panel interface rather than from a serial port. The local control switches replace traditional panel-mounted control switches. They may be set (turned ON), cleared (turned OFF), or pulsed (operated in a MOMENTARY fashion), in the same manner as the remote control switches. Access to the local control switches is via the CNTRL pushbutton on the front panel of the relay. The functions and positions of the switches are shown on the LCD display via user-defined labels. These labels are downloaded via a serial port, using the **SET T** command. If any of these local control switch functions have been defined, the default front-panel display will show the message “Press CNTRL for Local Control,” to alert the user that local control capabilities have been programmed. A more complete description of the switches and associated settings is located in ***Section 9: Front-Panel Interface***.

REMOTE CONTROL SWITCHES (RB1—RB16)

Remote control switches are operated via the serial communications port only (see ***Section 8: Serial Port Communications and Commands***).

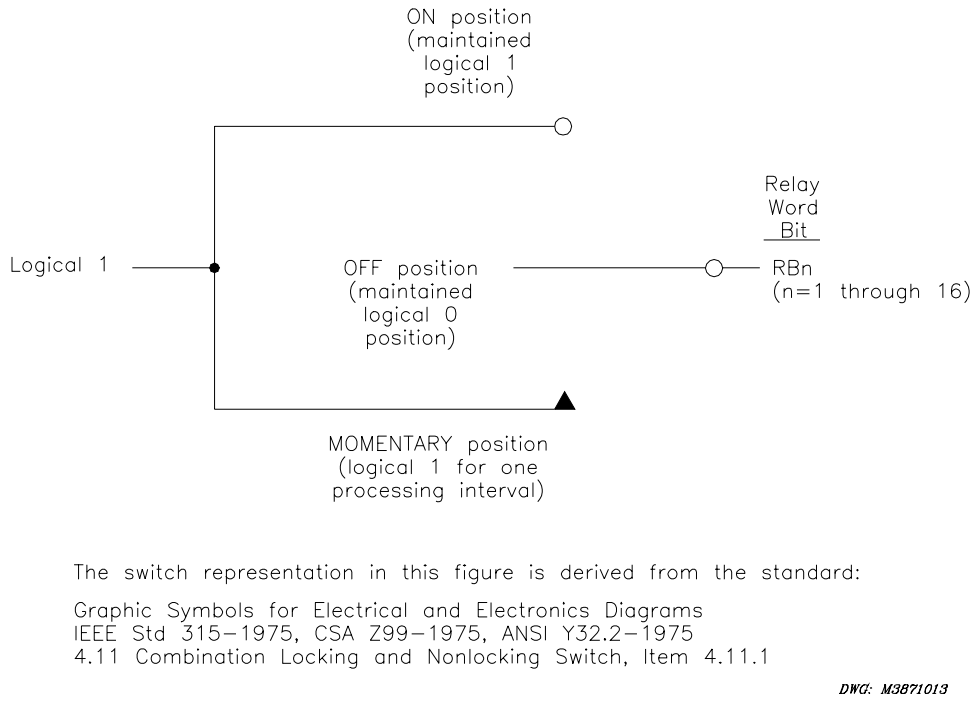

Figure 5.5: Remote Control Switches Drive Remote Bits RB1 Through RB16

The outputs of the remote control switches in Figure 5.5 are Relay Word bits RBn (n = 1 to 16), called remote bits. Use these remote bits in SELOGIC control equations.

Any given remote control switch can be put in one of the following three positions via the serial port commands shown. Begin with the **CON n** (Control Remote Bit n) command, then specify:

SRB n (Set Remote Bit n)	ON	(logical 1)
CRB n (Clear Remote Bit n)	OFF	(logical 0)
PRB n (Pulse Remote Bit n)	MOMENTARY	(logical 1 for an eighth cycle)

Remote Bit Application

With SELOGIC control equations, the remote bits can be used in applications where you want certain logic to be remotely enabled or disabled, depending on operating conditions of the system. Also, remote bits can be used in operating latches within SELOGIC control equations. Pulse (momentarily operate) the remote bits for this application. Latches are discussed later in this section.

Remote Bit States Not Retained When Power Is Lost

The states of the remote bits (Relay Word bits RB1 through RB16) are not retained if power to the relay is lost and then restored. The remote control switches always come back in the OFF position (corresponding remote bit is deasserted to logical 0) when power is restored to the relay.

Remote Bit States Retained When Settings Changed or Active Setting Group Changed

The state of each remote bit (Relay Word bits RB1 through RB16) is retained if relay settings are changed (for the active setting group or one of the other setting groups) or the active setting group is changed. If a remote control switch is in the ON position (corresponding remote bit is asserted to logical 1) before a setting change or an active setting group change, it comes back in the ON position (corresponding remote bit is still asserted to logical 1) after the change.

SELOGIC CONTROL EQUATION SET A

The SEL-352 Relay has two sets of logic reserved for additional flexibility. Set A and Set B provide timers, latches, and generic variables for customizing your application. General Purpose Logic Set A is processed every 1/8 cycle. SELOGIC control equation Set A is not used for any of the default logic.

Timers (62T1A, 62T1B, and 62T1C)

Range: 0–8191 cycles in 1/8-cycle steps

Three timers with a pickup and dropout time provide control for three independent phase elements. A-phase is shown in Figure 5.6, and B-phase and C-phase are similar.

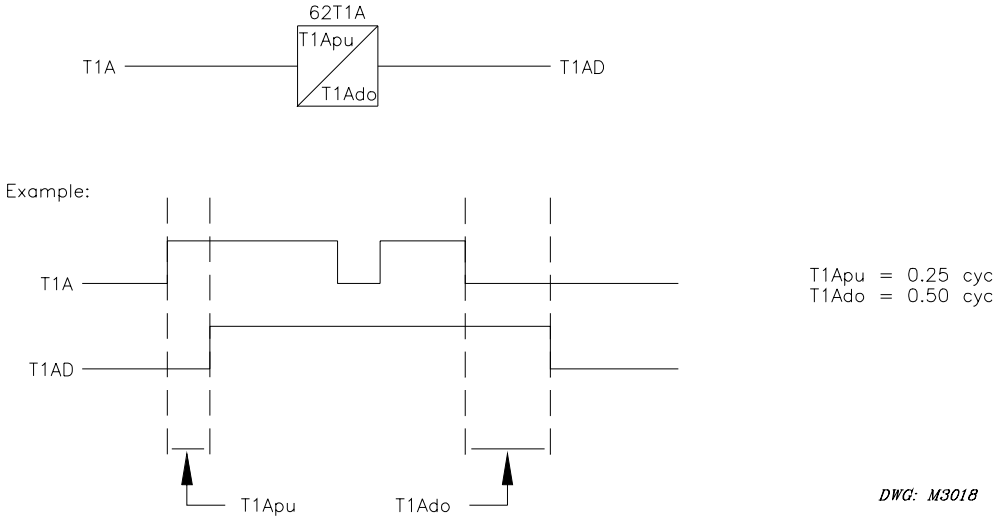

Figure 5.6: 62T1A Timer Logic

T1A must assert for T1Apu cycles before T1AD will assert, and T1A must deassert for T1Ado cycles before T1AD will deassert.

Latch Control Switches

The SELOGIC control equation latch bit feature of this relay replaces latching relays. Unlike other relays in the SEL-300 series, the SEL-352 Relay latch bits in Set A are volatile, and the results of the set and reset SELOGIC control equations are available as Relay Word bits (LxxS and LxxR, respectively). Also, the latch control switch output is labeled as LxxQ rather than LBx.

Latches are used throughout the relay logic. The S input is what sets the Q output, and the R input is what resets the Q output. If both inputs are asserted, the reset takes precedence. SELOGIC control equation Set A has three latches for independent phase control: L1AQ, L1BQ, and L1CQ. Figure 5.7 shows A-phase. B-phase and C-phase are similar.

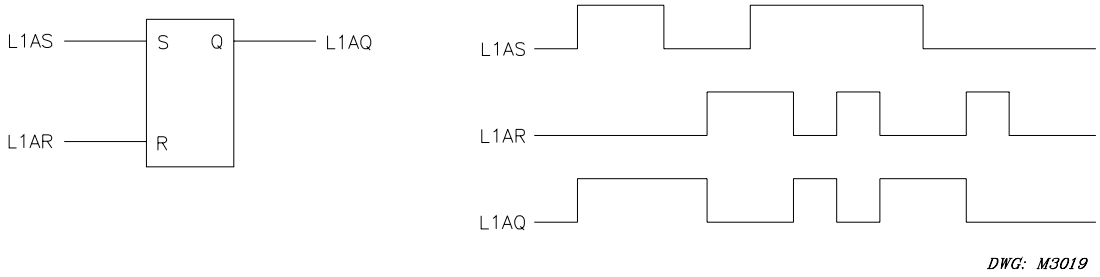

Figure 5.7: Latch Logic

L1AQ is the Q output for the L1 Latch. The L1AQ bit is set (asserted and latched) when L1AS asserts. L1AQ will only deassert when L1AR asserts. When both L1AR and L1AS are asserted, L1AQ resets (deasserts).

SELOGIC Control Equation Variables

Three variables are available for application flexibility. Set A variables SAA, SAB, and SAC may be used individually or as the same function for each individual phase. Use these variables to make larger SELOGIC control equations, to provide a monitoring point for testing, or to create a specific event triggering point.

SELOGIC CONTROL EQUATION SET B

The SEL-352 Relay has two sets of logic reserved for additional flexibility. Set A and Set B provide timers, latches, and generic variables for customizing your application. General Purpose Logic Set B is processed every quarter-cycle. SELOGIC control equation Set B is not used for any of the default logic.

Timers (62T2A, 62T2B, 62T2C and 62T3A, 62T3B, 62T3C)

Range: 0–16383 cycles in 1/4-cycle steps

Six timers with a pickup and dropout time provide control for two sets of three independent phase elements. A-phase is shown in Figure 5.6 for 62T1A of SELOGIC control equation Set A. SELOGIC control equation Set B timers are similar.

Latch Control Switches

The SELOGIC control equation latch bit feature of this relay replaces latching relays. Unlike other relays in the SEL-300 series, the SEL-352 Relay latch set and reset SELOGIC control equation results are available as Relay Word bits (LxxS and LxxR, respectively). Also, the latch control switch output is labeled as LxxQ rather than LBx.

Latches are used throughout the relay logic. The S input is what sets the Q output, and the R input is what resets the Q output. If both inputs are asserted, the reset takes precedence. SELOGIC control equation Set B has 18 **nonvolatile** latches for six sets of three independent phase controls. The status of the SELOGIC control equation Set B latches is checked approximately every second and saved to nonvolatile memory if there is any change in status. The SELOGIC control equation Set B latches are restored from the nonvolatile memory on power up. Figure 5.7 shows a latch for SELOGIC control equation Set A. SELOGIC control equation Set B latches are similar. They are denoted as L2AQ, L2BQ, L2CQ through L7AQ, L7BQ, L7CQ.

SELOGIC Control Equation Variables

Three variables are available for application flexibility. Set B variables SBA, SBB, and SBC may be used individually or as the same function for each individual phase. Use these variables to make larger SELOGIC control equations, to provide a monitoring point for testing, or to create a specific event triggering point.

OUTPUT CONTACTS

All contact output elements represent a programmable output contact. These contacts will only operate according to a corresponding SELOGIC control equation. These elements follow the state of that equation. For example, if output contact 101 is supposed to close for breaker failure lockout conditions, set OUT101 = 86BFT. Any combination of Relay Word bits may be set to operate an output contact. Refer to ***SELOGIC Control Equations*** earlier in this section.

The states of all outputs remain unchanged during the time a relay settings change is being made. However, when the new settings are put into effect, each individual output responds to the new logical state of the SELOGIC control equation that governs it.

ROTATING DEFAULT DISPLAY

The rotating default display on the relay front panel replaces indicating panel lights. Traditional indicating panel lights are turned on and off by circuit breaker auxiliary contacts, front-panel switches, SCADA contacts, etc. See ***Section 9: Front-Panel Interface*** for details.

SELOGIC control equations are used to determine which text message to display on the LCD. Unlike other relays in the SEL-300 series, the results of these control equations are available as Relay Word bits (DP1 through DP16) in the SEL-352 Relay.

LED TARGETING LOGIC

The target LEDs on the front panel illuminate based on various relay conditions. Under normal operating conditions, the EN LED should be lit. Whenever another LED is illuminated, it indicates that the relay has detected a particular condition since the last time the Target Reset button was pushed, the **TAR R** command was issued, or power was cycled. View these targets remotely by issuing the **TAR n** command to one of the serial ports, where n is a number representing the row of the Relay Word to be displayed. Row 0 and Row 1 of the Relay Word represent the 16 LEDs.

Front-panel targets are processed every 1/8 cycle and illuminate for the conditions shown in Table 5.7. All target LEDs latch except EN, 52A, and MOD. TRIP and CLOSE will reset one another. Targets are reset when power is cycled. Refer to Figure 5.8 through Figure 5.20 for logic diagrams for each target LED.

Table 5.7: Target LED Illumination Conditions

	Target LED	Conditions for Illumination	Latched
Row 0 (top row)			
	EN	Normal Operation	No
	PF	Breaker Pending Failure Detected	Yes
	86BFT	Lockout Relay Trip	Yes
	86RS	Lockout Relay Reset	Yes
	TRIP	Breaker Trip Received	Yes*
	CLOSE	Breaker Close Received	Yes*
	52A	52A Status Input Assertion	No
	MOD	MOD Status Input Assertion	No
Row 1 (bottom row)			
	A	A-Phase Breaker Failure	Yes
	B	B-Phase Breaker Failure	Yes
	C	C-Phase Breaker Failure	Yes
	FAULT	Fault Current Protection Operated	Yes
	LOAD	Load Current Protection Operated	Yes
	UBAL	Current Unbalance Protection Operated	Yes
	FLASH	Flashover Protection Operated	Yes
	THERM	Thermal Failure Protection Operated	Yes

*TRIP and CLOSE Target LEDs reset one another.

EN Target LED

The enable (EN) target LED is illuminated for all normal operating conditions. Any condition that temporarily or permanently disables the relay protection and control capabilities extinguishes the EN target LED.

Self-test failures, no power supplied to the relay, setting group changes in progress, and settings being saved all extinguish the EN target LED for as long as the condition exists. Figure 5.8 shows the EN target LED logic.

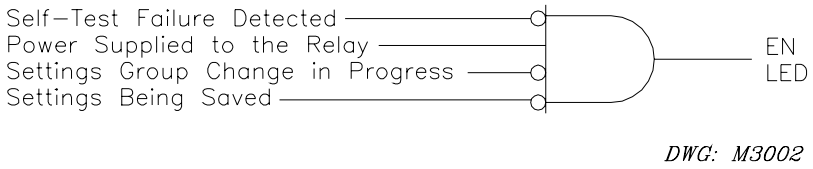

Figure 5.8: EN Target LED Logic

PF Target LED

The pending failure (PF) target LED is illuminated and latched whenever a failure is pending, based on various pending failure logic elements in the relay. The relay can detect a pending failure for the following conditions:

- Load current (LPF)
- Trip resistor thermal condition (26TP)
- Close resistor thermal condition (26CP)
- Flashover (FOPF)
- Current unbalance (UBPF)
- Loss of Dielectric (LODPF)

If any one of the logic pending failure bits asserts, the PF target LED latches until the condition goes away and either the Target Reset button is pushed or the **TAR R** command is issued to one of the serial ports. Figure 5.9 shows the PF target LED logic.

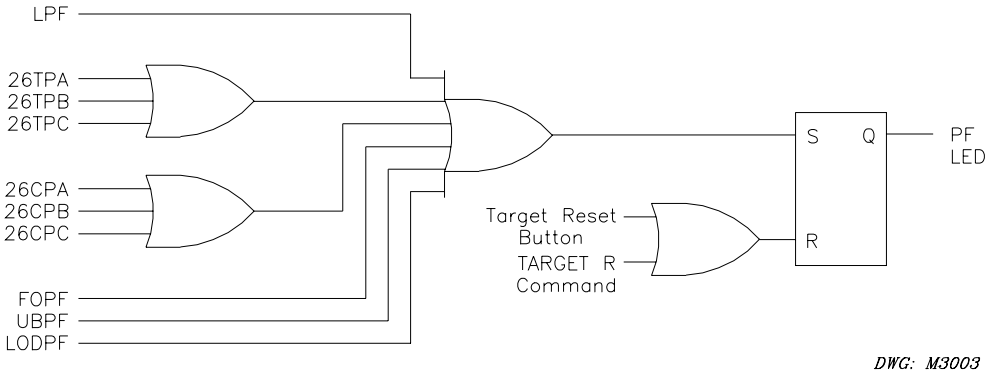

Figure 5.9: PF Target LED Logic

86BFT Target LED

The relay illuminates the 86BFT target LED whenever the breaker failure lockout relay trip bit (86BFT) in Relay Word Row 69 asserts. This bit is typically assigned to an output contact to pick up a lockout relay because of a breaker failure condition. The 86BFT Target LED latches when the 86BFT bit asserts. The 86BFT Target LED extinguishes when the condition goes away and either the Target Reset button is pushed or the **TAR R** command is issued to one of the serial ports. Figure 5.10 shows the 86BFT target LED logic.

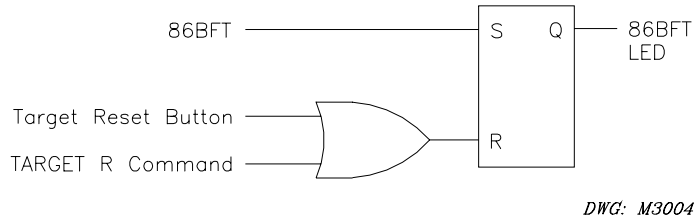

Figure 5.10: 86BFT Target LED Logic

86RS Target LED

The relay illuminates and latches the 86RS target LED whenever the breaker failure lockout relay reset element (86RS) in Relay Word Row 69 asserts. This bit is typically assigned to an output contact to reset a lockout relay after timing toward a breaker failure condition. The 86RS Target LED latches when the bit asserts. The 86RS Target LED extinguishes when the condition goes away and either the Target Reset button is pushed or the **TAR R** command is issued to one of the serial ports. Figure 5.11 shows the 86RS target LED logic.

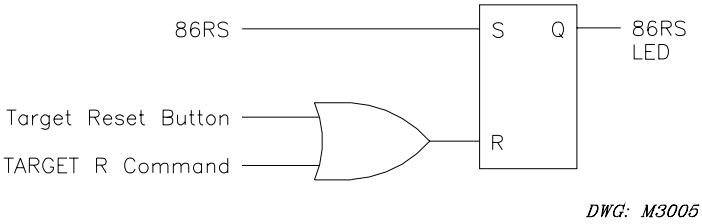

Figure 5.11: 86RS Target LED Logic

TRIP Target LED

The relay illuminates and latches the TRIP target LED whenever one of the trip elements (TRIP3, TRIPA, TRIPB, TRIPC) asserts and a close condition does not exist. The TRIP target LED latches until a close condition occurs, the Target Reset button is pushed, or the **TAR R** command is issued to one of the serial ports. Figure 5.12 shows the TRIP target LED logic.

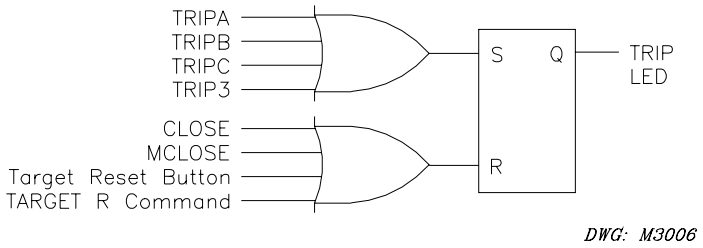

Figure 5.12: TRIP Target LED Logic

If both a trip and close condition exist at the same time, the CLOSE target LED illuminates and the TRIP target LED extinguishes because of the processing order. For simplicity, this is not represented in the logic diagram.

CLOSE Target LED

The relay illuminates and latches the CLOSE target LED whenever one of the close elements (CLOSE, MCLOSE) assert. The CLOSE target LED latches until the close conditions deassert, a trip condition asserts, the Target Reset button is pushed, or the **TAR R** command is issued to one of the serial ports. Figure 5.13 shows the CLOSE target LED logic.

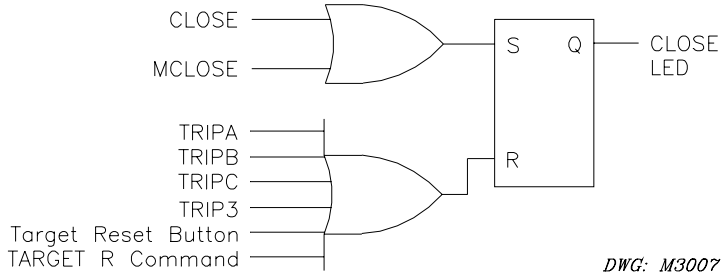

Figure 5.13: CLOSE Target LED Logic

If both a trip and close condition exist at the same time, the CLOSE target LED illuminates and the TRIP target LED extinguishes because of the processing order. For simplicity, this is not represented in the logic diagram.

52A Target LED

The relay illuminates the 52A target LED when all three breaker monitoring bits (52AA, 52AB, 52AC) assert. Figure 5.14 shows the 52A target LED logic.

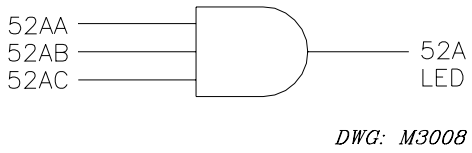

Figure 5.14: 52A Target LED Logic

A, B, and C Target LEDs

The relay illuminates and latches the A, B, and/or C target LED to indicate which phases were involved with the breaker failure. The failures during a FAULT, LOAD, FLASH, UBAL, and THERM include phase indication. When one of these conditions exists according to Figure 5.15, the phase(s) involved will target accordingly. A-phase logic is shown, but B and C are similar.

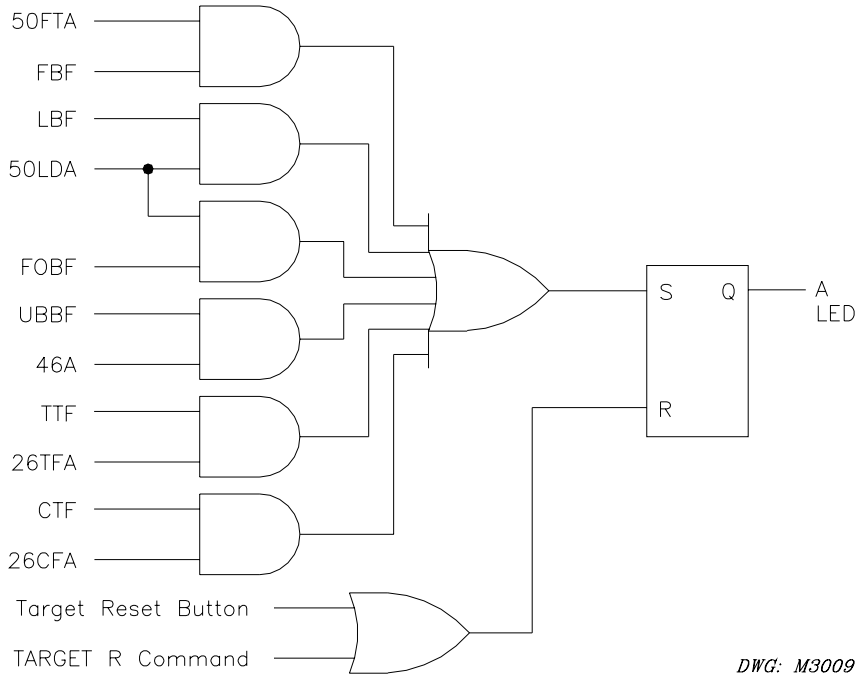

Figure 5.15: A-Phase Target LED Logic

These phase targets latch until the condition goes away and either the Target Reset button is pushed or the **TAR R** command is issued to one of the serial ports.

MOD Target LED

The relay illuminates the MOD target LED when the motor-operated disconnect status element (MODST) is asserted.

FAULT Target LED

The relay illuminates and latches the FAULT target LED when the output element for breaker failure while tripping fault current (FBF) asserts. The target LED latches until the condition goes away and either the Target Reset button is pushed or the **TAR R** command is issued to one of the serial ports. Figure 5.16 shows the FAULT target LED logic.

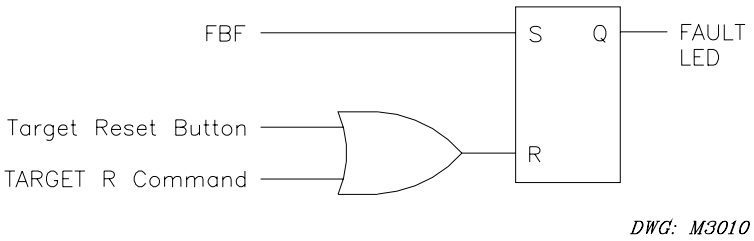

Figure 5.16: FAULT Target LED Logic

LOAD Target LED

The relay illuminates and latches the LOAD target LED when the output element for breaker failure while tripping load or line charging current (LBF) asserts. The target LED latches until the condition goes away and either the Target Reset button is pushed or the **TAR R** command is issued to one of the serial ports. Figure 5.17 shows the LOAD target LED logic.

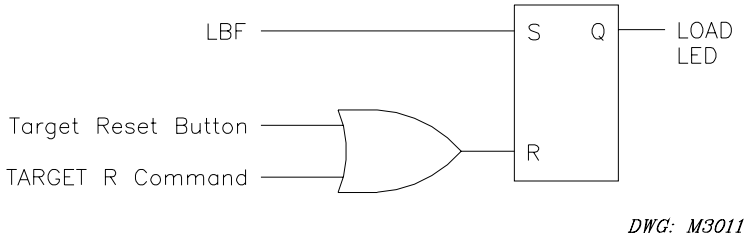

Figure 5.17: LOAD Target LED Logic

UBAL Target LED

The relay illuminates the UBAL target LED when the output element for breaker failure due to phase current unbalance while closing (UBBF) asserts. The target LED latches until the condition goes away and either the Target Reset button is pushed or the **TAR R** command is issued to one of the serial ports. Figure 5.18 shows the UBAL target LED logic.

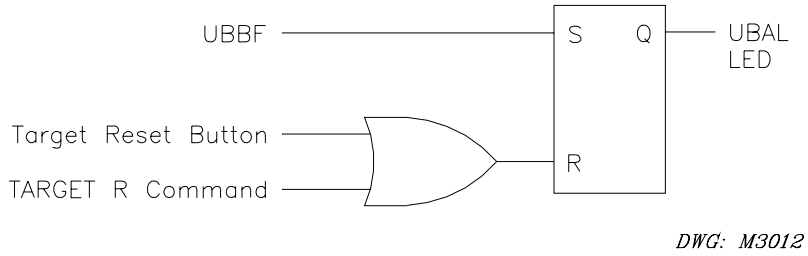

Figure 5.18: UBAL Target LED Logic

FLASH Target LED

The relay illuminates and latches the FLASH target LED when the output element for breaker failure due to a flashover (FOBF) asserts. The target LED latches until the condition goes away and either the Target Reset button is pushed or the **TAR R** command is issued to one of the serial ports. Figure 5.19 shows the FLASH target LED logic.

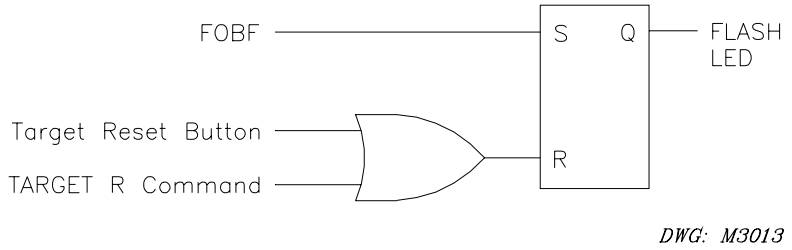

Figure 5.19: FLASH Target LED Logic

THERM Target LED

The relay illuminates and latches the THERM target LED when one of the output elements for trip or close resistor thermal failure (TTF, CTF) asserts. The target LED latches until the condition goes away and either the Target Reset button is pushed or the **TAR R** command is issued to one of the serial ports. Figure 5.20 shows the THERM target LED logic.

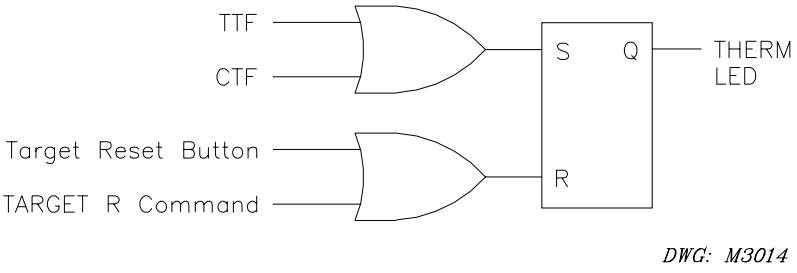

Figure 5.20: THERM Target LED Logic

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SECTION 6: METERING AND MONITORING

INTRODUCTION

The SEL-352 Relay provides metering information in several formats for the three-phase winding current input. In addition, a Breaker Monitor function records breaker trips, the cumulative current interrupted over time, and the amount of estimated contact wear. A Breaker Resistor Thermal Monitor tracks the temperature of the close and open resistor for each of the three phases. The relay also conducts a number of self-tests and provides warning and failure alarms.

METERING

The **MET** command generates metering reports similar to the following example. The report shows the TRMID setting, the date and time the report was displayed, and column labels as a header. The values displayed include phase-to-neutral and phase-to-phase voltages and currents in primary kilovolts and amperes, and real and reactive power in megawatts and megavars.

```
=>MET<ENTER>

EXAMPLE: BUS B, BREAKER 3         Date: 02/01/96    Time: 15:15:24.640

               A         B         C         AB        BC        CA
I (A)          202       198       197       349       339       344
VX(kV)       134.1     133.7     133.5     231.5     230.9     231.9
VY(kV)       134.0     133.8     133.6     231.5     230.9     231.9
dV(kV)       0.371     0.425     0.877
P (MW)       78.61
Q (MVAR)     13.85

=>
```

Metering Calculations

Currents are calculated based on the following (B and C are similar):

IA = Magnitude of (IA analog input) • (CTR)
IAB = Magnitude of [(IA analog input) – (IB analog input)] • (CTR)

Voltages are calculated based on the following (B and C are similar):

VXA = Magnitude of (VXA analog input) • (XPTR) / 1000
VXAB = Magnitude of [(VXA analog input) – (VXB analog input)] • (XPTR) / 1000
VYA = Magnitude of (VYA analog input) • (YPTR) / 1000
VYAB = Magnitude of [(VYA analog input) – (VYB analog input)] • (YPTR) / 1000
dVA = Magnitude of [(VXA analog input) • (XPTR) – (VYA analog input) • (YPTR)] / 1000

Three-phase power is calculated based on the following:

P = Real part of (IA•VXA + IB•VXB + IC•VXC) • (XPTR) • (CTR) / 1,000,000
Q = Imaginary part of (IA•VXA + IB•VXB + IC•VXC) • (XPTR) • (CTR) / 1,000,000

Note: Analog input angles must be considered for all phase-to-phase, power, and dV calculations. Refer to ***Section 1: Introduction and Specifications*** for metering accuracy.

BREAKER MONITOR

The SEL-352 Relay breaker monitor provides the following functions:

- Electrical operate time
- Mechanical operate time
- Trip and close energy
- Trip and close current
- Breaker contact wear percentage (SEL-352-2 Relay)
- Numerous alarms

Use the **BRE** (breaker monitor report) or **BRE S** (breaker monitor summary report) commands to display breaker operation information on a per-pole basis, a breaker operation summary, and a listing of breaker alarms. The operations and summary are stored in nonvolatile memory so the relay retains these if power is removed from the relay. Loss of relay power causes erasure of breaker alarms. Use the breaker operation report to analyze specific operations. Use the summary to identify a breaker that may be slowing down or is ready for maintenance. The breaker alarms report summarizes any occurrence of abnormal breaker conditions. An example breaker report follows:

```
=>BRE<ENTER>
EXAMPLE CIRCUIT BREAKER               Date: 02/17/21    Time: 04:02:08.509

FID=SEL-352-1-R100-D960112

                                BREAKER OPERATIONS


#      DATE         TIME        OPERATION  OP. TIME (ms)   ENERGY  CURRENT
                                           ELECT.  MECH.     (MJ)     (A)
1    09/26/96   16:24:37.401   TRIPA         29      16      0.03     5472
2    09/26/96   16:24:37.401   TRIPB         29      16      0.01     5454
3    09/26/96   16:24:37.401   TRIPC         29      16      0.01     5457
4    09/26/96   16:22:03.651   CCA            8      12      0.02     1248
5    09/26/96   16:22:03.651   CCB            8      12      0.01     1239
6    09/26/96   16:22:03.651   CCC           10      12      0.00     1236


                                OPERATION SUMMARY
                                  FROM 09/26/96

                        TRIPA   TRIPB   TRIPC   CLOSEA  CLOSEB  CLOSEC

Number of Operations    1       1       1       1       1       1

Ave. Elect. Time (ms)   29.0    29.0    29.0    8.0     8.0     10.0
Ave. Mech. Time  (ms)   16.0    16.0    16.0    12.0    12.0    12.0

Last Elect. Time (ms)   29      29      29      8       8       10.0
Last Mech. Time  (ms)   16      16      16      12      12      12

Total Energy  (MJ)       0.03    0.01    0.01    0.02    0.01    0.00
Total Current (A)       5472    5454    5457    1248    1249    1236
Percent Wear (%)        100     100     100

                                  BREAKER ALARMS

                                          ALARM    TOTAL COUNT

Failed CB trip resistors put in service   FTRS          0
Failed CB close resistors put in service  FCRS          0
52A contradicts voltage                   52ACV         1
Current while open                        CWO           0
Trip while open                           TWO           1
CB did not close                          BDNC          0
Current after MOD trip                    CAMT          0
MOD contradicts current                   MCC           0
Slow trip                                 ST            0
Slow close                                SC            0
Potential transformers disagree           PTD           2

=>
```

Header

The header of the breaker monitor report includes the TRMID setting, the date and time the breaker monitor report was displayed, and the relay firmware identification string. See ***Appendix A: Firmware Versions in This Manual*** for a description of the FID string.

Breaker Operations

The relay stores the latest 512 breaker operations in nonvolatile memory on a per-pole basis. The relay reports electrical and mechanical operate times, the energy dissipated, and the maximum current for the trip or close operation of each pole.

Date and Time

Recording of the date and time stamp occurs at the time of the breaker operation based on the assertion of the condition reported in the operation column.

Operation

The relay records a breaker operation at the time any of the following Relay Word bits assert:

TRIPA corresponds to an A-phase trip operation
TRIPB corresponds to a B-phase trip operation
TRIPC corresponds to a C-phase trip operation
CCA corresponds to an A-phase close operation
CCB corresponds to a B-phase close operation
CCC corresponds to a C-phase close operation

Electrical Operate Time

The relay defines electrical operating time per phase. The A-phase tripping time is measured from the assertion of TRIPA to the dropout of 50MNA ($0.02 \bullet I_{nom}$).

The electrical operating time for A-phase closing is measured from the assertion of CCA to the pickup of 50MNA or the dropout of 87THA (whichever occurs first).

If the breaker operating time exceeds both the SlowCl and SlowTr settings, the relay reports the larger of these two settings with an appended + (plus) symbol. B- and C-phases are similar.

Mechanical Operate Time

The relay defines mechanical operating time per phase. The A-phase tripping time is measured from the assertion of TRIPA to the dropout of 52AA.

The mechanical operating time for A-phase closing is measured from the assertion of CCA to the pickup of 52AA.

If the breaker operating time exceeds both the SlowCl and SlowTr settings, the relay reports the larger of the two with an appended + (plus) symbol. B- and C-phases are similar.

Energy

Energy measurement occurs during each trip and close operation on a per-pole basis. The energy is the integration of the power dissipated by the breaker during the electrical operating time. The power dissipation is determined by the amount of current times the difference voltage across the breaker.

Current

Current measurement occurs during each trip and close operation on a per-pole basis. The current is the maximum filtered current through the breaker during the electrical operating time.

Operation Summary

The relay calculates all operation summary information from the last date (listed below the heading) the breaker monitor was cleared. This calculation is not limited by the 512 operations of the operations report. Use the **BRE S** command to display the summary and breaker alarms independently of the breaker operations.

Number of Operations

The total operations since the last clearing of the breaker report is displayed on a per-pole basis for all trip and close operations. This count includes all operations listed in the operation report but is not limited to the last 512 operations. Any operations longer than the longest SlowCl or SlowTr settings (designated by a + symbol) also appear in the count.

Average Operation Times

Average electrical and mechanical operation time reporting is on a per-pole basis. This is an average of all operation times since the last clearing of the breaker monitor. Any operations longer than the longest SlowCl or SlowTr settings (designated by a + symbol) do not appear in the average calculation. This average, unlike the breaker operations report, is not limited to the last 512 events. Calculation of the average continues for all operations until clearing of the breaker monitor report.

Last Operation Times

The relay reports the last trip and close operation for each pole. These electrical and mechanical operation times provide the necessary information for fast comparisons of the averages to determine if a breaker is slowing down. Any operation longer than the longest SlowCl or SlowTr settings (designated by a + symbol) does not appear as the last operation. The slow close or slow trip alarms should indicate a slow breaker. When this occurs, view the breaker operations report with the **BRE** command.

Total Energy

Energy accumulates on a per-pole basis for the trip and close operations in megajoules (MJ). The energy of each normal electrical operation is added to the total energy. Any electrical operations longer than the longest SlowCl or SlowTr settings (designated by a + symbol) are not included in the energy accumulation.

Total Current

Total current accumulates on a per-pole basis for the trip and close operations in amps (A). The maximum current of each normal electrical operation is added to the total current. Any electrical operations that took longer than the longest SlowCl or SlowTr settings (designated by a + symbol) are not included in the current accumulation.

Percent Wear (SEL-352-2 Relay)

The breaker contact wear (percent wear) function is only available in the SEL-352-2 Relay.

Use the breaker contact wear function to estimate the amount of contact wear per pole. You can use this information and the BCW (breaker contact wear alarm) Relay Word bit in a Reliability Centered Maintenance program. The relay estimates the contact wear based on a simple model of the breaker manufacturer maintenance curves, number of breaker operations, and total interrupted current. The curve is a plot of close/open operations versus interrupted currents in kiloamperes (kA). The total interrupted current is an accumulation of the RMS current (IRMSA, IRMSB, IRMSC) measured Topen milliseconds after a trip (TRIPA, TRIPB, TRIPC Relay Word bit).

Use the three points shown in Figure 6.1 to model the breaker maintenance curve. These points divide the curve into three regions to tailor the curve for a breaker in a particular application. The first region is intended for low currents, the second for medium currents, and the third for high currents. This flexibility accommodates mechanical wear resulting from low-current breaker interruptions and electrical wear resulting from medium and high currents.

KASP1 is kA Set Point 1, while COSP1 is Close/Open Set Point 1. The relay will not accept the settings unless KASP3>KASP2>KASP1 and COSP1>COSP2>COSP3.

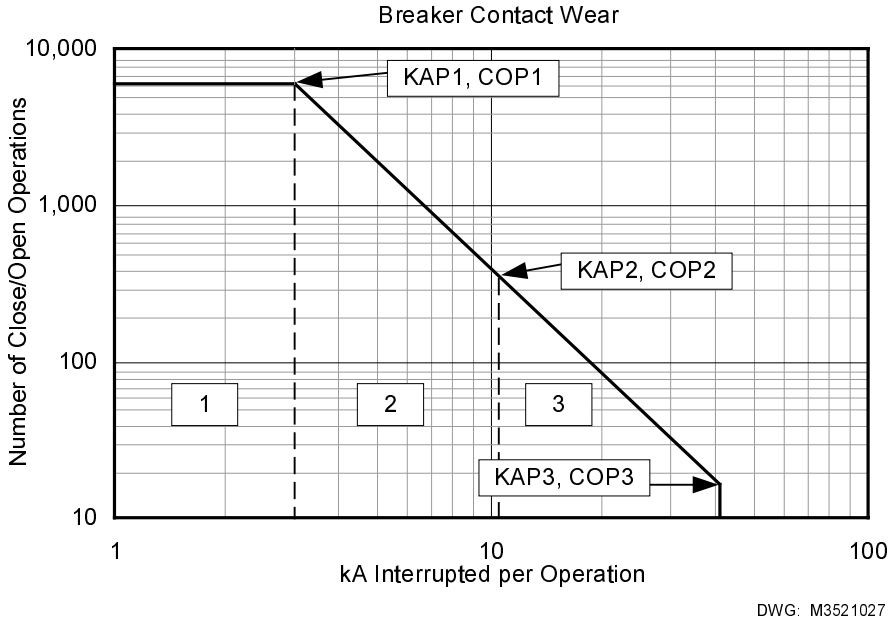

Figure 6.1: Breaker Maintenance Curve

Breaker contact wear calculation occurs on a per-phase basis (BCWPn where n=A, B, or C) by adding the percent wear for the latest operation to the previous sum. For example, the breaker can perform 6200 close/open operations if 3 kA is interrupted each time. Therefore, a single 3 kA operation adds 100 percent (1/6200) = 0.016 percent wear to the breaker. The breaker can perform 400 close/open operations if 10 kA is interrupted each time. Therefore, a single 10 kA operation adds 100 percent (1/400) = 0.25 percent wear to the breaker, an accumulated wear of 0.266 percent.

The relay uses the following equation to calculate the contact wear as described above:

$$BCWPp_{(k)} = \frac{100}{K \cdot I^{\alpha}} + BCWPp_{(k-1)}$$

The expression represents a straight-line equation in a log-log plot. You need to use three equations, because the curve has three regions and there is an equation per region. Each region has a corresponding K and • constant derived using the (KASP1, COPS1), (KASP2, COSP2), and (KASP3, COSP3) point pairs as follows:

Table 6.1: α **and K Constants for the Three Regions in Figure 6.1**

Region 1	Region 2	Region 3
$\alpha_1 = 0$	$\alpha_2 = \frac{\log(COSP1/COSP2)}{\log(KASP1/KASP2)}$	$\alpha_3 = \frac{\log(COSP2/COSP3)}{\log(KASP2/KASP3)}$
$K_1 = COSP1$	$K_2 = \frac{(COSP1)}{(KASP1^{\alpha 2})}$	$K_3 = \frac{(COSP2)}{(KASP2^{\alpha 3})}$

Relay Word bit BCW asserts when the accumulated breaker wear for a particular phase (A, B, or C) reaches the 100 percent level. Use this bit as an alarm to initiate breaker inspection or maintenance.

Breaker Alarms

The relay reports the total number of breaker operation alarms for each specified alarm condition. The BALRM setting indicates which alarms are reported. You can use the **BRE S** command to display the summary and breaker alarms independent from the breaker operations.

Selecting Alarms

Select breaker alarms with the BALRM setting. The default setting shown below includes all possible alarms. See ***Breaker Alarm Logic*** in ***Section 3: Breaker Logic***, for default setting descriptions and logic diagrams. Use the **SET R** command to set BALRM.

Use only the alarms applicable to the operations and configuration of the application. Additional alarms will only confuse the interpretation of the report. For example, if the breaker does not include trip and close resistors, the thermal alarms are not necessary. Do not list FTRS or FTCS in the BALRM setting.

```
=>>SET R BALRM<ENTER>

Breaker Monitor
Breaker Alarm Types (24 Max)
BALRM  =52ACV CWO TWO BDNC CAMT MCC ST SC PTD
 ?
```

Total Count

The count increments each time a breaker alarm condition is satisfied (rising-edge detection). If an alarm condition persists, the counter cannot increment again. The total count resets any time the **BRE C**, **SET**, **SET R**, or **SET G** command executes or the relay loses power.

Clearing the Breaker Monitor Report

Use the **BRE C** (breaker clear) command to reset the breaker operations, operations summary, and breaker alarms after breaker maintenance.

Preloading the Breaker Monitor Report (SEL 352-2 Relay)

Use the **BRE W** command to preload the number of operations, total current, total energy, and percent wear fields in the operation summary on a per-pole basis. Use this command when installing the relay in an existing installation or when a new breaker is installed. **BRE W** is only available in the SEL-352-2 Relay.

BREAKER RESISTOR THERMAL MONITOR

The SEL-352 Relay tracks the temperature of the close and open resistor for each of the three phases. The **HEAT** (**HEA**) command displays a report of the calculated heat content of each resistor (with respect to ambient) normalized to the resistor failure threshold, 26CF or 26TF.

For example, if the B-phase open resistor (ORB) contains 1.0 J of internal heat, and the trip failure threshold (26TF) setting is 2.0 J, the **HEA** command displays the ORB resistor heat as 0.50.

The thermal report headings use a simple format. **ORA** heads the A-phase opening resistor column, **CRA** the A-phase closing resistor column, and so on, for B-phase and C-phase.

```
=>HEA<ENTER>

RESISTOR HEAT IN PER UNIT TRIP VALUE

Example 500 kV Breaker                          Date: 6/1/96    Time: 10:16:04

ORA   CRA   ORB   CRB   ORC   CRC

0.00  0.00  0.31  0.11  0.00  0.00

=>
```

Resetting the Thermal Monitor

The **HEA C** command clears the thermal models. Use the **HEA C** command to clear and quickly reset the resistor heating to zero when testing the thermal elements.

STATUS MONITOR

The relay continuously runs a variety of self-tests. Some tests have warning and failure states; others only have failure states. Identification of warnings and failures is as follows:

All warnings, represented by a W in the status report, generate an automatic serial port message and pulse the ALARM output contact for five seconds.

All failures, represented by an F in the status report, generate an automatic serial port message, display the failure on the front-panel display, and latch the ALARM output contact.

Channel Offset

The relay measures the dc offset (OS) voltage of each analog input channel and compares the value against a fixed limit of 30 mV. If an offset measurement is outside the fixed limit, the relay declares a warning.

Master Offset

The master offset (MOF) test checks the dc offset in the multiplexer/analog to digital converter circuit. The relay selects a grounded input to sample for dc offset. If the offset measurement exceeds 20 mV, the relay declares a warning. If the offset measurement exceeds 30 mV, the relay declares a failure.

Power Supply

The relay measures the internal power supply (PS) voltages and regulated +5 and –5 voltages and compares the values against fixed limits. If a voltage measurement is outside the limits, the relay declares a warning or failure. See ***Section 3: Breaker Logic*** for the limits.

Temperature

The relay measures internal temperatures (TEMP) within itself. If the relay measures a temperature less than –40°C or greater than 85°C, the relay declares a warning. If the relay measures a temperature less than –50°C or greater than 100°C, the relay declares a failure. The temperature warning does not pulse the ALARM output contact.

RAM

The relay checks the random-access memory (RAM). If the relay can neither write to nor read from a byte, the relay declares a RAM failure. There is no warning state for this test.

Flash ROM

The relay computes a checksum to check the flash read-only memory (ROM). If the computed value does not agree with a stored value, the relay declares a ROM failure. There is no warning state for this test.

Analog-to-Digital Converter

The relay checks the A/D conversion time to verify A/D converter function. The test fails if conversion time is excessive or a conversion starts and never finishes. There is no warning state for this test.

Critical RAM

A check of RAM, where the relay stores settings, occurs with the relay computing a checksum. If the computed value does not agree with a stored value, the relay declares a critical RAM (CR_RAM) failure. There is no warning for the test.

EEPROM

The relay computes a checksum to check EEPROM. If the computed value does not agree with a stored value, the relay declares an EEPROM failure. There is no warning for the test.

I/O Boards

The relay checks the values in the I/O board ID register against a stored value. If any values differ, the relay declares an I/O_BRD failure. There is no warning state for this test. Use the **INITIO <ENTER>** command to reset the stored value for the new I/O configuration.

The following is an example of the status report:

```
EXAMPLE CIRCUIT BREAKER              Date: 11/09/96    Time: 14:09:49.628

FID=SEL-352-1-R100-V-D961030
SELF TESTS

W=Warn    F=Fail

        IA       IB       IC       VAX      VBX      VCX
OS       0       -0        0        0        0        0

        VAY      VBY      VCY      MOF
OS       0        0       -0        1

        +5V_PS   +5V_REG  -5V_REG  +12V_PS  -12V_PS  +15V_PS  -15V_PS
PS       4.92     5.01    -5.00     12.09   -12.21    14.92   -14.92

        TEMP     RAM      ROM      A/D      CR_RAM   EEPROM   IO_BRD
         32.7    OK       OK       OK       OK       OK       OK

Relay Enabled

=>>
```

Self-Testing Alarms

Table 6.2 summarizes all of the self-test warning and failure limits. Each self-test is described in ***Section 11: Testing and Troubleshooting***.

Table 6.2: Self-Test Summary

Self-Test	Warning Limits	Failure Limits
Channel Offset	30 mVdc	NA
Master Offset	20 mVdc	30 mVdc
+5 V Power Supply	4.80/5.20 Vdc	4.65/5.40 Vdc
+5 V Regulated	4.75/5.20 Vdc	4.50/5.40 Vdc
–5 V Regulated	–4.75/–5.25 Vdc	–4.50/–5.40 Vdc
+12 V Power Supply	11.50/12.50 Vdc	11.20/14.00 Vdc
–12 V Power Supply	–11.50/–12.50 Vdc	–11.20/–14.00 Vdc
+15 V Power Supply	14.40/15.60 Vdc	14.00/16.00 Vdc
–15 V Power Supply	–14.40/–15.60 Vdc	–14.00/–16.00 Vdc
Temperature	–40/85°C	–50/100°C
RAM	NA	Cannot READ/WRITE
Flash ROM	NA	Bad Checksum
A/D	NA	Slow Conversion
Critical RAM	NA	Bad Checksum
EEPROM	NA	Bad Checksum
IO_BRD	NA	Incorrect I/O Board Value

The relay continuously runs a variety of self-tests. Some tests have warning and failure states; others only have failure states. Warnings and failures are identified by the following:

Warnings

- Represented by a “W” in the status report
- Generate an automatic serial-port message
- Pulse the ALARM output contact for five seconds

Failures

- Represented by an “F” in the status report
- Generate an automatic serial-port message
- Displays a front-panel message
- Closes and latches the ALARM output contact
- Disables relay, freezes in current state

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TABLES

SECTION 7: SETTING THE RELAY

INTRODUCTION

Change or view settings with the **SET** and **SHOWSET** serial port commands and the front-panel SET pushbutton. Table 7.1 lists the serial port **SET** commands.

Table 7.1: Serial Port SET Commands

Command	Settings Type	Description
SET n	Relay	Overcurrent elements for settings group n (n = 1, 2, 3, 4, 5, 6).
SET G	Global	Battery and breaker monitors, etc.
SET R	SER	Sequential Events Recorder trigger conditions and Load Profile settings.
SET P n	Port	Serial port settings for Serial Port n (n = 1, 2, 3, or F).

View settings with the respective serial port **SHOWSET** commands (**SHO**, **SHO G**, **SHO R**, **SHO P**). See discussion of **SHO** commands in ***Section 8: Serial Port Communications and Commands***. Settings Sheets are at the end of this section.

SETTINGS CHANGES VIA THE FRONT PANEL

The relay front-panel SET pushbutton provides access to the Relay, Global, and Port settings only. Thus, the corresponding Relay, Global, and Port settings sheets that follow in this section can also be used when making these settings via the front panel. Refer to ***Section 9: Front-Panel Interface*** for information on front-panel settings.

SETTINGS CHANGES VIA THE SERIAL PORT

Note: In this manual commands you type appear in bold/upper case: **SHOWSET**. You need to type only the first three letters of a command, for example, **SHO**. Computer keys you press appear in bold/upper case/brackets: **<ENTER>**.

See ***Section 8: Serial Port Communications and Commands*** for information on serial port communications and relay access levels. The **SET** commands in Table 7.1 operate at Access Level 2 (screen prompt: =>>). To change a specific setting, enter the command:

SET *n m s TERSE*

where

n = L, G, R, T, or P (parameter n is not entered for the Relay settings).

m = group (1….6) or port (1….3). The relay selects the active group or port if m is not specified.

s = the name of the specific setting you wish to jump to and begin setting. If s is not entered, the relay starts at the first setting.

TERSE = instructs the relay to skip the **SHOWSET** display after the last setting. Use this parameter to speed up the **SET** command. If you wish to review the settings before saving, do not use the **TERSE** option.

When you issue the **SET** command, the relay presents a list of settings, one at a time. Enter a new setting or press **<ENTER>** to accept the existing setting. Editing keystrokes are shown in Table 7.2.

Table 7.2: SET Command Editing Keystrokes

Press Key(s)	Results
<ENTER>	Retains setting and moves to the next setting.
^ <ENTER>	Returns to previous setting.
< <ENTER>	Returns to previous setting.
> <ENTER>	Moves to next setting.
END<ENTER>	Exits editing session then prompts you to save the settings.
<CTRL> X	Aborts editing session without saving changes.

The relay checks each entry to ensure that it is within the setting range. If it is not, an "Out of Range" message is generated, and the relay prompts for the setting again.

When all the settings are entered, the relay displays the new settings and prompts for approval to enable them. Answer **Y<ENTER>** to enable the new settings. If changes are made to Global, SER, or Port settings (see Table 7.1), the relay is disabled while it saves the new settings. If changes are made to the Relay or Logic settings for the active setting group (see Table 7.1), the relay is disabled while it saves the new settings. The ALARM contact closes momentarily (for a "b" contact, opens for an "a") and the EN LED extinguishes while the relay is disabled. The relay is disabled for about one second. If Logic settings are changed for the active group, the relay can be disabled for as long as 15 seconds.

If changes are made to the Relay or Logic settings for a setting group other than the active setting group (see Table 7.1), the relay is not disabled while it saves the new settings. The ALARM contact closes momentarily (for a "b" contact, opens for an "a") but the EN LED remains on while the new settings are saved.

ADDITIONAL RELAY SETTINGS

Group Settings (SET Command)

The **SET** command accesses settings that are specific for each of the three setting groups (1, 2, or 3). All **SET** command settings are shown in this section in the order they appear in the setting procedure with their ranges.

Relay Identification (RELID)

The relay identification (RELID) setting is a 17-character label for record keeping. Use any keyboard character in the label. RELID is displayed each time the settings are displayed. It is not displayed for any other report. This setting can be used for tracking the relay serial number or relay type. For example:

```
RELID   = SEL3521, 96268085
```

Terminal Identification (TRMID)

The terminal identification (TRMID) setting is a 39-character label for record keeping and reporting. Use any keyboard character in the label. TRMID is displayed in many reports. This setting can be used for tracking the identification of the terminal that the SEL-352 Relay is monitoring. For example:

```
TRMID   =BKR 2302, McCall - Parsons 230 kV Line
```

Nominal Breaker Trip Time (Topen)

The nominal time for the breaker to open (Topen) is for record keeping only. Enter the manufacturer's specification, timing test results, your best guess for breaker tripping times, or results from previously recorded actual operations. The trip time is considered as the time between the trip coil circuit energization and the breaker opening. An open breaker typically is indicated by an auxiliary contact or the current dropout.

Nominal Breaker Close Time (Tclose)

The nominal time for the breaker to close (Tclose) is for record keeping and close anticipation for synchronizing. Enter the manufacturer's specification, timing test results, your best guess for breaker closing times, or results from previously recorded actual operations. The close time is considered as the time between the close coil circuit energization and the breaker closing. A closed breaker is typically indicated by an auxiliary contact or the current pickup. The SEL-352 Relay can also indicate a closed breaker based on the lack of difference voltage across the breaker.

Slow Trip Alarm (SlowTr)

SlowTr is the slowest time the breaker will take to open before declaring a failure mode. The ST breaker alarm logic uses the SlowTr setting. After the TRIPA Relay Word bit asserts, the SlowTr timer starts timing. If the current does not drop out based on the fixed threshold 50MNA

element before the timer expires, the ST Relay Word bit asserts declaring a slow trip condition. B- and C-phase logic are similar.

The SlowTr setting should be set slightly longer than the Topen setting. Sometimes breaker manufacturers provide a range for the operating time of the breaker. Set the SlowTr setting at the longest value provided by the manufacturer or slightly longer. If these times are unknown, use 125 percent–150 percent of the worst case of actual timing tests.

Slow Close Alarm (SlowCl)

SlowCl is the slowest time the breaker will take to close before declaring a failure mode. The SlowCl setting is used by the SC breaker alarm logic. After the CCA Relay Word bit asserts, the SlowCl timer starts timing. If the breaker has not closed based on 52AA before the timer expires, the SC Relay Word bit asserts declaring a slow close condition. B- and C-phase logic are similar.

The SlowCl setting should be set slightly longer than the Tclose setting. Sometimes breaker manufacturers provide a range for the operating time of the breaker. Set the SlowCl setting at the longest value provided by the manufacturer or slightly longer. If these times are unknown, use 125 percent–150 percent of the worst case of actual timing tests.

Current Transformer Ratio (CTR)

The current transformer ratio (CTR) setting is based on the actual CT ratio of the current inputs. The setting is entered as a ratio to 1. For example, if the current transformers that are connected to the SEL-352 Relay are connected on a tap of 600:5, set CTR to 120. Note that if the CTs are connected in a delta configuration, assuming the same tap, set the CTR to $120 \cdot \sqrt{3}$, which equals 204.

The CTR setting is used for all reports that display current or power in primary values, such as the event report. All actual relay calculations are done using secondary values, so this setting does not affect relay performance, only reporting.

X-Side Potential Transformer Ratio (XPTR)

The potential transformer ratio (XPTR) setting is based on the actual PT ratio of the X-side voltage inputs. The setting is entered as a ratio to 1. For example, if the potential transformers that are connected to the X side of the SEL-352 Relay are connected on a tap of 1200:1, set the XPTR to 1200.

The XPTR setting is used for all reports that display voltage or power in primary values, such as the event report and metering. All actual relay calculations are done using secondary values, so this setting does not affect relay performance, only reporting.

Y-Side Potential Transformer Ratio (YPTR)

The potential transformer ratio (YPTR) setting is based on the actual PT ratio of the Y-side voltage inputs. The setting is entered as a ratio to 1. For example, if the potential transformers that are connected to the Y side of the SEL-352 Relay are connected on a tap of 4300:1, set the YPTR to 4300.

The YPTR setting is used for all reports that display voltage or power in primary values, such as the event report. All actual relay calculations are done using secondary values, so this setting does not affect relay performance, only reporting.

Mask For Event Reporting (MER)

The mask for event reporting (MER) indicates what conditions trigger an event report. The SEL-352 Relay automatically triggers event reports for certain conditions. Customize triggering by using the MER setting. Refer to ***Event Report Triggering*** in ***Section 10: Event Reports and SER***.

MER can be a single Relay Word bit or a complex SELOGIC® control equation. Set MER to trigger event reports for things other than 86BFT triggering. If the SEL-352 Relay is used for reclosing, reclosing supervision, or point-on-wave closing, set MER = CLOSE+MCLOSE.

When selecting Relay Word bits to include in the MER equation, consider the LER setting, which determines the length of each event report. If your operation does not all occur within the LER setting time, important information may be lost. Use a time-delayed pickup timer to trigger a second report if necessary. For example, if you suspect your close operation to take approximately 13 cycles, you may want to trigger an event for the CLOSE input initiation, the close output (CCA), and a timed-delayed CLOSE initiation to be sure the relay actually sees the breaker closing.

```
LER  =  15
T1A  =  CLOSE
T1pu =  14
MER  =  CLOSE+CCA+T1AD
```

CLOSE triggers the first 15 cycles, and CCA or T1AD triggers the second 15 cycles.

Global Settings (SET G Command)

Date Format (DATE_F)

Most reports display the date they are displayed or give a date for particular operations. The DATE_F setting determines how this date is displayed. If DATE_F = MDY, the date is displayed 3/22/97 (month, day, year). If DATE_F = YMD, the date is displayed 97/3/22. Set the DATE_F setting to what your company typically uses. Most relays use the MDY format, which is the SEL-352 Relay default.

SETTINGS DESCRIPTIONS

If particular schemes are selected, the specific settings are shown for that scheme. If CUSTOM is used, all settings are available along with the SELOGIC control equations. The default equations for each scheme normally are hidden. When you change to a CUSTOM configuration, the SELOGIC control equations are shown for the scheme that was enabled last.

Table 7.4, Table 7.5, Table 7.6, and Table 7.7 list only the settings that appear if the scheme logic is used (not CUSTOM). The table gives a brief description of the use of the setting, the

setting range, and the incremental steps for the setting, if applicable. Also note that the settings are grouped by function. The title of each group references the application section that details how to set those settings. Refer to these sections for detailed application information.

Table 7.3: SET R (Report) Command Settings

Setting Name	Description	Setting Range
Input, Output, and Element Aliases (See ***Section 10: Event Reports and SER***)		
ALIAS1–ALIAS20	Redefine the name of Relay Word bits (elements) by assigning an alias.	Syntax is ELEMENT <SPACE> ALIAS
BALRM	List of breaker alarm types separated by spaces. Use none or all of the breaker alarms available.	FTRS FCRS 52ACV CWO TWO BDNC CAMT MCC ST SC PTD
LABEL	Text label for the SER report	59 characters
SER1, SER2, SER3	Define SER trigger conditions (SER1, 2, and 3 are provided to separate the potentially long list of elements).	Any Relay Word bit or alias

Table 7.4: SET Command Settings

Setting Name	Description	Setting Range
Labels (See ***Section 10: Event Reports and SER***)		
RELID	Relay Identifier text label	17 characters
TRMID	Terminal Identifier text label	39 characters
Breaker Monitor and Misc. Settings (See ***Section 10: Event Reports and SER***)		
Topen	Nominal Breaker Trip Time based on manufacturer data or timing tests	0–999 ms 1-ms steps
Tclose	Nominal Breaker Close Time based on manufacturer data or timing tests	0–320 ms 1-ms steps
SlowTr	Slow Breaker Trip Time based on manufacturer data or timing tests	0–999 ms 0.1-ms steps
SlowCl	Slow Breaker Close Time based on manufacturer data or timing tests	0–999 ms 0.1-ms steps
CTR	Current Transformer Ratio based on tap connection ratio	1–10000 steps of 1
XPTR	X-Side Potential Transformer Ratio based on tap connection ratio	1–10000 steps of 1
YPTR	Y-Side Potential Transformer Ratio based on tap connection ratio	1–10000 steps of 1

Setting Name	Description	Setting Range
Fault Current Logic Settings (See ***Section 3: Breaker Logic***)		
50FT	Fault Current Detector	0.5–45.0 A sec (5 A I_{nom}) 0.1–9.0 A sec (1 A I_{nom}) 0.01-A steps
50RMS	RMS Current Detector (SEL-352-2 Relay only)	0.5–45.0 A sec (5 A I_{nom}) 0.10-A steps 0.1–9.0 A sec (1 A I_{nom}) 0.02-A steps
FTLOG	Fault Current Scheme Selection	OFF, 1–5, CUSTOM
TTpu	62TT Trip Timer Pickup Time used in Scheme 4	0–8191 cyc 0.125 cyc steps
TTdo	62TT Trip Timer Dropout Time used in Schemes 1 and 4	0–8191 cyc 0.125 cyc steps
FCpu	62FC Fault Current Pickup Time used in Schemes 1, 2, 3, and 5	0–8191 cyc 0.125 cyc steps
Load Current Logic Settings (See ***Section 3: Breaker Logic***)		
50LD	Load Current Detector	0.1–45.0 A sec (5 A I_{nom}) 0.02–9.00 A sec (1 A I_{nom}) 0.01-A steps
50N	Ground Current Detector (not used in default logic)	0.1–45.0 A sec (5 A I_{nom}) 0.02–9.00 A sec (1 A I_{nom}) 0.01-A steps
LDLOG	Load Current Scheme Selection	OFF, 1, 2, CUSTOM
LPpu	62LP Pending Failure Pickup Time used in Schemes 1 and 2	0–16383 cyc 0.25-cyc steps
LDpu	62LD Breaker Failure Pickup Time used in Schemes 1 and 2	0–16383 cyc 0.25-cyc steps
APpu	62AP 52A Pending Failure Time used in Scheme 2 only	0–16383 cyc 0.25-cyc steps
AFpu	62AF 52A Breaker Failure Time used in Scheme 2 only	0–16383 cyc 0.25-cyc steps
Thermal Protection Logic Settings (See ***Section 3: Breaker Logic***)		
37OP	Phase Overpower Element for enabling the thermal model	0.1–3400.0 W sec (5 A I_{nom}) 0.02–680.0 W sec (1 A I_{nom}) 0.01-W steps

Setting Name	Description	Setting Range
47Q	Negative-Sequence Overvoltage (V2) for any user-defined logic. Not presently used in Thermal Protection Logic.	2.0–140.0 V sec 0.1-V steps
87TH	Thermal Model Voltage Threshold for enabling the thermal model	1.0–150.0 V sec 0.1-V steps
VNpu	62VN Voltage Nulling Delay Time for qualifying the system is not in a transient state	0–240 min 0.01-min steps
Kmag	Maximum Voltage Magnitude Error to Null sets an alarm bit if the error exceeds this setting	0–30% 0.1% steps
Kang	Maximum Phase Error to Null sets an alarm bit if the error exceeds this setting	0–15 deg 0.1-deg steps
THLOG	Resistor Protection Logic enable	OFF, ON, CUSTOM
OPpu	62OP Thermal Overpower Pickup time qualifies the enable conditions for the thermal models	0–16383 cyc 0.25-cyc steps
26CP	Close Resistor Alarm Energy is not used in the default logic	0.01–1000.0 J sec (5 A I_{nom}) 0.002–200.0 J sec (1 A I_{nom}) 0.001-J steps
26CF	Close Resistor Failure Energy level determines the failure threshold for the thermal model output	0.01–1000.0 J sec (5 A I_{nom}) 0.002–200.0 J sec (1 A I_{nom}) 0.001-J steps
26TP	Trip Resistor Alarm Energy is not used in the default logic	0.01–1000.0 J sec (5 A I_{nom}) 0.002–200.0 J sec (1 A I_{nom}) 0.001-J steps
26TF	Trip Resistor Failure Energy level determines the failure threshold for the thermal model output	0.01–1000.0 J sec (5 A I_{nom}) 0.002–200.0 J sec (1 A I_{nom}) 0.001-J steps
CRTC	Close Resistor Cooling Time Constant	1–1140 min 1-min steps
TRTC	Trip Resistor Cooling Time Constant	1–1140 min 1-min steps
Flashover Protection Logic Settings (See ***Section 3: Breaker Logic***)		
87H	Flashover Voltage Difference determines the preflashover difference level	1.0–150.0 V sec 0.1-V steps
87FO	Post Flashover Voltage Difference to provide flashover detection security	1.0–150.0 V sec 0.1-V steps
59H	Flashover Phase Voltage is not used by the flash-over logic (See 59L under Controlled Closing)	1.0–130.0 V sec 0.1-V steps
FOLOG	Flashover Protection Logic scheme selection	OFF, 1, 2, CUSTOM

Setting Name	Description	Setting Range
FPpu	62FP Pending Failure Pickup Time determines if flashover conditions indicate a pending failure	0–16383 cyc 0.25-cyc steps
FFpu	62FF Breaker Failure Pickup Time determines if flashover conditions indicate a failure	0–16383 cyc 0.25-cyc steps
Unbalanced Current Protection Logic Settings (See ***Section 3: Breaker Logic***)		
46UB	Phase Current Unbalance Ratio determines sensitivity of unbalance logic (8 is most sensitive)	8, 16, 32, 64
UBLOG	Phase Current Unbalance Logic enable	OFF, ON, CUSTOM
UCpu	62UC Close Input Timer Pickup Time allows the breaker time to close before calculating unbalance	0–16383 cyc 0.25-cyc steps
UPpu	62UP Pending Failure Pickup Time determines if unbalance conditions indicate a pending failure	0–16383 cyc 0.25-cyc steps
UFpu	62UF Breaker Failure Pickup Time determines if unbalance conditions indicate a failure	0–16383 cyc 0.25-cyc steps
Dielectric Monitor Logic Settings (See ***Section 3: Breaker Logic***)		
DELOG	Loss-of-Dielectric Logic enable	OFF, ON, CUSTOM
L2pu	62L2 Leak Timer Pickup Time defines a rapid loss of pressure versus a slow leak	0–16383 cyc 0.25-cyc steps
Controlled Close Logic Settings (See ***Section 5: Control Logic***)		
59L	Live Line/Bus Voltage for both the X and Y sides	10.0–120.0 V sec 0.1-V steps
27D	Dead Line/Bus Undervoltage for both the X and Y sides	1.0–120.0 V sec 0.1-V steps
CLSLOG	Controlled Close Logic scheme selection	OFF, 1, 2, CUSTOM
CLSdo	62CLS Timer Dropout Time holds the close output closed	0–16383 cyc 0.25-cyc steps
RCApu	62RCA Timer Pickup Time defines the A-phase staggered close time (Scheme 1)	0–16383 cyc 0.25-cyc steps
RCBpu	62RCB Timer Pickup Time defines the B-phase staggered close time (Scheme 1)	0–16383 cyc 0.25-cyc steps
RCCpu	62RCC Timer Pickup Time defines the C-phase staggered close time (Scheme 1)	0–16383 cyc 0.25-cyc steps

Setting Name	Description	Setting Range
25SC	Maximum Slip Frequency for synchronism supervision and control during Automatic Closing	0.005–0.5 Hz 0.001-Hz steps
25AC	Maximum Angle for synchronism supervision and control during Automatic Closing	32 • 25SC-90 deg, min. = 1 0.1-deg steps
25SM	Maximum Slip Frequency for synchronism supervision and control during Manual Closing	0.005–0.5 Hz 0.001-Hz steps
25AM	Maximum Angle for synchronism supervision and control during Manual Closing	32 • 25SM-90 deg, min. = 1 0.1-deg steps
SYNCP	Synchronism phase	A, B, or C
SYNCdo	62SYNC Timer Dropout Time allows time to synchronize slipping systems	0–99999 cyc 0.25-cyc steps
PCApu	62PCA Timer Pickup Time for A-phase peak closing	0.00–40.00 ms 0.01-ms steps
PCBpu	62PCB Timer Pickup Time for B-phase peak closing	0.00–40.00 ms 0.01-ms steps
PCCpu	62PCC Timer Pickup Time for C-phase peak closing	0.00–40.00 ms 0.01-ms steps
ZCApu	62ZCA Timer Pickup Time for A-phase zero-crossing closing	0.00–40.00 ms 0.01-ms steps
ZCBpu	62ZCB Timer Pickup Time for B-phase zero-crossing closing	0.00–40.00 ms 0.01-ms steps
ZCCpu	62ZCC Timer Pickup Time for C-phase zero-crossing closing	0.00–40.00 ms 0.01-ms steps
CLSA	Direct Hardware Close Output Contact for A-phase	Any programmable output
CLSB	Direct Hardware Close Output Contact for B-phase	Any programmable output
CLSC	Direct Hardware Close Output Contact for C-phase	Any programmable output
Retrip Logic Settings (See ***Section 5: Control Logic***)		
RTPLOG	Circuit Breaker Retrip Logic scheme selection	OFF, 1, 2, CUSTOM
RTpu	62RT Timer Pickup Time for delaying a retrip	0–16383 cyc 0.25-cyc steps

Setting Name	Description	Setting Range
86BF Trip and Reset Logic Settings (See ***Section 5: Control Logic***)		
M86T Trip Equation	Trip equation for elements that trip the lockout relay. Typical settings are protection logic failure bits.	SELOGIC control equation
50MD	MOD Operating Current	0.1–45.0 A sec (5 A I_{nom}) 0.02–9.00 A sec (1 A I_{nom}) 0.01-A steps
TRLOG	86BF Trip and Reset Logic	OFF, 1, 2, CUSTOM
M2pu	62M2 Timer Pickup Time defines amount of time for breaker failure clearing	0–8191 cyc 0.125-cyc steps
M3pu	62M3 Timer Pickup Time defines amount of time for MOD tripping	0–8191 cyc 0.125-cyc steps
Event Report Trigger (See ***Section 10: Event Report and SER***)		
MER	Event Report triggering equation	SELOGIC control equation
Output Contacts (SELOGIC Control Equations)		
OUT101–OUT316	Programmable output contacts. Use SELOGIC control equations to make the output contacts close for the desired conditions.	SELOGIC control equation
Display Points (SELOGIC Control Equations)		
DP1–DP16	Programmable display points. Use SELOGIC control equations to control text display.	SELOGIC control equation

Table 7.5: SET G (Global) Command Settings

Setting Name	Description	Setting Range
Selector Switch One and Two Settings (See ***Section 5: Control Logic***)		
SS1	Programmable input number 1 for controlling the setting group variable	SELOGIC control equation
SS2	Programmable input number 2 for controlling the setting group variable	SELOGIC control equation
A-, B-, C-Phase and Three-Pole Trip (See ***Section 5: Control Logic***)		
TRIPA	Programmable input that defines an A-phase trip initiation receive	SELOGIC control equation
TRIPB	Programmable input that defines a B-phase trip initiation receive	SELOGIC control equation

Setting Name	Description	Setting Range
TRIPC	Programmable input that defines a C-phase trip initiation receive	SELOGIC control equation
TRIP3	Programmable input that defines a three-phase trip initiation receive	SELOGIC control equation
A-, B-, C-Phase Breaker Status and Motor-Operated Disconnect Status (See ***Section 5: Control Logic***)		
52AA	Programmable input that defines the breaker status for A-phase	SELOGIC control equation
52AB	Programmable input that defines the breaker status for B-phase	SELOGIC control equation
52AC	Programmable input that defines the breaker status for C-phase	SELOGIC control equation
MODST	Programmable input that defines the motor-operated disconnect status	SELOGIC control equation
Automatic and Manual Breaker Close Signal (See ***Section 5: Control Logic***)		
CLOSE	Programmable input that defines an automatic close initiation receive	SELOGIC control equation
MCLOSE	Programmable input that defines a manual close initiation receive	SELOGIC control equation
Dielectric Pressure Level for Breaker 1, Breaker 2, and Curr. Transformer (See ***Section 3: Breaker Logic***)		
LOD1	Programmable input that defines dielectric pressure level 1 for the breaker	SELOGIC control equation
LOD2	Programmable input that defines dielectric pressure level 2 for the breaker	SELOGIC control equation
LODCT	Programmable input that defines dielectric pressure level for the current transformer	SELOGIC control equation

Setting Name	Description	Setting Range
Relay Settings (See ***Section 10: Event Reports and SER*** for some settings)		
LER	Event Report Length	15, 30, 60 cycles
PRE	Number of cycles of pre-event in Event Report	1 to (LER-1)
NFREQ	Nominal system frequency	50, 60 Hz
PHROT	System phase rotation	ABC, ACB
DATE_F	Date format for **DAT** command and reporting	MDY, YMD
FP_ TIMEOUT	Front-panel timeout	0–30 min 1-min steps
TGR	Setting group change delay time required before settings actually change	0–900 sec 1-sec steps
Breaker Monitor Settings (SEL-352-2 Relay only) (See ***Section 10: Event Reports and SER*** for some settings)		
EBCW	Enable breaker contact wear monitoring	Y, N
COSP1	Close/Open Set Point 1	1–65000 in steps of 1
COSP2	Close/Open Set Point 2	1–65000 in steps of 1
COSP3	Close/Open Set Point 3	1–65000 in steps of 1
KASP1	kA Interrupt Set Point 1	0.1–999.0 kA in 0.1-kA steps
KASP2	kA Interrupt Set Point 2	0.1–999.0 kA in 0.1-kA steps
KASP3	kA Interrupt Set Point 3	0.1–999.0 kA in 0.1-kA steps

Table 7.6: SET P (Port) Command Settings

Setting Name	Description	Setting Range
Port Settings (See ***Section 8: Serial Port Communications and Commands***)		
PROTO	Setting for selecting ASCII or addressed protocol	SEL, LMD, DNP (DNP for SEL-352-2 Relay only)
PREFIX	Prefix character for addressed LMD protocol	#, $, %, &, @
ADDRESS	Number for LMD protocol address	1–99
SETTLE	Serial Port settling time	0–30 sec
SPEED	Serial Port Communication baud rate	(300, 1200, 2400, 4800, 9600, 19200, 38400)
D_BITS	Serial Port Communication Data Bits	7, 8
PARITY	Serial Port Communication Parity Bit, none, even, or odd	N, E, O
STOP	Serial Port Communication Stop Bits	1, 2
TIMEOUT	Serial Port timeout	0–30 min 1-min steps
AUTO	Automatic Messages enabled on this port	Y, N
RTS_CTS	Hardware flow control enabled on this port (not available on EIA-485 Port 1)	Y, N
FAST_OP	Fast Operate Enable	Y, N
For DNP settings, see ***Appendix G: Distributed Network Protocol (DNP) 3.00***		

Table 7.7: SET T Command Settings

Setting Name	Description	Setting Range
NLB1–NLB16	Name of the local bit	14 characters
SLB1–SLB16	Text label to display when the local bit is set	7 characters
CLB1–CLB16	Text label to display when the local bit is clear	7 characters
PLB1–PLB16	Text label to display when the local bit is pulsed	7 characters
DP1_0–DP16_0	Text label to display when DPn Relay Word bit is 0	16 characters
DP1_1–DP16_1	Text label to display when DPn Relay Word bit is 1	16 characters

DEFAULT SETTINGS

The following settings are the factory default settings for a nominal 5 A relay. For a nominal 1 A relay, divide the following settings by 5: 50FT, 50LD, 50N, 37OP, 26CP, 26CF, 26TP, 26TF, 50MD. If an **R_S** command is issued, the default settings will be the new active settings.

Relay versions with only 1 or no I/O boards come from the factory with CLSLOG = OFF so settings CLSdo through CLSC do not appear. However, the **R_S** command will restore the following settings in all versions of the relay.

```
=>SHO<ENTER>
Group 1

RELID  =EXAMPLE SEL-352-1
TRMID  =EXAMPLE CIRCUIT BREAKER
Topen  = 33        Tclose = 66        SlowTr = 42.0      SlowCl = 83.0
CTR    = 600       XPTR   = 4300      YPTR   = 4300

SALOG  = OFF

50FT   = 8.60      FTLOG  = 2
FCpu   = 4.000

50LD   = 0.50      50N    = 0.50      LDLOG  = 1
LPpu   = 3.25      LDpu   = 5.50

37OP   = 2.07      47Q    = 18.7      87TH   = 4.3
VNpu   = 10.00     Kmag   = 5.0       Kang   = 10.0      THLOG  = ON
OPpu   = 3.00
26CP   = 1.110     26CF   = 1.450     26TP   = 3.490     26TF   = 4.560
CRTC   = 80        TRTC   = 80

87H    = 57.0      87FO   = 4.0       59H    = 100.0     FOLOG  = 1
FPpu   = 25.00     FFpu   = 30.00

46UB   = 16        UBLOG  = ON
UCpu   = 6.00      UPpu   = 50.00     UFpu   = 60.00

DELOG  = OFF

59L    = 57.0      27D    = 10.0      CLSLOG = 1         CLSdo  = 5.00
RCApu  = 0.00      RCBpu  = 0.00      RCCpu  = 0.00
RTPLOG = 1

SBLOG  = OFF

M86T   =FBF + LBF + TTF + CTF + FOBF + UBBF
50MD   = 0.10      TRLOG  = 2
M2pu   = 600.000   M3pu   = 600.000

MER    =UBPF + LPF + FOPF + LODPF + TRIPA + TRIPB + TRIPC +
        CLOSE + MCLOSE + 26CPA + 26CPB + 26CPC + 26TPA + 26TPB +
        26TPC + MDT

OUT101 =86BFT
OUT102 =86BFT
OUT103 =BALRM
OUT104 =!50MNA*!50MNB*!50MNC*!52AA*!52AB*!52AC
OUT105 =MDT
OUT106 =LPF + FOPF + UBPF
OUT107 =86RS
DP1    =IN104
DP2    =0
DP3    =0
DP4    =0
DP5    =0
DP6    =0
```

(continued on next page)

```
                                (continued from previous page)

DP7    =0
DP8    =0
DP9    =0
DP10   =0
DP11   =0
DP12   =0
DP13   =0
DP14   =0
DP15   =0
DP16   =0
```

```
=>SHO G<ENTER>
SS1    =0
SS2    =0
TRIPA  =IN101 + TCMD + LB1
TRIPB  =IN102 + TCMD + LB1
TRIPC  =IN103 + TCMD + LB1
TRIP3  =IN101*IN102*IN103 + TCMD + LB1
52AA   =IN104
52AB   =IN104
52AC   =IN104
MODST  =IN105
CLOSE  =IN106
MCLOSE =IN106 + CCMD + LB2
LOD1   =0
LOD2   =0
LODCT  =0
LER    = 30        PRE    = 2         NFREQ  = 60        PHROT  = ABC
DATE_F = MDY       FP_TIMEOUT= 5         TGR    = 5
```

```
=>SHO R<ENTER>
ALIAS1 =NA
ALIAS2 =NA
ALIAS3 =NA
ALIAS4 =NA
ALIAS5 =NA
ALIAS6 =NA
ALIAS7 =NA
ALIAS8 =NA
ALIAS9 =NA
ALIAS10=NA
ALIAS11=NA
ALIAS12=NA
ALIAS13=NA
ALIAS14=NA
ALIAS15=NA
ALIAS16=NA
ALIAS17=NA
ALIAS18=NA
ALIAS19=NA
ALIAS20=NA
BALRM  =FTRS FCRS 52ACV CWO TWO BDNC CAMT MCC ST SC PTD
LABEL  =Example Report Label
SER1   =NA
SER2   =NA
SER3   =NA
```

```
=>SHO P 1<ENTER>
PROTO  = SEL
SPEED  = 2400      D_BITS = 8         PARITY = N         STOP   = 1
TIMEOUT= 5         AUTO   = N         FAST_OP =N
```

```
=>SHO P 2<ENTER>

PROTO  = SEL
SPEED  = 2400      D_BITS = 8         PARITY = N         STOP   = 1
TIMEOUT= 5         AUTO   = N         RTS_CTS= N         FAST_OP =N
```

```
=>SHO P 3<ENTER>

PROTO  = SEL
SPEED  = 2400      D_BITS = 8         PARITY = N         STOP   = 1
TIMEOUT= 5         AUTO   = N         RTS_CTS= N         FAST_OP =N
```

```
=>SHO P 4<ENTER>

PROTO  = SEL
SPEED  = 2400      D_BITS = 8         PARITY = N         STOP   = 1
TIMEOUT= 5         AUTO   = N         RTS_CTS= N         FAST_OP =N
```

```
=>>SHO T<ENTER>

Text Settings
NLB1   =MANUAL TRIP    CLB1   =RETURN  SLB1   =        PLB1   =TRIP
NLB2   =MANUAL CLOSE   CLB2   =RETURN  SLB2   =        PLB2   =CLOSE
NLB3   =               CLB3   =        SLB3   =        PLB3   =
NLB4   =               CLB4   =        SLB4   =        PLB4   =
NLB5   =               CLB5   =        SLB5   =        PLB5   =
NLB6   =               CLB6   =        SLB6   =        PLB6   =
NLB7   =               CLB7   =        SLB7   =        PLB7   =
NLB8   =               CLB8   =        SLB8   =        PLB8   =
NLB9   =               CLB9   =        SLB9   =        PLB9   =
NLB10  =               CLB10  =        SLB10  =        PLB10  =
NLB11  =               CLB11  =        SLB11  =        PLB11  =
NLB12  =               CLB12  =        SLB12  =        PLB12  =
NLB13  =               CLB13  =        SLB13  =        PLB13  =
NLB14  =               CLB14  =        SLB14  =        PLB14  =
NLB15  =               CLB15  =        SLB15  =        PLB15  =
NLB16  =               CLB16  =        SLB16  =        PLB16  =
DP1_1  =BREAKER CLOSED   DP1_0  =BREAKER OPEN
DP2_1  =                 DP2_0  =
DP3_1  =                 DP3_0  =
DP4_1  =                 DP4_0  =
DP5_1  =                 DP5_0  =
DP6_1  =                 DP6_0  =

                                    (continued on next page)
```

```
                                  (continued from previous page)

DP7_1  =                  DP7_0  =
DP8_1  =                  DP8_0  =
DP9_1  =                  DP9_0  =
DP10_1 =                  DP10_0 =
DP11_1 =                  DP11_0 =
DP12_1 =                  DP12_0 =
DP13_1 =                  DP13_0 =
DP14_1 =                  DP14_0 =
DP15_1 =                  DP15_0 =
DP16_1 =                  DP16_0 =
```

DEFAULT SCHEME SELOGIC CONTROL EQUATIONS

The default schemes use hidden SELOGIC control equations for their logic. If the scheme selection settings are set to CUSTOM, all of the SELOGIC control equations are displayed for the previously selected scheme. Modify the equations to meet your specific application needs.

For example, if the fault current protection logic that you typically use is not available as one of the default schemes, find one that is close to the same logic. Set the FTLOG setting to the desired scheme (i.e., Scheme 4), and save the settings. Scheme 4 equations are now loaded into the current settings. Now set FTLOG to CUSTOM so that the SELOGIC control equations for Scheme 4 appear. You may now modify the Scheme 4 settings to meet your application needs. Save your settings. If at any time you want to go back to the default Scheme 4 settings, set FTLOG to 4 and save the settings.

Each default scheme SELOGIC control equations follow. Refer to ***Section 5: Control Logic*** for a logic diagram of the following equations.

Fault Current Protection Scheme 1

The default SELOGIC control equation settings for the fault current protection logic Scheme 1 follow:

```
TTA    =TRIPA
TTB    =TRIPB
TTC    =TRIPC

LFAS   =TRIPA*(TTAD + 50FTA)
LFAR   =!50FTA*!TTAD
LFBS   =TRIPB*(TTBD + 50FTB)
LFBR   =!50FTB*!TTBD
LFCS   =TRIPC*(TTCD + 50FTC)
LFCR   =!50FTC*!TTCD

FCA    =LFAQ
FCB    =LFBQ
FCC    =LFCQ

FBF    =FCAD + FCBD + FCCD
```

Fault Current Protection Scheme 2

The default SELOGIC control equation settings for the fault current protection logic Scheme 2 follow:

```
TTA    =NA
TTB    =NA
TTC    =NA

LFAS   =TRIPA*50FTA
LFAR   =!50FTA
LFBS   =TRIPB*50FTB
LFBR   =!50FTB
LFCS   =TRIPC*50FTC
LFCR   =!50FTC

FCA    =LFAQ
FCB    =LFBQ
FCC    =LFCQ

FBF    =FCAD + FCBD + FCCD
```

Fault Current Protection Scheme 3

The default SELOGIC control equation settings for the fault current protection logic Scheme 3 follow:

```
TTA    =NA
TTB    =NA
TTC    =NA

LFAS   =NA
LFAR   =NA
LFBS   =NA
LFBR   =NA
LFCS   =NA
LFCR   =NA

FCA    =50FTA*TRIPA
FCB    =50FTB*TRIPB
FCC    =50FTC*TRIPC

FBF    =FCAD + FCBD + FCCD
```

Fault Current Protection Scheme 4

The default SELOGIC control equation settings for the fault current protection logic Scheme 4 follow:

```
TTA    =TRIPA
TTB    =TRIPB
TTC    =TRIPC

LFAS   =NA
LFAR   =NA
LFBS   =NA
LFBR   =NA
LFCS   =NA
LFCR   =NA

FCA    =NA
FCB    =NA
FCC    =NA

FBF    =50FTA*TTAD + 50FTB*TTBD + 50FTC*TTCD
```

Fault Current Protection Scheme 5

The default SELOGIC control equation settings for the fault current protection logic Scheme 5 follow:

```
TTA    =NA
TTB    =NA
TTC    =NA

LFAS   =NA
LFAR   =NA
LFBS   =NA
LFBR   =NA
LFCS   =NA
LFCR   =NA

FCA    =TRIPA
FCB    =TRIPB
FCC    =TRIPC

FBF    =50FTA*FCAD + 50FTB*FCBD + 50FTC*FCCD
```

Load Current Protection Scheme 1

The default SELOGIC control equation settings for the load current protection logic Scheme 1 follow:

```
LLAS   =!/TRIPA*TRIPA*50LDA
LLAR   =!50LDA
LLBS   =!/TRIPB*TRIPB*50LDB
LLBR   =!50LDB
LLCS   =!/TRIPC*TRIPC*50LDC
LLCR   =!50LDC

LPA    =LLAQ
LPB    =LLBQ
LPC    =LLCQ
LDA    =LLAQ
LDB    =LLBQ
LDC    =LLCQ

L52S   =NA
L52R   =NA

AP     =NA
AF     =NA

LPF    =LPAD + LPBD + LPCD
LBF    =LDAD + LDBD + LDCD
```

Load Current Protection Scheme 2

The default SELOGIC control equation settings for the load current protection logic Scheme 2 follow:

```
LLAS   =!/TRIPA*TRIPA*50LDA
LLAR   =!50LDA
LLBS   =!/TRIPB*TRIPB*50LDB
LLBR   =!50LDB
LLCS   =!/TRIPC*TRIPC*50LDC
LLCR   =!50LDC

LPA    =LLAQ
LPB    =LLBQ
LPC    =LLCQ
LDA    =LLAQ
LDB    =LLBQ
LDC    =LLCQ

L52S   =/TRIP3
L52R   =!52AA*!52AB*!52AC + 86BFT

AP     =L52Q
AF     =L52Q

LPF    =LPAD + LPBD + LPCD + APD
LBF    =LDAD + LDBD + LDCD + AFD
```

Thermal Protection of Trip and Close Resistors

The default SELOGIC control equation settings for the thermal protection logic follow:

```
OPA    =37OPA*87THA
OPB    =37OPB*87THB
OPC    =37OPC*87THC

LTAS   =CLOSE + MCLOSE
LTAR   =TRIPA
LTBS   =CLOSE + MCLOSE
LTBR   =TRIPB
LTCS   =CLOSE + MCLOSE
LTCR   =TRIPC

TRMEA  =OPAD*!LTAQ
TRMEB  =OPBD*!LTBQ
TRMEC  =OPCD*!LTCQ

CRMEA  =OPAD*LTAQ*!(52AA*X27DA*Y59LA + 52AA*Y27DA*X59LA)
CRMEB  =OPBD*LTBQ*!(52AB*X27DB*Y59LB + 52AB*Y27DB*X59LB)
CRMEC  =OPCD*LTCQ*!(52AC*X27DC*Y59LC + 52AC*Y27DC*X59LC)

TTF    =(26TFA*50MNA) + (26TFB*50MNB) + (26TFC*50MNC)
CTF    =(26CFA*50MNA) + (26CFB*50MNB) + (26CFC*50MNC)
```

NOTE: !(X + Y) => !X * !Y
!(X * Y) => !X + !Y

Flashover Protection Scheme 1

The default SELOGIC control equation settings for the flashover protection logic Scheme 1 follow:

```
F1A    =87HA
F1B    =87HB
F1C    =87HC
F2A    =50LDA
F2B    =50LDB
F2C    =50LDC
F3A    =TRIPA + CLOSE + MCLOSE
F3B    =TRIPB + CLOSE + MCLOSE
F3C    =TRIPC + CLOSE + MCLOSE

LHAS   =NA
LHAR   =NA
LHBS   =NA
LHBR   =NA
LHCS   =NA
LHCR   =NA

LVAS   =F1AD*!87HA*!F2AD*50LDA*!87FOA*!F3AD
LVAR   =!(50LDA*!F3AD*!87FOA)
LVBS   =F1BD*!87HB*!F2BD*50LDB*!87FOB*!F3BD
LVBR   =!(50LDB*!F3BD*!87FOB)
LVCS   =F1CD*!87HC*!F2CD*50LDC*!87FOC*!F3CD
LVCR   =!(50LDC*!F3CD*!87FOC)

FPA    =LVAQ
FPB    =LVBQ
FPC    =LVCQ

FFA    =LVAQ
FFB    =LVBQ
FFC    =LVCQ

FOPF   =FPAD + FPBD + FPCD
FOBF   =FFAD + FFBD + FFCD
```

Flashover Protection Scheme 2

The default SELOGIC control equation settings for the flashover protection logic Scheme 2 follow:

```
F1A    =X59LA
F1B    =X59LB
F1C    =X59LC
F2A    =50LDA
F2B    =50LDB
F2C    =50LDC
F3A    =TRIPA + CLOSE + MCLOSE
F3B    =TRIPB + CLOSE + MCLOSE
F3C    =TRIPC + CLOSE + MCLOSE

LHAS   =F1AD
LHAR   =!50LDA
LHBS   =F1BD
LHBR   =!50LDB
LHCS   =F1CD
LHCR   =!50LDC

LVAS   =LHAQ*!F2AD*50LDA*!52AA*!F3AD
LVAR   =!50LDA + F3AD + 52AA
LVBS   =LHBQ*!F2BD*50LDB*!52AB*!F3BD
LVBR   =!50LDB + F3BD + 52AB
LVCS   =LHCQ*!F2CD*50LDC*!52AC*!F3CD
LVCR   =!50LDC + F3CD + 52AC

FPA    =LVAQ
FPB    =LVBQ
FPC    =LVCQ

FFA    =LVAQ
FFB    =LVBQ
FFC    =LVCQ

FOPF   =FPAD + FPBD + FPCD
FOBF   =FFAD + FFBD + FFCD
```

Unbalanced Current Protection

The default SELOGIC control equation settings for the unbalanced current protection logic follow:

```
UC     =CLOSE + MCLOSE

LUS    =UCD*50LD*(46A + 46B + 46C)
LUR    =!50LD + !(46A + 46B + 46C)

UPA    =LUQ*46A
UPB    =LUQ*46B
UPC    =LUQ*46C

UFA    =LUQ*46A
UFB    =LUQ*46B
UFC    =LUQ*46C

UBPF   =UPAD + UPBD + UPCD
UBBF   =UFAD + UFBD + UFCD
```

NOTE: **!(X + Y) => !X * !Y**
!(X * Y) => !X + !Y

Loss-of-Dielectric Detection

The default SELOGIC control equation settings for the loss-of-dielectric detection logic follow:

```
LT1    =LOD1
LT2    =LOD2
LT3    =LODCT

LODPF  =!LT1D*LT2D + LT3D
LODBF  =!LT2D*LT1D
```

Controlled Closing Scheme 1 (Staggered Closing)

The default SELOGIC control equation settings for the controlled closing logic Scheme 1 follow:

```
RCLS   =TRIPA + TRIPB + TRIPC

RCA    =CLOSE + MCLOSE
RCB    =CLOSE + MCLOSE
RCC    =CLOSE + MCLOSE

CCT    =NA
MCT    =NA
SYNCT  =NA
SCT    =NA

ZCNA   =NA
ZCNB   =NA
ZCNC   =NA

ZCPA   =NA
ZCPB   =NA
ZCPC   =NA

PCNA   =NA
PCNB   =NA
PCNC   =NA

PCPA   =NA
PCPB   =NA
PCPC   =NA

SYNCEN =NA

CCA    =RCAD
CCB    =RCBD
CCC    =RCCD
```

Controlled Closing Scheme 2 (Point-on-Wave Closing)

The default SELOGIC control equation settings for the controlled closing logic Scheme 2 follow:

```
RCLS   =TRIPA + TRIPB + TRIPC

RCA    =NA
RCB    =NA
RCC    =NA

CCT    =CLOSE
MCT    =MCLOSE
SYNCT  =CLOSE
SCT    =25M*MCTD + !X59L3*!Y59L3*MCTD + 25C*SYNCTD

ZCNA   =(CCTD + MCTD)*!XPTA*!XNTA*!YPTA*!YNTA*(X59L3*!Y59L3 + !X59L3*Y59L3)
ZCNB   =(CCTD + MCTD)*!XPTB*!XNTB*!YPTB*!YNTB*(X59L3*!Y59L3 + !X59L3*Y59L3)
ZCNC   =(CCTD + MCTD)*!XPTC*!XNTC*!YPTC*!YNTC*(X59L3*!Y59L3 + !X59L3*Y59L3)

ZCPA   =NA
ZCPB   =NA
ZCPC   =NA

PCNA   =(CCTD + MCTD)*(XNTA + YNTA)*(X59L3*!Y59L3 + !X59L3*Y59L3)
PCNB   =(CCTD + MCTD)*(XNTB + YNTB)*(X59L3*!Y59L3 + !X59L3*Y59L3)
PCNC   =(CCTD + MCTD)*(XNTC + YNTC)*(X59L3*!Y59L3 + !X59L3*Y59L3)

PCPA   =(CCTD + MCTD)*(XPTA + YPTA)*(X59L3*!Y59L3 + !X59L3*Y59L3)
PCPB   =(CCTD + MCTD)*(XPTB + YPTB)*(X59L3*!Y59L3 + !X59L3*Y59L3)
PCPC   =(CCTD + MCTD)*(XPTC + YPTC)*(X59L3*!Y59L3 + !X59L3*Y59L3)

SYNCEN =!52AA*!52AB*!52AC

CCA    =CTAD + SCTD
CCB    =CTBD + SCTD
CCC    =CTCD + SCTD
```

Retripping Scheme 1

The default SELOGIC control equation settings for the retripping logic Scheme 1 follow:

```
LRTAS  =NA
LRTAR  =NA
LRTBS  =NA
LRTBR  =NA
LRTCS  =NA
LRTCR  =NA

RT1    =NA
RT2    =NA
RT3    =NA

RTA    =TRIPA
RTB    =TRIPB
RTC    =TRIPC
```

Retripping Scheme 2

The default SELOGIC control equation settings for the retripping logic Scheme 2 follow:

```
LRTAS  =TRIPA*50LDA
LRTAR  =!50LDA
LRTBS  =TRIPB*50LDB
LRTBR  =!50LDB
LRTCS  =TRIPC*50LDC
LRTCR  =!50LDC

RT1    =LRTAQ
RT2    =LRTBQ
RT3    =LRTCQ

RTA    =RT1D
RTB    =RT2D
RTC    =RT3D
```

Lockout Relay Control Scheme 1 (No MOD Trip)

The default SELOGIC control equation settings for the lockout relay control logic Scheme 1 follow:

```
M1     =M4D

L1MS   =M86T*!M1D
L1MR   =M1D

M2     =L1MQ

L2MS   =NA
L2MR   =NA

M3     =NA

L3MS   =M86T
L3MR   =!M86T*!50MD*M2D

M4     =!M86T*!50MD*M2D

MDT    =NA
86RS   =M4D*!(CTF + TTF)
86BFT  =L3MQ
```

Lockout Relay Control Scheme 2 (MOD Tripping)

The default SELOGIC control equation settings for the loss-of-dielectric detection logic follow:

```
M1     =M4D

L1MS   =M86T*!M1D
L1MR   =M1D

M2     =L1MQ

L2MS   =!M1D*!50MD*M2D
L2MR   =M1D

M3     =L2MQ

L3MS   =M86T
L3MR   =!M86T*!(50LD + MODST)*M3D

M4     =!M86T*!(50LD + MODST)*M3D

MDT    =!50MD*M2D
86RS   =M4D
86BFT  =L3MQ
```

SETTINGS SHEETS

The Settings Sheets that follow present every SEL-352 Relay setting:

Pages 1–2	Report Settings (SET R
Pages 3–21	Group Settings (SET)
Pages 22–23	Global Settings (SET G)
Pages 24-26	Port Settings (SET P)
Pages 27–28	Text Settings (SET T)

Categorization of group (SET) settings is according to the Function column of Table 7.8. Note that functions involving logic settings can be set to "Off," a predefined scheme, or "Custom." Simple settings sheet arrangement and presentation of each scheme and custom logic setting make it easy for you to consider only the settings necessary for your application.

Table 7.8: SET Command Categories

Function	Logic Selection		
General Data			
Breaker Monitor and Miscellaneous			
SELOGIC A	OFF		CUSTOM
Fault Current Logic Settings	OFF	1, 2, 3, 4, 5	CUSTOM
Load Current Logic Settings	OFF	1, 2	CUSTOM

Function	Logic Selection		
Thermal Protection Logic Settings	OFF	ON	CUSTOM
Flashover Protection Logic Settings	OFF	1, 2	CUSTOM
Unbalanced Current Protection Logic Settings	OFF	ON	CUSTOM
Dielectric Monitor Logic Settings	OFF	ON	CUSTOM
Controlled Close Logic Settings	OFF	1, 2	CUSTOM
Retrip Logic Settings	OFF	1, 2	CUSTOM
SELOGIC B	OFF		CUSTOM
86BF Trip and Reset Logic Settings	OFF	1, 2	CUSTOM
Event Report Trigger and SELOGIC Output Equations			
Display Point Elements			

Report Settings (SET R Command)

Input, Output, and Element Aliases

Alias syntax is as follows: *ELEMENT*<SPACE>*ALIAS_NAME*. Aliases may contain the characters A–Z, 0–9, or '_'. For example: ALIAS1 = IN101 BREAKER_OPEN. Fifteen characters may be used in each alias. Set alias names and use these aliases in SELOGIC® control equations to ensure valid SEL-5010 setting comparison.

ALIAS1 = _____

ALIAS2 = _____

ALIAS3 = _____

ALIAS4 = _____

ALIAS5 = _____

ALIAS6 = _____

ALIAS7 = _____

ALIAS8 = _____

ALIAS9 = _____

ALIAS10 = _____

ALIAS11 = _____

ALIAS12 = _____

ALIAS13 = _____

ALIAS14 = _____

ALIAS15 = _____

ALIAS16 = _____

ALIAS17 = _____

ALIAS18 = _____

ALIAS19 = _____

ALIAS20 = _____

Breaker Monitor

Description	**Range**
Breaker Alarm Types	FTRS, FCRS, 52ACV, CWO, TWO, BDNC, CAMT, MCC, ST, SC, PTD

BALRM = _____

Report Settings (SET R Command) (cont.)

Sequential Events Recorder Settings

Description	Range
Report Label	59 Characters (Text strings may contain any printing character (A–Z, 0–9, space, ., etc.), but they cannot start with ^, <, or >.)
LABEL =	_____

Relay Element Event Trigger List Settings

Description	Range
Relay Element Event Trigger Lists	Maximum of 24 Relay Word bits per list, with space or comma delimiters between bits.
SER1 =	_____
SER2 =	_____
SER3 =	_____

Group ☐ Settings (SET Command)

General Data

Description	Range			
Relay Identifier:	17 Characters	**RELID**	=	
Terminal Identifier:	39 Characters	**TRMID**	=	

Breaker Monitor and Miscellaneous

Description	Range			
Nominal Breaker Trip Time	0–999 ms in 1-ms steps	**Topen**	=	
Nominal Breaker Close Time	0–320 ms in 1-ms steps	**Tclose**	=	
Slow Trip Alarm	0.0–999.0 ms in 0.1-ms steps	**SlowTr**	=	
Slow Close Alarm	0.0–999.0 ms in 0.1-ms steps	**SlowCl**	=	
Current Transformer Ratio	1–10000 in increments of 1	**CTR**	=	
X-Side Potential Transformer Ratio	1–10000 in increments of 1	**XPTR**	=	
Y-Side Potential Transformer Ratio	1–10000 in increments of 1	**YPTR**	=	

SELOGIC A

Description	Range			
SELOGIC Set A	OFF, CUSTOM	**SALOG**	=	

If SALOG = Custom

62T1A Pickup Time	0–8191 cycles in 1/8-cycle steps	**T1Apu**	=	
62T1A Dropout Time	0–8191 cycles in 1/8-cycle steps	**T1Ado**	=	
62T1B Pickup Time	0–8191 cycles in 1/8-cycle steps	**T1Bpu**	=	
62T1B Dropout Time	0–8191 cycles in 1/8-cycle steps	**T1Bdo**	=	
62T1C Pickup Time	0–8191 cycles in 1/8-cycle steps	**T1Cpu**	=	
62T1C Dropout Time	0–8191 cycles in 1/8-cycle steps	**T1Cdo**	=	

Latch L1A, L1B, and L1C Inputs

L1AS =
L1AR =
L1BS =
L1BR =
L1CS =
L1CR =

SELOGIC A (cont.)

Timer T1A, T1B, and T1C Inputs

T1A =

T1B =

T1C =

SELOGIC Set A Elements

SAA =

SAB =

SAC =

Fault Current Logic Settings[1]

Description	Range			
Fault Current Detector	0.50–45.00 A in 0.01-A steps	(5 A)		
	0.10–9.00 A in 0.01-A steps	(1 A)	**50FT** =	
RMS Current Detector	0.50–45.00 A in 0.10-A steps	(5 A)		
(Only available in SEL-352-2 Relay)	0.10–9.00 A in 0.02-A steps	(1 A)	**50RMS** =	
Fault Current Logic	OFF, 1–5, CUSTOM		**FTLOG** =	
If FTLOG = 1				
62TT Trip Timer Dropout Time	0–8191 cycles in 1/8-cycle steps		**TTdo** =	
62FC Fault Current Pickup Time	0–8191 cycles in 1/8-cycle steps		**FCpu** =	
If FTLOG = 2				
62FC Fault Current Pickup Time	0–8191 cycles in 1/8-cycle steps		**FCpu** =	
If FTLOG = 3				
62FC Fault Current Pickup Time	0–8191 cycles in 1/8-cycle steps		**FCpu** =	
If FTLOG = 4				
62TT Trip Timer Pickup Time	0–8191 cycles in 1/8-cycle steps		**TTpu** =	
62TT Trip Timer Dropout Time	0–8191 cycles in 1/8-cycle steps		**TTdo** =	
If FTLOG = 5				
62FC Fault Current Pickup Time	0–8191 cycles in 1/8-cycle steps		**FCpu** =	
If FTLOG = Custom				
62TT Trip Timer Pickup Time	0–8191 cycles in 1/8-cycle steps		**TTpu** =	
62TT Trip Timer Dropout Time	0–8191 cycles in 1/8-cycle steps		**TTdo** =	
62FC Fault Current Pickup Time	0–8191 cycles in 1/8-cycle steps		**FCpu** =	

[1] Amperes are set in secondary quantities.

Fault Current Logic Settings[1] (cont.)

Fault Current Timer 62TTA, 62TTB, and 62TTC Inputs

TTA =
TTB =
TTC =

Fault Current Latch LFA, LFB, and LFC Inputs

LFAS =
LFAR =
LFBS =
LFBR =
LFCS =
LFCR =

Fault Current Timer FCA, FCB, and FCC Inputs

FCA =
FCB =
FCC =

Fault Current Breaker Failure

FBF =

Load Current Logic Settings[1]

Description	Range			
Load Current Detector	0.10–45.00 A in 0.01-A steps	(5 A)		
	0.02–9.00 A in 0.01-A steps	(1 A)	**50LD** =	
Ground Current Detector	0.10–45.00 A in 0.01-A steps	(5 A)		
	0.02–9.00 A in 0.01-A steps	(1 A)	**50N** =	
Load Current Logic	OFF, 1, 2, CUSTOM		**LDLOG** =	
If LDLOG = 1				
62LP Pending Failure Pickup Time	0–16383 cycles in 1/4-cycle steps		**LPpu** =	
62LD Breaker Failure Pickup Time	0–16383 cycles in 1/4-cycle steps		**LDpu** =	
If LDLOG = 2				
62LP Pending Failure Pickup Time	0–16383 cycles in 1/4-cycle steps		**LPpu** =	
62LD Breaker Failure Pickup Time	0–16383 cycles in 1/4-cycle steps		**LDpu** =	
62AP 52A Pending Failure Time	0–16383 cycles in 1/4-cycle steps		**APpu** =	
62AF 52A Breaker Failure Time	0–16383 cycles in 1/4-cycle steps		**AFpu** =	

[1] Amperes are set in secondary quantities.

Load Current Logic Settings[1] (cont.)

If LDLOG = Custom

62LP Pending Failure Pickup Time	0–16383 cycles in 1/4-cycle steps	**LPpu**	**=**	
62LD Breaker Failure Pickup Time	0–16383 cycles in 1/4-cycle steps	**LDpu**	**=**	
62AP 52A Pending Failure Time	0–16383 cycles in 1/4-cycle steps	**APpu**	**=**	
62AF 52A Breaker Failure Time	0–16383 cycles in 1/4-cycle steps	**AFpu**	**=**	

Load Current Latch LLA, LLB, and LLC Inputs

LLAS = _____

LLAR = _____

LLBS = _____

LLBR = _____

LLCS = _____

LLCR = _____

Load Current Timer 62LP and 62LD Inputs

LPA = _____

LPB = _____

LPC = _____

LDA = _____

LDB = _____

LDC = _____

Load Current 52 Latch Inputs

L52S = _____

L52R = _____

Load Current Timer 62AP and 62AF Inputs

AP = _____

AF = _____

Load Current Pending Failure

LPF = _____

Load Current Breaker Failure

LBF = _____

[1] Amperes are set in secondary quantities.

Thermal Protection Logic Settings[2]

Description	Range			
Phase Overpower Element	0.10–3400.00 W in 0.01-W steps (5 A) 0.02–680.00 W in 0.01-W steps (1 A)	**37OP**	=	
Negative Sequence Voltage[3]	2.0–140.0 V in 0.1-V steps	**47Q**	=	
Thermal Model Voltage Threshold	1.0–150.0 V in 0.1-V steps	**87TH**	=	
62VN Voltage Nulling Delay Time	0.00–240.00 minutes in 0.01-min steps	**VNpu**	=	
Maximum Voltage Magnitude Error to Null	0.0–30.0% in 0.1% steps	**Kmag**	=	
Maximum Phase Angle Error to Null	0.0–15.0° in 0.1° steps	**Kang**	=	
Resistor Protection Logic	OFF, ON, CUSTOM	**THLOG**	=	
If THLOG = ON				
62OP Thermal Overpower Pickup	0–16383 cycles in 1/4-cycle steps	**OPpu**	=	
Close Resistor Alarm Energy	0.010–1000.000 J in 0.001-J steps (5 A) 0.002–200.000 J in 0.001-J steps (1 A)	**26CP**	=	
Close Resistor Failure Energy	0.010–1000.000 J in 0.001-J steps (5 A) 0.002–200.000 J in 0.001-J steps (1 A)	**26CF**	=	
Trip Resistor Alarm Energy	0.010–1000.000 J in 0.001-J steps (5 A) 0.002–200.000 J in 0.001-J steps (1 A)	**26TP**	=	
Trip Resistor Failure Energy	0.010–1000.000 J in 0.001-J steps (5 A) 0.002–200.000 J in 0.001-J steps (1 A)	**26TF**	=	
Close Resistor Cooling Time Constant	1–1140 minutes in 1-min steps	**CRTC**	=	
Trip Resistor Cooling Time Constant	1–1140 minutes in 1-min steps	**TRTC**	=	
If THLOG = Custom				
62OP Thermal Overpower Pickup	0–16383 cycles in 1/4-cycle steps	**OPpu**	=	
Close Resistor Alarm Energy	0.010–1000.000 J in 0.001-J steps (5 A) 0.002–200.000 J in 0.001-J steps (1 A)	**26CP**	=	
Close Resistor Failure Energy	0.010–1000.000 J in 0.001-J steps (5 A) 0.002–200.000 J in 0.001-J steps (1 A)	**26CF**	=	
Trip Resistor Alarm Energy	0.010–1000.000 J in 0.001-J steps (5 A) 0.002–200.000 J in 0.001-J steps (1 A)	**26TP**	=	
Trip Resistor Failure Energy	0.010–1000.000 J in 0.001-J steps (5 A) 0.002–200.000 J in 0.001-J steps (1 A)	**26TF**	=	
Close Resistor Cooling Time Constant	1–1140 minutes in 1-min steps	**CRTC**	=	
Trip Resistor Cooling Time Constant	1–1140 minutes in 1-min steps	**TRTC**	=	

[2] Volts, Watts, and Joules are set in secondary quantities.

[3] Not used in default logic.

Thermal Protection Logic Settings[2] (cont.)

Thermal Protection Timer 62OP Inputs

OPA = _____
OPB = _____
OPC = _____

Thermal Protection Latch LTA, LTB, and LTC Inputs

LTAS = _____
LTAR = _____
LTBS = _____
LTBR = _____
LTCS = _____
LTCR = _____

Trip Resistor Thermal Model Enables

TRMEA = _____
TRMEB = _____
TRMEC = _____

Close Resistor Thermal Model Enables

CRMEA = _____
CRMEB = _____
CRMEC = _____

Trip Resistor Thermal Failure

TTF = _____

Close Resistor Thermal Failure

CTF = _____

[2] Volts, Watts, and Joules are set in secondary quantities.

Flashover Protection Logic Settings[4]

Description	Range			
Flashover Voltage Difference	1.0–150.0 V in 0.1-V steps	**87H**	=	
Post Flashover Voltage Difference	1.0–150.0 V in 0.1-V steps	**87FO**	=	
Flashover Phase Voltage	1.0–130.0 V in 0.1-V steps	**59H**	=	
Flashover Protection Logic	OFF, 1, 2, CUSTOM	**FOLOG**	=	
If FOLOG = 1				
62FP Pending Failure Pickup Time	0–16383 cycles in 1/4-cycle steps	**FPpu**	=	
62FF Breaker Failure Pickup Time	0–16383 cycles in 1/4-cycle steps	**FFpu**	=	
If FOLOG = 2				
62FP Pending Failure Pickup Time	0–16383 cycles in 1/4-cycle steps	**FPpu**	=	
62FF Breaker Failure Pickup Time	0–16383 cycles in 1/4-cycle steps	**FFpu**	=	
If FOLOG = Custom				
62FP Pending Failure Pickup Time	0–16383 cycles in 1/4-cycle steps	**FPpu**	=	
62FF Breaker Failure Pickup Time	0–16383 cycles in 1/4-cycle steps	**FFpu**	=	

Flashover Protection Timer F1, F2, and F3 Inputs

F1A = _____
F1B = _____
F1C = _____
F2A = _____
F2B = _____
F2C = _____
F3A = _____
F3B = _____
F3C = _____

Flashover Protection Latch LHA, LHB, and LHC Inputs

LHAS = _____
LHAR = _____
LHBS = _____
LHBR = _____
LHCS = _____
LHCR = _____

[4] Volts are set in secondary quantities.

Flashover Protection Logic Settings[4] (cont.)

Flashover Protection Latch LVA, LVB, and LVC Inputs

LVAS = _____

LVAR = _____

LVBS = _____

LVBR = _____

LVCS = _____

LVCR = _____

Flashover Pending Failure Timer FPA, FPB, and FPC Inputs

FPA = _____

FPB = _____

FPC = _____

Flashover Breaker Failure Timer FFA, FFB, and FFC Inputs

FFA = _____

FFB = _____

FFC = _____

Flashover Pending Failure

FOPF = _____

Flashover Breaker Failure

FOBF = _____

[4] Volts are set in secondary quantities.

Unbalanced Current Protection Logic Settings

Description	Range		
Phase Current Unbalance Ratio	8, 16, 32, 64	**46UB**	=
Phase Current Unbalance Logic	OFF, ON, CUSTOM	**UBLOG**	=

If UBLOG = ON

62UC Close Input Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**UCpu**	=
62UP Pending Failure Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**UPpu**	=
62UF Breaker Failure Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**UFpu**	=

If UBLOG = Custom

62UC Close Input Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**UCpu**	=
62UP Pending Failure Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**UPpu**	=
62UF Breaker Failure Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**UFpu**	=

Current Unbalance Timer 62UC Input

UC =

Current Unbalance Latch LU Input

LUS =

LUR =

Current Unbalance Timer 62UP Pending Failure Inputs

UPA =

UPB =

UPC =

Current Unbalance Timer 62UF Breaker Failure Inputs

UFA =

UFB =

UFC =

Current Unbalance Pending Failure

UBPF =

Current Unbalance Breaker Failure

UBBF =

Dielectric Monitor Logic Settings

Description	Range		
Loss of Dielectric Logic	OFF, ON, CUSTOM	**DELOG**	=
If DELOG = ON			
62L2 Leak Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**L2pu**	=
If DELOG = Custom			
62L2 Leak Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**L2pu**	=
Loss of Dielectric Timer 62LT1, 62LT2, and 62LT3			
LT1 =			
LT2 =			
LT3 =			
Loss of Dielectric Pending Failure			
LODPF =			
Loss of Dielectric Breaker Failure			
LODBF =			

Controlled Close Logic Settings[4]

Description	Range		
Live Line/Bus Voltage	10.0–120.0 V in 0.1-V steps	**59L**	=
Dead Line/Bus Under Voltage	1.0–120.0 V in 0.1-V steps	**27D**	=
Controlled Close Logic	OFF, 1, 2, CUSTOM	**CLSLOG**	=
If CLSLOG = 1			
62CLS Timer Dropout Time	0–16383 cycles in 1/4-cycle steps	**CLSdo**	=
62RCA Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**RCApu**	=
62RCB Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**RCBpu**	=
62RCC Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**RCCpu**	=
If CLSLOG = 2			
62CLS Timer Dropout Time	0–16383 cycles in 1/4-cycle steps	**CLSdo**	=
Maximum Slip Freq. for Control Close	0.005–0.500 Hz in 0.001-Hz steps	**25SC**	=
Maximum Control Close Angle	32 • 25SC to 90° (min =1) in 0.1° steps	**25AC**	=
Maximum Slip Freq. for Manual Close	0.005–0.500 Hz in 0.001-Hz steps	**25SM**	=
Maximum Manual Close Angle	32 • 25SM to 90° (min =1) in 0.1° steps	**25AM**	=
Synchronizing Phase	A, B, C	**SYNCP**	=

[4] Volts are set in secondary quantities.

Controlled Close Logic Settings[4] (cont.)

62SYNC Timer Dropout Time	0–99999 cycles in 1/4-cycle steps	**SYNCdo** =	
62PCA Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**PCApu** =	
62PCB Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**PCBpu** =	
62PCC Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**PCCpu** =	
62ZCA Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**ZCApu** =	
62ZCB Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**ZCBpu** =	
62ZCC Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**ZCCpu** =	
Close Phase A (Output)	**CLSA** =		
Close Phase B (Output)	**CLSB** =		
Close Phase C (Output)	**CLSC** =		

If CLSLOG = Custom

62CLS Timer Dropout Time	0–16383 cycles in 1/4-cycle steps	**CLSdo** =	
62RCA Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**RCApu** =	
62RCB Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**RCBpu** =	
62RCC Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**RCCpu** =	
Maximum Slip Freq. for Control Close	0.005–0.5 Hz in 0.001-Hz steps	**25SC** =	
Maximum Control Close Angle	32 • 25SC to 90° (min =1), in 0.1° steps	**25AC** =	
Maximum Slip Freq. for Manual Close	0.005–0.500 Hz in 0.001-Hz steps	**25SM** =	
Maximum Manual Close Angle	32 • 25SM to 90° (min =1), in 0.1° steps	**25AM** =	
Synchronizing Phase	A, B, C	**SYNCP** =	
62SYNC Timer Dropout Time	0–99999 cycles in 1/4-cycle steps	**SYNCdo** =	
62PCA Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**PCApu** =	
62PCB Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**PCBpu** =	
62PCC Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**PCCpu** =	
62ZCA Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**ZCApu** =	
62ZCB Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**ZCBpu** =	
62ZCC Timer Pickup Time	0.00–40.00 ms in 0.01-ms steps	**ZCCpu** =	
Close Phase A (Output)	**CLSA** =		
Close Phase B (Output)	**CLSB** =		
Close Phase C (Output)	**CLSC** =		

Controlled Close Timer Reset Input

RCLS = _____

[4] Volts are set in secondary quantities.

Controlled Close Logic Settings[4] (cont.)

Controlled Close RCA, RCB, and RCC Inputs

RCA = _____

RCB = _____

RCC = _____

Controlled Close Timer CCT, MCT, SYNCT, and SCT Inputs

CCT = _____

MCT = _____

SYNCT = _____

SCT = _____

Controlled Close Negative Zero Crossing

ZCNA = _____

ZCNB = _____

ZCNC = _____

Controlled Close Positive Zero Crossing

ZCPA = _____

ZCPB = _____

ZCPC = _____

Controlled Close Negative Peak Crossing

PCNA = _____

PCNB = _____

PCNC = _____

Controlled Close Positive Peak Crossing

PCPA = _____

PCPB = _____

PCPC = _____

Controlled Close Synchronism Logic Enable

SYNCEN = _____

[4] Volts are set in secondary quantities.

Controlled Close Logic Settings[4] (cont.)

Controlled Close CCA, CCB, and CCC Outputs

CCA = _____

CCB = _____

CCC = _____

Retrip Logic Settings

Description	Range			
Circuit Breaker Retrip Logic	OFF, 1, 2, CUSTOM	**RTPLOG**	=	_____
If RTPLOG = 1[5]				
If RTPLOG = 2				
62RT Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**RTpu**	=	_____
If RTPLOG = Custom				
62RT Timer Pickup Time	0–16383 cycles in 1/4-cycle steps	**RTpu**	=	_____

Circuit Breaker Retrip Latch LRTA, LRTB, and LRTC Inputs

LRTAS = _____

LRTAR = _____

LRTBS = _____

LRTBR = _____

LRTCS = _____

LRTCR = _____

Circuit Breaker Retrip Timer RT1, RT2, and RT3 Inputs

RT1 = _____

RT2 = _____

RT3 = _____

Circuit Breaker Retrip RTA, RTB, and RTC

RTA = _____

RTB = _____

RTC = _____

[4] Volts are set in secondary quantities.

[5] There are no additional settings for RTPLOG = 1.

SELOGIC B

Description	Range			
SELOGIC Set B	OFF, CUSTOM	**SBLOG**	=	
If SBLOG = Custom				
62T2A Pickup Time	0–16383 cycles in 1/4-cycle steps	**T2Apu**	=	
62T2A Dropout Time	0–16383 cycles in 1/4-cycle steps	**T2Ado**	=	
62T2B Pickup Time	0–16383 cycles in 1/4-cycle steps	**T2Bpu**	=	
62T2B Dropout Time	0–16383 cycles in 1/4-cycle steps	**T2Bdo**	=	
62T2C Pickup Time	0–16383 cycles in 1/4-cycle steps	**T2Cpu**	=	
62T2C Dropout Time	0–16383 cycles in 1/4-cycle steps	**T2Cdo**	=	
62T3A Pickup Time	0–16383 cycles in 1/4-cycle steps	**T3Apu**	=	
62T3A Dropout Time	0–16383 cycles in 1/4-cycle steps	**T3Ado**	=	
62T3B Pickup Time	0–16383 cycles in 1/4-cycle steps	**T3Bpu**	=	
62T3B Dropout Time	0–16383 cycles in 1/4-cycle steps	**T3Bdo**	=	
62T3C Pickup Time	0–16383 cycles in 1/4-cycle steps	**T3Cpu**	=	
62T3C Dropout Time	0–16383 cycles in 1/4-cycle steps	**T3Cdo**	=	

Latch L2A, L2B, and L2C Inputs

L2AS =
L2AR =
L2BS =
L2BR =
L2CS =
L2CR =

Latch L3A, L3B, and L3C Inputs

L3AS =
L3AR =
L3BS =
L3BR =
L3CS =
L3CR =

Timer T2A, T2B, and T2C Inputs

T2A =
T2B =
T2C =

Latch L4A, L4B, and L4C Inputs

L4AS =
L4AR =

SELOGIC B (cont.)

L4BS =
L4BR =
L4CS =
L4CR =

Latch L5A, L5B, and L5C Inputs

L5AS =
L5AR =
L5BS =
L5BR =
L5CS =
L5CR =

Timer T3A, T3B, and T3C Inputs

T3A =
T3B =
T3C =

Latch L6A, L6B, and L6C Inputs

L6AS =
L6AR =
L6BS =
L6BR =
L6CS =
L6CR =

Latch L7A, L7B, and L7C Inputs

L7AS =
L7AR =
L7BS =
L7BR =
L7CS =
L7CR =

SELOGIC Set B Elements

SBA =
SBB =
SBC =

86BF Trip and Reset Logic Settings[1]

M86T Trip Equation

M86T = _____

Description	Range				
MOD Operating Current	0.10–45.00 A in 0.01-A steps 0.02–9.00 A in 0.01-A steps	(5 A) (1 A)	**50MD**	=	
86BF Trip and Reset Logic	OFF, 1, 2, CUSTOM		**TRLOG**	=	
If TRLOG = 1					
62M2 Timer Pickup Time	0–8191 cycles in 1/8-cycle steps		**M2pu**	=	
If TRLOG = 2					
62M2 Timer Pickup Time	0–8191 cycles in 1/8-cycle steps		**M2pu**	=	
62M3 Timer Pickup Time	0-8191 cycles in 1/8-cycle steps		**M3pu**	=	

Trip and Reset Timer M1 Input

M1 = _____

Trip and Reset Latch L1M Inputs

L1MS = _____

L1MR = _____

Trip and Reset Timer M2 Input

M2 = _____

Trip and Reset Latch L2M Inputs

L2MS = _____

L2MR = _____

Trip and Reset Timer M3 Input

M3 = _____

Trip and Reset Latch L3M Inputs

L3MS = _____

L3MR = _____

[1] Amperes are set in secondary quantities.

86BF Trip and Reset Logic Settings[1] (cont.)
Trip and Reset Timer M4 Input
M4 =
Motor-Operated Disconnect Trip
MDT =
Lockout Reset
86RS =
Breaker Failure Trip
86BFT =

[1] Amperes are set in secondary quantities.

Event Report Trigger Equation and SELOGIC Output Equations

Event Report Trigger Equation (SELOGIC control equation)

MER =

Mainboard Output Contacts (SELOGIC control equations)

OUT101 =
OUT102 =
OUT103 =
OUT104 =
OUT105 =
OUT106 =
OUT107 =

Interface Board #1 Output Contacts (SELOGIC control equations)

OUT201 =
OUT202 =
OUT203 =
OUT204 =
OUT205 =
OUT206 =
OUT207 =
OUT208 =
OUT209 =
OUT210 =
OUT211 =
OUT212 =
OUT213 =
OUT214 =
OUT215 =
OUT216 =

Event Report Trigger Equation and SELOGIC Output Equations (cont.)

Interface Board #2 Output Contacts (SELOGIC control equations)

OUT301 =
OUT302 =
OUT303 =
OUT304 =
OUT305 =
OUT306 =
OUT307 =
OUT308 =
OUT309 =
OUT310 =
OUT311 =
OUT312 =
OUT313 =
OUT314 =
OUT315 =
OUT316 =

Display Point Elements (SELOGIC Control Equations)

DP1 =
DP2 =
DP3 =
DP4 =
DP5 =
DP6 =
DP7 =
DP8 =
DP9 =
DP10 =
DP11 =
DP12 =
DP13 =
DP14 =
DP15 =
DP16 =

Global Settings (SET G Command)

Inputs (SELOGIC Control Equations)

Selector Switch One and Two Settings (SELOGIC control equations)

SS1 = _____

SS2 = _____

A-, B-, C-Phase and Three-Pole Trip Signals (SELOGIC control equations)

TRIPA = _____

TRIPB = _____

TRIPC = _____

TRIP3 = _____

A-, B-, C-Phase Breaker Status and Motor-Operated Disconnect Status (SELOGIC control equations)

52AA = _____

52AB = _____

52AC = _____

MODST = _____

Automatic and Manual Breaker Close Signal (SELOGIC control equations)

CLOSE = _____

MCLOSE = _____

Dielectric Pressure Level Indicators (SELOGIC control equations)

LOD1 = _____

LOD2 = _____

LODCT = _____

Relay Settings

Description	Range			
Event Report Length	15, 30, 60 cycles	**LER**	=	_____
Pre-Event Length	1 to 14 when LER = 15 1 to 29 when LER = 30 1 to 59 when LER = 60	**PRE**	=	_____
Nominal Frequency	50, 60 Hz	**NFREQ**	=	_____
Phase Rotation	ABC, ACB	**PHROT**	=	_____
Format for Date	MDY, YMD	**DATE_F**	=	_____
Front-Panel Timeout	0–30 minutes in 1-min steps	**FP_TIMEOUT**	=	_____
Group Change Delay	0–900 seconds in 1-sec steps	**TGR**	=	_____

Global Settings (SET G Command) (cont.)

Breaker Monitor Settings (Only available in SEL-352-2 Relay)

Description				
Enable Breaker Contact Wear Monitoring	Y, N	**EBCW**	=	_____
Close/Open Set Point 1	1–65000 in steps of 1	**COSP1**	=	_____
Close/Open Set Point 2	1–65000 in steps of 1	**COSP2**	=	_____
Close Open Set Point 3	1–65000 in steps of 1	**COSP3**	=	_____
kA Interrupt Set Point 1	0.1–999.0 kA in 0.1-kA steps	**KASP1**	=	_____
kA Interrupt Set Point 2	0.1–999.0 kA in 0.1-kA steps	**KASP2**	=	_____
kA Interrupt Set Point 3	0.1–999.0 kA in 0.1-kA steps	**KASP3**	=	_____

Port Settings (SET P Command)

Port Description				485	232	232	232
Port Number		**Port #**		**1**	**2**	**3**	**4**
Description	**Range**	**Setting**					
Serial Port Protocol	SEL, LMD, DNP	**PROTO**	=	_____	_____	_____	_____
If PROTO = SEL							
Serial Port Baud Rate	300, 1200, 2400, 4800, 9600, 19200, 38400	**SPEED**	=	_____	_____	_____	_____
Serial Port Data Bits	7, 8	**D_BITS**	=	_____	_____	_____	_____
Serial Port Parity	N, E, O	**PARITY**	=	_____	_____	_____	_____
Serial Port Stop Bits	1, 2	**STOP**	=	_____	_____	_____	_____
Serial Port Timeout	0–30 min	**TIMEOUT**	=	_____	_____	_____	_____
Send Auto Message to Port	Y, N	**AUTO**	=	_____	_____	_____	_____
Enable Hardware Handshaking	Y, N	**RTS_CTS**	=	_____	_____	_____	_____
Fast Operate Enable	Y, N	**FAST_OP**	=	_____	_____	_____	_____
If PROTO = LMD							
Serial Port Address Prefix	#, $, %, &, @	**PREFIX**	=	_____	_____	_____	_____
Serial Port Address	1–99	**ADDRESS**	=	_____	_____	_____	_____
Serial Port Settling Time	0–30 sec	**SETTLE**	=	_____	_____	_____	_____
Serial Port Baud Rate	300, 1200, 2400, 4800, 9600, 19200, 38400	**SPEED**	=	_____	_____	_____	_____
Serial Port Data Bits	7, 8	**D_BITS**	=	_____	_____	_____	_____
Serial Port Parity	N, E, O	**PARITY**	=	_____	_____	_____	_____
Serial Port Stop Bits	1, 2	**STOP**	=	_____	_____	_____	_____
Serial Port Timeout	0–30 min	**TIMEOUT**	=	_____	_____	_____	_____
Send Auto Message to Port	Y, N	**AUTO**	=	_____	_____	_____	_____
Fast Operate Enable	Y, N	**FAST_OP**	=	_____	_____	_____	_____

Port Settings (SET P Command) (cont.)

Port Description			485	232	232	232
Port Number		**Port #**	**1**	**2**	**3**	**4**
If PROTO = DNP (SEL-352-2 Relay only)						
Serial Port Baud Rate	300, 1200, 2400, 4800, 9600, 19200, 38400	**SPEED =**	_____	_____	_____	_____
Serial Port Data Bits	7, 8	**D_BITS =**	_____	_____	_____	_____
Serial Port Parity	N, E, O	**PARITY =**	_____	_____	_____	_____
Serial Port Stop Bits	1, 2	**STOP =**	_____	_____	_____	_____
Serial Port Timeout	0–30 min	**TIMEOUT =**	_____	_____	_____	_____
DNP Address	0–65534	**DNPADR =**	_____	_____	_____	_____
Modem Connected?	Y, N	**MODEM =**	_____	_____	_____	_____
Modem Startup String	30 chars.	**MSTR =**	_____	_____	_____	_____
Phone Number	30 chars.	**PH_NUM =**	_____	_____	_____	_____
Dial-Out Time	5–300 sec	**MDTIME =**	_____	_____	_____	_____
Time Between Dial-Out Attempts	5–3600 sec	**MDRETI =**	_____	_____	_____	_____
Number of Dial-Out Attempts	0–5	**MDRETN =**	_____	_____	_____	_____
Class for Analog Event Data	0–3	**ECLASSA =**	_____	_____	_____	_____
Class for Binary Event Data	0–3	**ECLASSB =**	_____	_____	_____	_____
Class for Counter Event Data	0–3	**ECLASSC =**	_____	_____	_____	_____
Currents Scaling Decimal Places	0–3	**DECPLA =**	_____	_____	_____	_____
Voltage Scaling Decimal Places	0–3	**DECPLV =**	_____	_____	_____	_____
Misc. Scaling Decimal Places	0–3	**DECPLM =**	_____	_____	_____	_____
Timeset Request Interval	0–32767 min	**TIMERQ =**	_____	_____	_____	_____
Select/Operate Time-out	0.0–30.0 sec	**STIMEO =**	_____	_____	_____	_____
Data Link Time-out	0.0–5.0 sec	**DTIMEO =**	_____	_____	_____	_____
Minimum Time from DCD to Tx	0.00–1.00 sec	**MINDLY =**	_____	_____	_____	_____
Maximum Time from DCD to Tx	0.00–1.00 sec	**MAXDLY =**	_____	_____	_____	_____
Time from RTS ON to Tx OFF	OFF, 0.00–30.00 sec	**PREDLY =**	_____	_____	_____	_____

Port Settings (SET P Command) (cont.)

Port Description			485	232	232	232
Port Number		**Port #**	**1**	**2**	**3**	**4**
Time from Tx to RTS OFF	0.00–30.00 sec	**PSTDLY =**	_____	_____	_____	_____
Analog Deadband for Currents	0–32767 counts	**ANADBA =**	_____	_____	_____	_____
Analog Deadband for Voltages	0–32767 counts	**ANADBV =**	_____	_____	_____	_____
Analog Deadband Miscellaneous	0–32767 counts	**ANADBM =**	_____	_____	_____	_____
Event Data Confirmation Time-Out	0.1–50.0 sec	**ETIMEO =**	_____	_____	_____	_____
Data Link Retries	0–15	**DRETRY =**	_____	_____	_____	_____
Enable Unsolicited Reporting	Y, N	**UNSOL =**	_____	_____	_____	_____
Enable Unsolicited Reporting at Power up	Y, N	**PUNSOL =**	_____	_____	_____	_____
DNP Address to Report to	0–65534	**REPADR =**	_____	_____	_____	_____
Number of Events to Transmit on	1–200	**NUMEVE =**	_____	_____	_____	_____
Age of Oldest Event to Tx on	0–60 sec	**AGEEVE =**	_____	_____	_____	_____

Text Settings (SET T Command)

Local Bits

The following settings determine the text string labels the relay front panel displays for each of the 16 Local Bits. Labels correspond to the Local Bit name and to the clear, set, or pulse condition of each Local Bit. Text strings may contain any printing character (A–Z, 0–9, space, ., etc.), but they cannot start with ^, <, or >. Labels are subject to the specified character limit. Enter NA to null a display text label. Setting conventions are as follows:

NLB*n* = Name of Local Bit*n* (14 characters maximum)	SLB*n* = Set Local Bit*n* (7 characters maximum)
CLB*n* = Clear Local Bit*n* (7 characters maximum)	PLB*n* = Pulse Local Bit*n* (7 characters maximum)

NLB1 =		**NLB9 =**	
CLB1 =		**CLB9 =**	
SLB1 =		**SLB9 =**	
PLB1 =		**PLB9 =**	
NLB2 =		**NLB10 =**	
CLB2 =		**CLB10 =**	
SLB2 =		**SLB10 =**	
PLB2 =		**PLB10 =**	
NLB3 =		**NLB11 =**	
CLB3 =		**CLB11 =**	
SLB3 =		**SLB11 =**	
PLB3 =		**PLB11 =**	
NLB4 =		**NLB12 =**	
CLB4 =		**CLB12 =**	
SLB4 =		**SLB12 =**	
PLB4 =		**PLB12 =**	
NLB5 =		**NLB13 =**	
CLB5 =		**CLB13 =**	
SLB5 =		**SLB13 =**	
PLB5 =		**PLB13 =**	
NLB6 =		**NLB14 =**	
CLB6 =		**CLB14 =**	
SLB6 =		**SLB14 =**	
PLB6 =		**PLB14 =**	
NLB7 =		**NLB15 =**	
CLB7 =		**CLB15 =**	
SLB7 =		**SLB15 =**	
PLB7 =		**PLB15 =**	
NLB8 =		**NLB16 =**	
CLB8 =		**CLB16 =**	
SLB8 =		**SLB16 =**	
PLB8 =		**PLB16 =**	

Text Settings (SET T Command) (cont.)

Display Point Set and Clear Labels

The following settings determine text string labels the relay front panel displays for each of the 16 Display Points when they are in either the set (logical 1) or clear (logical 0) position. *Example*: DP*n*_1 = text displayed when display point is in the set (logical 1) position. DP*n*_0 = text displayed when display point is in the clear (logical 0) position. Text strings may contain any printing character (A–Z, 0–9, space, . , etc.), but they cannot start with ^, <, or >. Each label may contain as many as 16 characters. Enter NA to null a setting.

DP1_1 =		**DP9_1 =**	
DP1_0 =		**DP9_0 =**	
DP2_1 =		**DP10_1 =**	
DP2_0 =		**DP10_0 =**	
DP3_1 =		**DP11_1 =**	
DP3_0 =		**DP11_0 =**	
DP4_1 =		**DP12_1 =**	
DP4_0 =		**DP12_0 =**	
DP5_1 =		**DP13_1 =**	
DP5_0 =		**DP13_0 =**	
DP6_1 =		**DP14_1 =**	
DP6_0 =		**DP14_0 =**	
DP7_1 =		**DP15_1 =**	
DP7_0 =		**DP15_0 =**	
DP8_1 =		**DP16_1 =**	
DP8_0 =		**DP16_0 =**	

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SECTION 8: SERIAL PORT COMMUNICATIONS AND COMMANDS

INTRODUCTION

The SEL-352 Relay is equipped with four serial ports: one EIA-232 port on the front, two EIA-232 ports on the rear, and one EIA-485 port on the rear. Establish communication by connecting a terminal to one of the serial ports with the appropriate cable. Connect computers, modems, protocol converters, printers, an SEL-2020 or an SEL-2030 Communications Processor, an SEL-2885, a SCADA serial port, and/or RTUs for local or remote communications.

Use one of the SEL protocols for communication. The SEL ASCII commands and structure are defined in detail in this section. Other SEL protocols used for interfacing other intelligent electronic devices for automated communication are described in detail in the appendices.

ESTABLISH COMMUNICATION

Establish communication with the SEL-352 Relay through one of its serial ports by using standard "off-the-shelf" software and the appropriate cable connections, depending on the device.

Software

Use any system that emulates a standard terminal system. Such PC-based terminal emulation programs include: Procomm® Plus, Relay/Gold, Microsoft® Windows® Terminal, Microsoft® Windows® 95 HyperTerminal, SmartCOM, and CROSSTALK®. Many terminal emulation programs will work with the SEL-352 Relay. For the best display, use VT-100 terminal emulation or the closest variation.

The default communication settings for the serial ports follow:

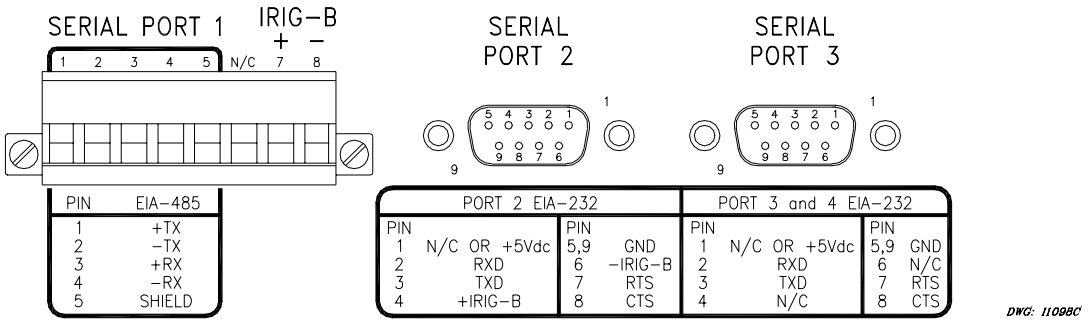
Baud Rate = 2400
Data Bits = 8
Parity = N
Stop Bits = 1
RTS/CTS = N

Change the port settings using the front panel or the **SET P <ENTER>** command.

Cables

Connect the SEL-352 Relay to another device using the appropriate cable. The pin definitions for Port 1, 2, 3, and 4 are given on the relay rear panel and detailed in Table 8.1.

A drawing of the 9-pin port connector and pin definitions appears in Figure 8.1.



(female chassis connectors as viewed from outside panel)

Figure 8.1: SEL-352 Relay Serial Port Connectors

Pinouts for EIA-232 and EIA-485 ports follow:

Table 8.1: Serial Port Pin Definitions

Pin Number	Port 1 Rear EIA-485	Port 2 Rear EIA-232 with IRIG-B	Port 3 Rear EIA-232	Port 4 Front EIA-232
1	+TX (Out)	N/C or +5Vdc*	N/C or +5Vdc*	N/C
2	–TX (Out)	RXD (In)	RXD (In)	RXD (In)
3	+RX (In)	TXD (Out)	TXD (Out)	TXD (Out)
4	–RX (In)	N/C or +IRIG-B*	N/C	N/C
5	Shield	GND	GND	GND
6	N/C	N/C or –IRIG-B*	N/C	N/C
7	+IRIG-B	RTS (Out)	RTS (Out)	RTS (Out)
8	–IRIG-B	CTS (In)	CTS (In)	CTS (In)
9	NA	GND	GND	GND

* Install a jumper to use the 5 V connection, and remove a solder jumper to disable the IRIG-B input. See ***Serial Port Jumpers*** in ***Section 2: Installation*** for more information.

Port 1 is an EIA-485 protocol connection on the rear of the relay. It accepts a plug in/plug out terminal block that supports wire sizes from 24 AWG up to 12 AWG. The connector is supplied with the relay. Ports 2, 3, and 4 are EIA-232 protocol connections with Ports 2 and 3 on the rear of the relay and Port 4 on the front of the relay. These female connectors are 9-pin D-subminiature connectors. Any combination of these ports or all of them may be used for relay communication. Table 8.2 gives a list of cables that can be purchased from SEL for various communication applications.

Table 8.2: SEL-352 Relay Communications Cable Numbers

SEL-352 Port #	Connect to Device (gender refers to device)	SEL Cable #
2, 3, 4	PC, 25-Pin Male (DTE)	C227A
2, 3, 4	Laptop PC, 9-Pin Male (DTE)	C234A
2, 3	SEL-2020 or SEL-2030 without IRIG-B	C272A
2	SEL-2020 or SEL-2030 with IRIG-B	C273A
2	SEL-IDM, Ports 2 through 11	Requires a C254 and C257 cable.
2, 3	Modem, 5 Vdc Powered (Pin 10)	C220*
2, 3	Standard Modem, 25-Pin Female (DCE)	C222

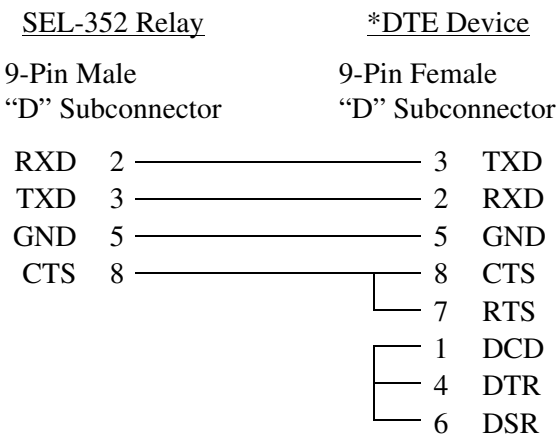
* The 5 Vdc serial port jumper must be installed to power the modem using C220. See ***Serial Port Jumpers*** in ***Section 2: Installation***.

For example, to connect the SEL-352 Relay Port 2, 3, or 4 to the 9-pin male connector on a laptop, order cable number C234A, and specify the length needed. To connect the SEL-352 Relay Port 2 to the SEL-2020/SEL-2030 Communications Processor that supplies the communications link and the time synchronization signal, order cable number C273A, and specify the length needed. For connecting devices at over 100 feet, fiber-optic transceivers are available. The SEL-2800 and SEL-2810 provide fiber-optic links between devices for electrical isolation and long distance signal transmission. Call the factory for further information on these products.

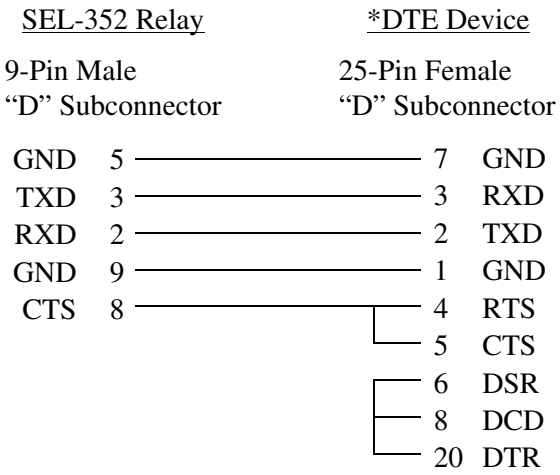
The following cable diagrams show several types of EIA-232 serial communications cables. These and other cables are available from SEL. Contact the factory for more information.

SEL-352 Relay to Computer

Cable C234A

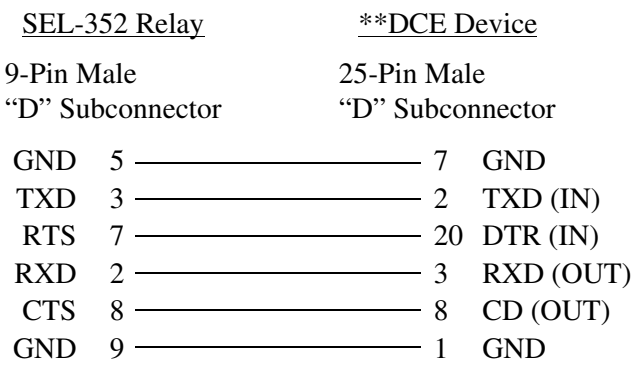


Cable C227A



SEL-352 Relay to Modem

Cable C222



Cable C220

SEL-352 Relay			Modem 5 Vdc Powered **DCE Device	
9-Pin Male "D" Subconnector			25-Pin Male "D" Subconnector	
GND	5	———	7	GND
TXD	3	———	2	TXD (IN)
RTS	7	———	20	DTR (IN)
RXD	2	———	3	RXD (OUT)
CTS	8	———	8	CD (OUT)
+5 VDC	1	———	10	PWR (IN)
GND	9	———	1	GND

SEL-352 Relay to SEL-2020 or SEL-2030

Cable 272A

SEL-2020 or SEL-2030			SEL-352 Relay	
9-Pin Male "D" Subconnector			9-Pin Male "D" Subconnector	
RXD	2	———	3	TXD
TXD	3	———	2	RXD
GND	5	———	5	GND
RTS	7	⌐	7	RTS
CTS	8	⌙	8	CTS

Cable 273A

SEL-2020 or SEL-2030			SEL-352 Relay	
9-Pin Male "D" Subconnector			9-Pin Male "D" Subconnector	
RXD	2	———	3	TXD
TXD	3	———	2	RXD
IRIG+	4	———	4	IRIG+
GND	5	———	5	GND
IRIG-	6	———	6	IRIG-
RTS	7	———	8	CTS
CTS	8	———	7	RTS

* DTE= Data Terminal Equipment (Computer, Terminal, Printer, etc.)
** DCE = Data Communications Equipment (Modem, etc.)

Table 8.3: Serial Communications Port Pin Function Definitions

Pin Function	Definition
N/C	No Connection
+5 V dc	5 V dc Power Connection
RXD, RX	Receive Data
TXD, TX	Transmit Data
IRIG-B	IRIG-B Time-Code Input
GND	Ground
SHIELD	Shielded Ground
RTS	Request to Send
CTS	Clear to Send
DCD	Data Carrier Detect
DTR	Data Terminal Ready
DSR	Data Set Ready

COMMUNICATIONS PROTOCOL

This section explains the serial port communications protocol used by the SEL-352 Relay. You set and operate the SEL-352 Relay via the serial communications ports.

Note: In this document, commands you type appear in bold/upper case: **SET**. Keys you press appear in bold/upper case/brackets: **<ENTER>**.

Relay output appears boxed and in the following format:

```
EXAMPLE: BUS B, BREAKER 3     Date: 02/01/93    Time: 00:03:25.180
```

The communications protocol consists of hardware and software features.

Hardware Protocol

The following hardware protocol is designed for manual and automatic communications.

1. If the SET P setting “RTS_CTS” = N, RTS will always be asserted.
2. If the SET P setting “RTS_CTS” = Y, RTS asserts while the communications buffer is less than 87 percent full, and RTS deasserts when the communications port buffer is greater than 87 percent full.
3. If the SET P setting “RTS_CTS” = Y, the relay does not send characters until the CTS input is asserted.

Software Protocol

Software protocols consist of standard SEL ASCII, SEL Distributed Port Switch (LMD), SEL Distributed Network Protocol (DNP) (SEL-352-2 Relay only), SEL *Fast Meter*, SEL *Fast Operate*, and SEL Compressed ASCII. Based on the port PROTOCOL setting, the relay activates SEL ASCII, SEL LMD, or SEL DNP protocol. SEL *Fast Meter* and SEL Compressed ASCII commands are always active.

SEL ASCII

The following software protocol is designed for manual and automatic communications.

1. All commands received by the relay must be of the form:

   <command><CR> or <command><CR><LF>

   A command transmitted to the relay should consist of the following:

   - A command followed by either a carriage return or a carriage return and line feed.
   - You must separate arguments from the command by spaces, commas, semicolons, colons, or slashes.
   - You may truncate commands to the first three characters. **EVENT 1 <ENTER>** would become **EVE 1 <ENTER>**.
   - Upper- and lower-case characters may be used without distinction, except in passwords.

2. The relay transmits all messages in the following format:

   <STX><CR><LF>
   <MESSAGE LINE 1><CR><LF>
   <MESSAGE LINE 2><CR><LF>
   .
   .
   <LAST MESSAGE LINE><CR><LF>
   <ETX> <PROMPT>

   Each message begins with the start-of-transmission character STX (ASCII character 02) and ends with the end-of-transmission character ETX (ASCII character 03).

3. The relay indicates how full its receive buffer is through an XON/XOFF protocol.

   The relay transmits XON (ASCII hex 11) when the buffer drops below 40 percent full.

   The relay transmits XOFF (ASCII hex 13) when the buffer is over 80 percent full. Automatic transmission sources should monitor for the XOFF character so they do not overwrite the buffer. Transmission should terminate at the end of the message in progress when XOFF is received and may resume when the relay sends XON.

4. You can use an XON/XOFF procedure to control the relay during data transmission. When the relay receives an **XOFF** command during transmission, it pauses until it receives an **XON** command. If there is no message in progress when the relay receives an **XOFF** command, it blocks transmission of any message presented to its buffer.

The CAN character (ASCII hex 18) aborts a pending transmission. This is useful in terminating an unwanted transmission.

5. Control characters can be sent from most keyboards with the following keystrokes:

XON:	**<CTRL>Q**	(hold down the Control key and press Q)
XOFF:	**<CTRL>S**	(hold down the Control key and press S)
CAN:	**<CTRL>X**	(hold down the Control key and press X)

SEL Distributed Port Switch Protocol

The SEL Distributed Port Switch Protocol (LMD) permits multiple SEL relays to share a common communications channel. The protocol is selected by setting the SET P setting PROTOCOL = LMD. See ***Appendix C: SEL Distributed Port Switch Protocol (LMD)*** for more information on Distributed Port Switch Protocol (LMD).

SEL Distributed Network Protocol (SEL-352-2 Relay Only)

SEL Distributed Network Protocol (DNP) meets DNP 3.00 Level 2 requirements. Select the protocol by setting **PROTOCOL = DNP**, a SET P setting. See ***Appendix G: Distributed Network Protocol (DNP) 3.00*** for more information.

SEL *Fast Meter* Protocol

SEL *Fast Meter* protocol supports binary messages to transfer metering messages. SEL *Fast Meter* protocol is always available on any serial port. The protocol is described in ***Appendix D: Configuration, Fast Meter, and Fast Operate Commands***.

SEL *Fast Operate* Protocol

SEL *Fast Operate* protocol supports binary messages to control Relay Word bits. SEL *Fast Operate* protocol is available on any serial port. It may be turned off by setting the SET P setting FAST_OP=N. The protocol is described in ***Appendix D: Configuration, Fast Meter, and Fast Operate Commands***.

SEL Compressed ASCII Protocol

SEL Compressed ASCII protocol provides compressed versions of some of the relay ASCII commands. SEL Compressed ASCII protocol is always available on any serial port. The protocol is described in ***Appendix E: Compressed ASCII Commands***.

SEL ASCII PROTOCOL DETAILS

Automatic Messages

The SEL-352 Relay generates automatic messages and sends them out the serial port(s) with the SET P setting AUTO = Y. Four different automatic messages can be displayed:

- Relay startup message
- Setting group change message
- Relay self-test warning or failure
- Event summary message

Startup Message

Immediately after power is applied, the relay transmits the following automatic message:

```
EXAMPLE CIRCUIT BREAKER              Date: 11/09/96    Time: 13:17:39.122
SEL-352-1
=
```

Group Switch Message

The SEL-352 Relay has three different setting groups for the SET settings. The active group is selected by the group variable or the SS1 and SS2 bits. When either of these change the active group, the following automatic message is generated.

```
EXAMPLE CIRCUIT BREAKER              Date: 11/09/96    Time: 13:39:07.560

Active Group = 2
Group Variable = 1

=>>
```

- TRMID setting for the new active group
- Date and time of group change
- Active setting group now being used
- Group variable last set by the **GRO** command (the SET G settings SS1 and SS2 take precedence over the **GRO** command)

Status Report

The relay automatically generates a status report whenever the self-tests declare a failure state and some warning states. Refer to ***Self-Testing Alarms*** in ***Section 6: Metering and Monitoring*** for a summary table of the self-tests. ***Section 6*** provides a complete description of the status report.

```
EXAMPLE CIRCUIT BREAKER              Date: 11/09/96    Time: 14:09:49.628

FID=SEL-352-1-R100-V-D961030
SELF TESTS

W=Warn    F=Fail

       IA       IB       IC       VAX      VBX      VCX
OS      0       -0        0        0        0        0

       VAY      VBY      VCY      MOF
OS      0        0       -0        1

       +5V_PS   +5V_REG  -5V_REG  +12V_PS  -12V_PS  +15V_PS  -15V_PS
PS     4.92     5.01     -5.00     12.09   -12.21    14.92   -14.92

       TEMP     RAM      ROM      A/D      CR_RAM   EEPROM   IO_BRD
        32.7    OK       OK       OK       OK       OK       OK

Relay Enabled

=>>
```

- TRMID setting for the new active group
- Date and time the failure or warning was detected
- Firmware identification string
- Individual self-test results
- Relay protection enabled or disabled indication

Summary Event Report

An automatic message is generated each time an event is triggered. The message is a summary of the event.

```
EXAMPLE CIRCUIT BREAKER              Date: 11/09/96    Time: 14:23:41.758

Event: INT        Frequency (Hz):  60.0

=>>
```

- TRMID setting
- Date and time the event was triggered
- The event type
- Frequency the sampling rate of the relay was tracking to at the time of trigger

Access Levels

Commands can be issued to the relay via the serial port to view metering values, change relay settings, etc. The available ASCII serial port commands are listed in Figure 8.2 and the ***Command Summary*** at the end of this section. (The ***Command Summary*** also can be found in the ***Quick Reference*** section at the end of this instruction manual.) The commands can be accessed only from the corresponding access level as shown in Figure 8.2 and the ***Command Summary***. The four access levels are:

- Access Level 0 (the lowest access level)
- Access Level 1
- Access Level B
- Access Level 2 (the highest access level)

A multilevel password system provides security against unauthorized access. This access scheme allows you to give personnel access to only those functions they require.

Each level has an associated screen prompt and password. Figure 8.2 shows the access levels, passwords, prompts, commands available from each access level, and commands that move you between access levels.

Access Level 0

Once serial port communications are established with the relay, the following prompt appears:

```
=
```

If a different prompt appears, the relay was left in a different access level or the terminal emulation you are using is translating the characters differently. VT-100 emulation is recommended.

This prompt is referred to as Access Level 0. The only commands that can be executed at Access Level 0 are the **ACC** and **QUI** commands (see Figure 8.2). Enter the **ACC** command at the Access Level 0 prompt to go to Access Level 1.

Access Level 1

After issuing the **ACC** command and entering the Level 1 password, if it is required (see ***PAS (Passwords)*** for factory default passwords), the relay is in Access Level 1. The following prompt appears when in Access Level 1:

```
=>
```

Many commands can be executed from Access Level 1 for viewing relay information. The **2AC** command allows the relay to go to Access Level 2. The **BAC** command allows the relay to go to Access Level B.

Access Level B (Breaker Level)

After issuing the **BAC** command and entering the password if it is required, the relay pulses the alarm contact and is in Access Level B (breaker access level). The following prompt appears when in Access Level B:

```
==>
```

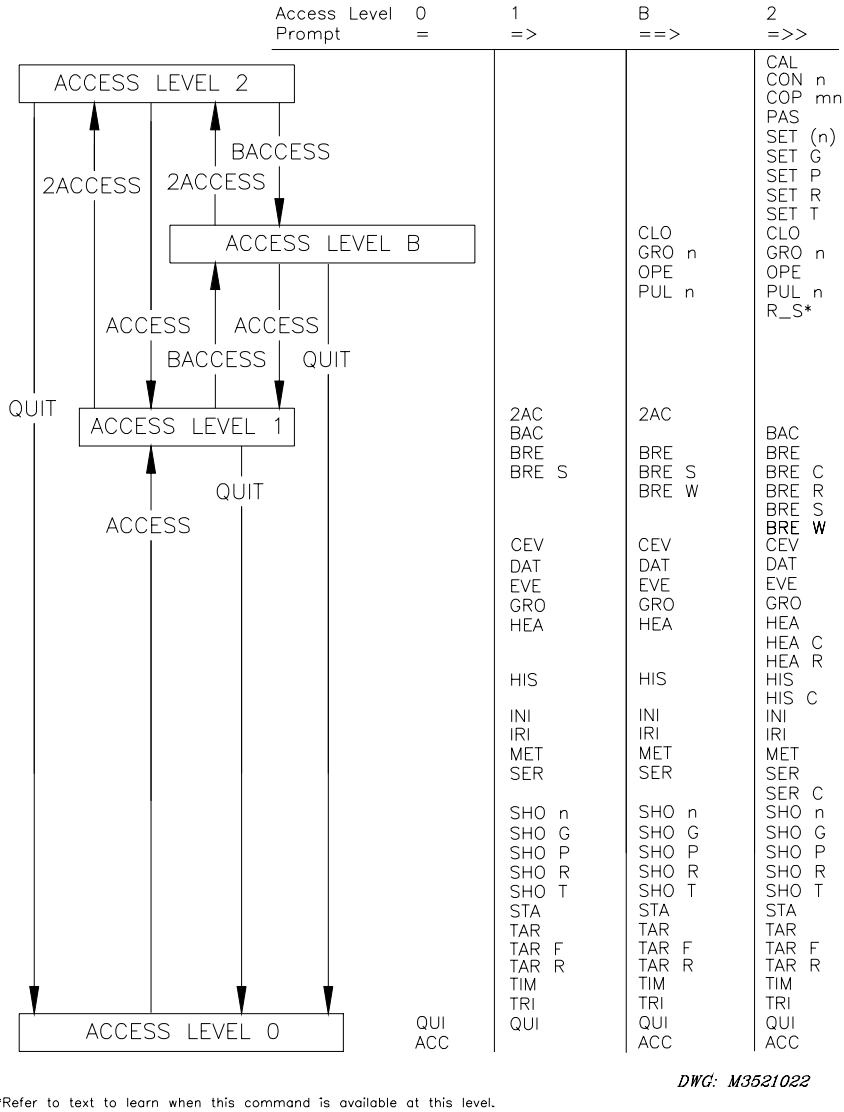
Many commands can be executed from Access Level 2 for viewing relay information, and controlling the breaker. While in Access Level B, any of the commands available in the lower access levels can be executed.

Access Level 2

After issuing the **2AC** command and entering the password, if it is required, the relay pulses the alarm contact and is in Access Level 2. The following prompt appears when in Access Level 2:

```
=>>
```

Many commands can be executed from Access Level 2 for viewing relay information, controlling the breaker, and changing settings. While in Access Level 2, any of the commands available in the lower access levels can be executed.



*Refer to text to learn when this command is available at this level.

Figure 8.2: Access Level Relationships

Command Definitions

SEL ASCII commands require three characters and some commands require certain parameters. Each command is defined in alphabetical order. The previous two pages give a summary of most of the commands and optional parameters. Examples are shown for each command following its definition. Text you type appears in bold, and keyboard keys you push appear in bold with brackets. For example, to enter Access Level 1 from Access Level 0 type **ACC<ENTER>**.

2AC (Access Level 2)

Access Level 1

Use the **2ACCESS** command to enter Access Level 2. The default password for Level 2 is shown under ***PAS (Passwords)*** later in this section. Use the **PASSWORD** command from Access Level 2 to change passwords. Install main board jumper JMP6A to disable password protection.

The following display indicates successful access to Level 2:

```
=>2AC<ENTER>
Password: ? @@@@@@

EXAMPLE CIRCUIT BREAKER              Date: 11/09/96    Time: 14:23:41.758

Level 2
=>>
```

You may use any command from the "=>>" prompt. The relay pulses the ALARM contact for one second after any Level 2 access attempt, unless an alarm condition already exists.

ACC (Access Level 1)

Access Level 0

Use the **ACCESS** command to enter Access Level 1. The default password for Level 1 is shown under ***PAS (Passwords)*** later in this section. Use the **PASSWORD** command from Access Level 2 to change passwords. Install main board jumper JMP6A to disable password protection.

The following display indicates successful access to Level 1:

```
=ACC<ENTER>
Password: ? @@@@@@

EXAMPLE CIRCUIT BREAKER              Date: 11/09/96    Time: 14:23:41.758

Level 1
=>
```

BAC (Breaker Access Level)

Access Level 1

Use the **BACCESS** command to enter breaker Access Level B. The default password for Level B is shown under ***PAS (Passwords)*** later in this section. Use the **PASSWORD** command from Access Level 2 to change this password. Install main board jumper JMP6A to disable password protection.

The following display indicates successful access to Level B:

```
=>BAC<ENTER>
Password: ?  @@@@@@

EXAMPLE CIRCUIT BREAKER              Date: 11/11/96    Time: 14:04:51.251

Breaker Level
==>
```

The relay pulses the ALARM contact closed for one second after any Level B access attempt, unless an alarm condition already exists.

BRE (Breaker Report)

Access Level 1

Use the **BREAKER** command to display a report of breaker operation information. The breaker monitor report gives electrical and mechanical operating times, total energy dissipated, and maximum current interrupted for the last 512 operations on a per-pole basis, and a summary of all of this information. The summary of the operations and breaker alarms provides valuable breaker diagnostic information at a glance. An example breaker report follows, but it would also include the summary shown under the **BRE S** command. Refer to ***Breaker Monitor*** in ***Section 6: Metering and Monitoring*** for further information and a complete explanation of the report.

```
=>>BRE<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 02/17/96    Time: 04:02:08.509

FID=SEL-352-1-R100-D960112

                                BREAKER OPERATIONS


#      DATE         TIME        OPERATION  OP. TIME (ms)   ENERGY  CURRENT
                                           ELECT.  MECH.     (MJ)     (A)
1    09/26/96   16:24:37.401   TRIPA        29      16      0.03     5472
2    09/26/96   16:24:37.401   TRIPB        29      16      0.01     5454
3    09/26/96   16:24:37.401   TRIPC        29      16      0.01     5457
4    09/26/96   16:22:03.651   CCA          8       12      0.02     1248
5    09/26/96   16:22:03.651   CCB          8       12      0.01     1239
6    09/26/96   16:22:03.651   CCC          10      12      0.00     1236
```

BRE C (Clear Breaker Report)

Access Level 2

Reset the breaker operations, operation summary, and breaker alarm counters by clearing the report with the **BRE C** or **BRE R** command. **BRE R** is only available in the SEL-352-2 Relay.

```
=>>BREAKER C<ENTER>

Reset/Clear Breaker Monitor Data
Are you sure (Y/N) ?

=>>
```

CAUTION

Automated clearing of the breaker report should be limited to reduce the possibility of wearing out the nonvolatile memory. Limit automated **BRE C** commands to once per week or less.

BRE S (Breaker Report Summary)

Access Level 1

Use the **BREAKER S** command to view only the breaker operation summary and the breaker alarms. This provides the average breaker operation times and the time for the last operation. Compare these two values to determine if the breaker is slowing down and requires maintenance. Refer to ***Section 6: Metering and Monitoring***, ***Breaker Monitor*** for more information and a complete description of the report. Percent wear is only available in the SEL-352-2 Relay.

```
=>BRE S<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 02/17/21    Time: 04:02:08.509

FID=SEL-352-2-R100-D960112
                                OPERATION SUMMARY

                        TRIPA   TRIPB   TRIPC   CLOSEA  CLOSEB  CLOSEC

Number of Operations    1       1       1       1       1       1

Ave. Elect. Time (ms)   29.0    29.0    29.0    8.0     8.0     10.0
Ave. Mech. Time  (ms)   16.0    16.0    16.0    12.0    12.0    12.0

Last Elect. Time (ms)   29      29      29      8       8       10.0
Last Mech. Time  (ms)   16      16      16      12      12      12

Total Energy  (MJ)       0.03    0.01    0.01    0.02    0.01    0.00
Total Current (A)       5472    5454    5457    1248    1249    1236
Percent Wear  (%)       100     100     100

                                     (continued on next page)
```

```
                                (continued from previous page)

                                 BREAKER ALARMS

                                          ALARM    TOTAL COUNT

Failed CB Trip Resistors Put In Service    FTRS          0
Failed CB Close Resistors Put In Service   FCRS          0
52A Contradicts Voltage                    52ACV         1
Current While Open                         CWO           0
Trip While Open                            TWO           1
CB Did Not Close                           BDNC          0
Current After MOD Trip                     CAMT          0
MOD Contradicts Current                    MCC           0
Slow Trip                                  ST            0
Slow Close                                 SC            2
Potential Transformers Disagree            PTD           2

Last Breaker Monitor Reset: xx/xx/xx xx:xx:xx
=>>
```

BRE W (Preload Breaker Wear Data) (SEL-352-2 Relay)

Access Level B

Use the **BRE W** command to preload contact wear, trip and close operation counters, and trip and close current accumulators on a per-phase basis. This command is only available in the SEL-352-2 Relay.

```
         1         2         3         4         5         6         7         8
12345678901234567890123456789012345678901234567890123456789012345678901234567890
=>>BREAKER W<ENTER>

Preload Contact Wear, Operation Counters, and Accumulated Currents

Percent Wear (%)    TRIPA  =    5 ?
                    TRIPB  =   10 ?
                    TRIPC  =    7 ?

Num of Operations:  TRIPA  =   25 ?
                    TRIPB  =   30 ?
                    TRIPC  =   24 ?
                    CLOSEA =   25 ?
                    CLOSEB =   30 ?
                    CLOSEC =   24 ?

Total Current (A)   TRIPA  =  990 ?
                    TRIPB  =  980 ?
                    TRIPC  =  900 ?
                    CLOSEA =   30 ?
                    CLOSEB =   50 ?
                    CLOSEC =   98 ?

Total Energy (MJ)   TRIPA  = 5.10 ?
                    TRIPB  = 5.08 ?
                    TRIPC  = 5.00 ?
                    CLOSEA = 0.03 ?
                    CLOSEB = 0.05 ?
                    CLOSEC = 0.20 ?

                             Breaker Summary Report is displayed here

Are you sure (Y/N) ?

=>>
```

CAL (Calibration Access Level)

Access Level 2

The **CALIBRATION** command is used to enter the calibration access level in the relay. Normal relay operation does not require access to this level. The only user command that may be necessary to use from this level is the **R_S** command, which resets factory default settings. Do not access this level unless instructed by the factory or using the **R_S** command. The relay is calibrated at the factory and will not need field calibration. Contact the factory if you suspect the relay is not calibrated.

CEVE (Compressed Event)

Access Level 1

The SEL-5601 Analytic Assistant software is available for graphical analysis of event reports. The **CEVE** command is a compressed (no formatting) version of the **EVE** command. Use the **CEVE** command to download events for the SEL-5601 Analytic Assistant. Refer to ***Appendix E: Compressed ASCII Commands*** for a complete description of the command.

CLO (Close)

Access Level B

The **CLOSE** command asserts the CCMD bit if TRIPA, TRIPB, TRIPC, and TRIP3 are not all asserted. The CCMD bit remains asserted for 30 cycles, then the relay checks the status of the 52A input assignments to determine if the breaker is closed.

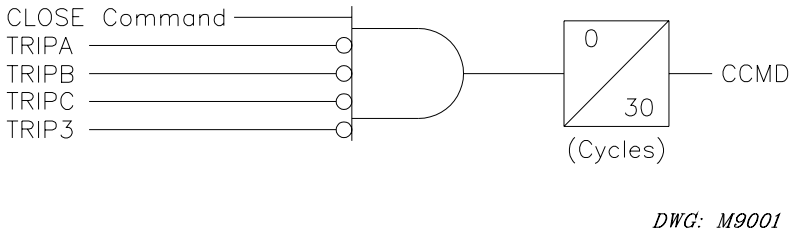


Figure 8.3: CCMD Relay Word Bit

If the breaker closes successfully based on the 52A indication at the end of the 30 cycles, the relay responds with "Breaker CLOSED." If the breaker does not close based on the 52A indication at the end of the 30 cycles, the relay responds with "Breaker OPEN."

The CCMD bit typically is used as part of the MCLOSE input assignment. If the **CLO** command is issued, the relay responds as if it had received a manual close input.

To close the circuit breaker with this command, type **CLOSE <ENTER>**. The prompting message "Close Breaker (Y/N) ?" is displayed. Then "Are you sure (Y/N)?" Typing **N <ENTER>** after either of the above prompts aborts the closing operation with the message "Command Aborted."

If the main board jumper JMP6B is not in place, the relay responds: "Aborted: Breaker Jumper Not in Place."

```
==>CLO<ENTER>
Close Breaker (Y/N) ? Y<ENTER>
Are you sure (Y/N) ? Y<ENTER>
Breaker CLOSED
==>
```

CON n (Control RBn)

Access Level 2

This command is used to control the Relay Word bit RBn, or Remote Bit n, n having a value of 1 to 16. The relay responds with CONTROL RBn. The user must then respond with one of the following: **SRB n<ENTER>** (Set Remote Bit n), or **CRB n<ENTER>** (Clear Remote Bit n), or **PRB n<ENTER>** (Pulse Remote Bit n). The latter asserts RBn for one processing interval, one-eighth cycle. The Remote Bits permit design of SELOGIC control equations that can be set, cleared, or momentarily activated via a remote serial-port command.

```
=>>CON 1<ENTER>
CONTROL RB1: PRB 1
=>>
```

COP m n (Copy Settings)

Access Level 2

The **COPY** command copies settings and logic from setting Group m to Group n (m and n can be any combination of 1, 2, or 3). After entering the settings into one setting group with the **SET** command, copy it to the other groups with the **COPY** command. Use the **SET** command to modify copied setting groups. The ALARM output contact closes momentarily when you change settings in an active setting group, but not in an inactive setting group.

```
=>>COP 1 3<ENTER>
COPY 1 to 3
Are you sure (Y/N) ? Y<ENTER>

Please wait...
Settings copied
=>>
```

DAT (Date)

Access Level 1

The **DATE** command displays or sets the date stored by the internal calendar/clock. Simply typing **DAT<ENTER>** displays the date. Set the date by typing **DATE d1<ENTER>** where d1 is either mm/dd/yy or yy/mm/dd depending on the SET G date format setting DATE_F. View the date from Access Level 1, but the date can only be changed from Access Level 2. The following example views the current date, verifies the DATE_F setting, and changes the date. Note that single digit numbers may be entered without leading zeros like the 9 in 11/9/96.

```
=>>DAT<ENTER>
11/11/96
=>>SHO G DATE_F<ENTER>

Relay Settings
DATE_F = MDY       FP_TIMEOUT= 5         TGR    = 5

=>>DAT 11/9/96<ENTER>
11/09/96
=>>
```

Note: After setting the date, allow at least 60 seconds before powering down the relay or the new setting may be lost.

EVE (Event Reports)

Access Level 1

The **EVENT** command displays an event report. Optional parameters are specified to determine the event displayed and its format. Refer to ***Event Reports*** in ***Section 10: Event Reports and SER*** for a complete description of the event reports.

The entire syntax of the **EVENT** command is as follows:

EVE n A Ss Lc

The parameters may be entered in any order following the three-letter command **EVE**, but must be separated by spaces or commas. The following is a summary of the parameters followed by some examples:

- n n specifies event number according to the **HIS** command.
- A A specifies the alternate report showing VY (not VX and I).
- Ss Ss specifies the samples per cycle (s = 4, 8, 16, 64).
- Lc Lc specifies the length in cycles (c = 1 to LER setting).

EVE (Defaults)	Display
	Most recent event (EVE 1)
	VX and I analogs, standard digitals
	4 samples per cycle
	All available cycles

EVE A 3 S8

Display
Event number 3
VY analogs, alternate digitals
8 samples per cycle
All available cycles

EVE S8 L5 10

Display
Event number 10
VX and I analogs, standard digitals
8 samples per cycle
First 5 cycles of the event

The n parameter specifies the event number to display based on the **HISTORY** command. The **HIS** command displays an event summary of all of the events stored in memory. Each summary is numbered. The number of event reports stored is dependent on the length of the events, which is determined by the SET G setting LER as follows:

LER Setting	Number of Event Reports Stored
15 cycles	40
30 cycles	20
60 cycles	10

To select one of the events stored in relay memory, enter the **EVENT** command with a number, with 1 being the newest event recorded. If no event report is selected, the relay defaults to n = 1 to display the newest event report. Type **EVE 9 <ENTER>** to display event number 9.

Include the A as a parameter to display the alternate Y-side voltages and an alternate set of digital channels. If the A is not specified, the standard X-side voltages and currents with the standard digitals are displayed.

Specify the number of samples per-cycle resolution of the event with the Ss parameter. The small s can be 4, 8, 16, or 64. If the Ss parameter is not specified, the relay defaults to S4. The relay stores the event with 64-samples-per-cycle resolution. When displaying the event, select the most appropriate resolution for your application. Some recommendations follow:

- Overview of relay operation: S4 (provides quickest display of general information)
- Diagnostics using digital channels: S8 (the digital channels are processed every eighth cycle)
- Best resolution for SEL-2020/SEL-2030 event storage: S16 (largest event size the SEL-2020/SEL2030 can store)
- Detailed analysis of analog channels: S64 (analog channels are sampled every 64th cycle)

To specify the length of the event displayed, use the Lc parameter. The c can be any integer from 1 to LER in cycles. If the LER is set to 30, then L30 is the largest value that may be entered. If the Lc parameter is not specified, the relay defaults to the LER setting. Any attempt to enter a length greater than the LER setting will produce an error.

Refer to ***Event Reports*** in ***Section 10: Event Reports and SER*** for example event reports and descriptions.

GRO (Setting Group)

Access Level 1 and 2

The **GROUP** command displays or designates the setting group variable. This variable (1–3) specifies which setting group is the active group when the setting group selection inputs (SS1, SS2) are not assigned or are deasserted. The following example verifies the existing group variable, changes it, and then waits for the automatic message when the setting group changes. The variable must be changed for a certain number of seconds as specified by the SET G setting TGR before the new settings are enabled.

```
=>>GRO<ENTER>

Active Group = 1
Group Variable = 1

=>>GRO 2<ENTER>
Change Group Variable:
Are you sure (Y/N) ? Y<ENTER>
=>>
```

The **GROUP** command does not clear the event report buffer. If the active group is changed, the relay pulses the ALARM output contacts and generates the following automatic message:

```
EXAMPLE: BUS B, BREAKER 3     Date: 02/01/93    Time: 23:31:17.489

Active Group = 2
Group Variable = 2

=>>
```

Note: The relay will be disabled momentarily while the group switch takes place.

The **GROUP** command at Access Level 1 shows the active group but does not allow changes. Access Level 2 allows the **GROUP** command to change the group variable.

HEA (Resistor Heat Report)

Access Level 1

The SEL-352 Relay tracks heat of the close and open resistor for each of the three phases. The **HEAT** command allows you to examine resistor status, presenting the heat content of each resistor (with respect to ambient) normalized to the resistor failure threshold, 26CF or 26TF. For example, if the B-phase open resistor (ORB) contains 1.0 J of internal heat, and the trip failure threshold (26TF) setting is 2.0 J, the **HEAT** command displays the ORB resistor heat as 0.50.

The **HEAT** command report headings use a simple format. **ORA** heads the A-phase opening resistor column, **CRA** the A-phase closing resistor column, and so on, for the B- and C-phases.

Automatically repeat the **HEAT** command by adding a repeat count. To repeat the command 1000 times, type **HEA 1000 <ENTER>**. The command **<CTRL>X** cancels the listing at any time. Repetition is especially useful when testing thermal elements.

```
=>HEAT 4 <ENTER>

RESISTOR HEAT IN PER UNIT TRIP VALUE

Example 500 kV Breaker                          Date: 6/1/96    Time: 10:16:04

ORA   CRA   ORB   CRB   ORC   CRC

0.00  0.00  0.31  0.11  0.00  0.00
0.00  0.00  0.31  0.11  0.00  0.00
0.00  0.00  0.30  0.11  0.00  0.00
0.00  0.00  0.30  0.11  0.00  0.00

=>
```

HEA C (Clear Resistor Heating)

Access Level 2

The **HEAT C** command clears the thermal models. Quickly reset the resistor heating to zero when testing the thermal elements by clearing them with the **HEA C** command.

```
=>HEA C<ENTER>
Reset Thermal Models
Are you sure (Y/N) ?Y<ENTER>
Resetting Complete

=>>
```

HIS (History of Events)

Access Level 1

The **HISTORY** command displays up to 40 event summaries depending on the SET G setting LER as follows:

LER Setting	Number of Event Reports Stored
15 cycles	40
30 cycles	20
60 cycles	10

Each summary shows the date, time, event type, active setting group, and relay targets.

Enter **HIS n**, where n is a positive number, to limit the history report to the most recent n events. The history is stored in nonvolatile memory, so it is retained through power failures.

The date and time is saved to the nearest millisecond and referenced to the trigger row of data in the event report.

An example of the display appears below. Note that in this example only seven events have occurred since the history was cleared:

```
=>HIS<ENTER>

Example 500 kV Breaker                              Date: 6/1/96    Time: 01:16:24

#       DATE        TIME       EVENT     GROUP


1     01/06/96  00:18:10.333  CLOSE        1
2     01/04/96  09:08:20.058  INT          1
3     01/04/96  08:53:55.429  TRIP3        1
4     01/01/96  00:18:10.258  CLOSE        1
5     01/01/96  00:18:08.095  TRIPA        1
6     12/09/95  22:41:33.108  CLOSE        1
7     12/09/95  22:27:47.870  TRIP3        1

=>
```

If an event has not occurred since the history was last cleared, the headings are displayed with the message: History Buffer Empty.

HIS C (Clear History and Events)

Access Level 2

The **HIS C** command clears the history and associated events from nonvolatile Flash memory. The clearing process may take up to 30 seconds under normal operation. It may be even longer if the relay is busy processing a fault or other protection logic. The following is an example of the **HIS C** command. The relay will pause after the word "Clearing" until the buffer is completely clear, and then it will display the rest of the information.

```
=>HIS C<ENTER>
Clear History Buffer
Are you sure (Y/N) ? Y<ENTER>
Clearing Complete                          Relay pauses after the word Clearing
=>
```

Automated clearing of the event buffer should be limited to reduce the possibility of wearing out the nonvolatile memory. Limit automated **HIS C** commands to once per week or less.

INI (Initialize I/O)

Access Level 1 and 2

The **INI** command reports the number and type of I/O boards in the relay from Access Level 1. If the number or type of I/O boards has changed since last power up, **INI** will confirm that the I/O boards now present are correct from Access Level 2. If the user answers yes, I/O settings will be changed unless any inputs or outputs that may be in SELOGIC® control equations have been removed. If so, a warning is issued and the relay confirms the change again with "Are you sure (Y/N) ?"

If an I/O board type is not supported, then “CALL FACTORY” will be printed, and the user will not be prompted for correctness. If there is no I/O board, “NO BOARD CONNECTED” will be printed. A “T” parameter passed in **INI** will cause the factory type number of the I/O board to be shown.

The following examples walk through the insertion of a new board and then the removal of another board:

Display Existing I/O

```
=>INI<ENTER>
I/O BOARD       INPUTS    OUTPUTS
Main              6         7
1                 8         16
2                 No Board Connected

=>
```

Power Cycled on Relay to Install I/O Board

```
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:47:57.123
SEL-352-1
=
```

Automatic Status Message Generated for Failed I/O Test (Entire status report not shown)

```
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:48:00.310
.
.
       TEMP     RAM      ROM      A/D      CR_RAM   EEPROM   IO_BRD
        27.5    OK       OK       OK       OK       OK       FAIL

Relay Disabled
```

Enter Access Level 1 (Password Jumper JMP6A Removed)

```
=ACC<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:48:10.717

Level 1
```

Display New I/O

```
=>INI<ENTER>
I/O BOARD       INPUTS    OUTPUTS
Main              6         7
1                 8         16
2                 8         8
2 Previous        No Board Connected
```

Enter Access Level 2 (Password Jumper JMP6A Removed)

```
=>2AC
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:49:03.405

Level 2
```

Initialize New I/O

```
=>>INI<ENTER>
I/O BOARD       INPUTS    OUTPUTS
Main              6         7
1                 8         16
2                 8         8
2 Previous        No Board Connected

I/O board(s) have changed
Are the new I/O board(s) correct (Y/N) ? Y<ENTER>
I/O board configuration complete
```

Relay Reenables Itself

```
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:49:24.115
SEL-352-1

=
```

Display Existing I/O

```
=>INI<ENTER>
I/O BOARD       INPUTS    OUTPUTS
Main              6         7
1                 8         16
2                 8         8

=>
```

Power Cycled on Relay to Remove I/O Board

```
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:50:10.122
SEL-352-1
=
```

Automatic Status Message Generated for Failed I/O Test (Entire status report not shown)

```
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:50:13.293
.
.
        TEMP     RAM      ROM      A/D      CR_RAM   EEPROM   IO_BRD
        19.4     OK       OK       OK       OK       OK       FAIL

Relay Disabled
```

Enter Access Level 1 (Password Jumper JMP6A Removed)

```
=ACC<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:50:22.778


Level 1
```

Display New I/O

```
=>INI<ENTER>
I/O BOARD       INPUTS    OUTPUTS
Main              6         7
1                 No Board Connected
1 Previous        8         16
2                 8         8
```

Enter Access Level 2 (Password Jumper JMP6A Removed)

```
=>2AC
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:50:30.747

Level 2
```

Initialize New I/O

```
=>>INI<ENTER>
I/O BOARD       INPUTS    OUTPUTS
Main              6         7
1                 No Board Connected
1 Previous        8         16
2                 8         8

I/O board(s) have changed
Are the new I/O board(s) correct (Y/N) ? Y<ENTER>
Output SELogic settings may be lost due to loss of output contacts
Are you sure (Y/N) ? Y<ENTER>
I/O board configuration complete
```

Relay Reenables Itself

```
EXAMPLE CIRCUIT BREAKER              Date: 11/10/96    Time: 22:50:54.115
SEL-352-1

=
```

IRI (IRIG-B Synchronization)

Access Level 1

The **IRIG** command forces the relay to read the demodulated IRIG-B time-code input at the time of the command.

If the relay reads the time code successfully, it updates the internal clock/calendar time and date to the time-code reading. The relay then transmits a message with relay setting TRMID, date, and time.

```
=>IRI<ENTER>

EXAMPLE: BUS B, BREAKER 3         Date: 02/01/96    Time: 01:45:40.762
=>
```

If no IRIG-B signal is present or the code cannot be read successfully, the relay sends the error message "IRIG-B DATA ERROR."

Note: Normally, it is not necessary to synchronize using this command because the relay automatically synchronizes approximately once a minute. The **IRIG** command is provided to prevent delays during testing and installation checkout.

MET (Metering Report)

Access Level 1

The **METER** command displays the phase-to-neutral and phase-to-phase voltages and currents in primary kilovolts and amperes. It also displays real and reactive power in megawatts and megavars. Refer to ***Metering*** in ***Section 6: Metering and Monitoring*** for a complete description of the meter report. An example is shown below. Use the **MET n** command, where n is a positive number, to repeat the meter report n times. To display a series of eight meter readings, type **MET 8 <ENTER>**.

```
=>MET<ENTER>

EXAMPLE: BUS B, BREAKER 3         Date: 02/01/96    Time: 15:15:24.640

               A         B         C         AB        BC        CA
I (A)          202       198       197       349       339       344
VX(kV)       134.1     133.7     133.5     231.5     230.9     231.9
VY(kV)       134.0     133.8     133.6     231.5     230.9     231.9
dV(kV)       0.371     0.425     0.877
P (MW)       78.61
Q (MVAR)     13.85

=>
```

OPE (Open)

Access Level B

The **OPEN** command asserts the TCMD bit. The TCMD bit remains asserted for 30 cycles, then the relay checks the status of the 52A input assignments to determine if the breaker is open.

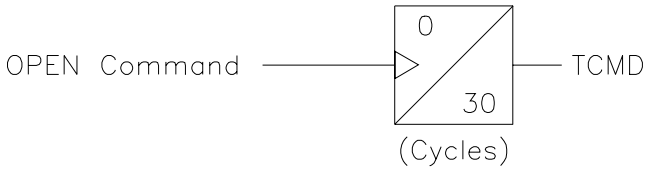


Figure 8.4: TCMD Relay Word Bit

If the breaker opens successfully based on the 52A indication at the end of the 30 cycles, the relay responds with "Breaker OPENED." If the breaker does not open based on the 52A indication at the end of the 30 cycles, the relay responds with "Breaker CLOSED."

The TCMD bit typically is used as part of the trip input assignments such as TRIP3. If the **OPE** command is issued, the relay responds as if it had received a trip initiation. If the retrip logic is used, the relay will close the retrip output contact. The TCMD bit may be used anywhere in the logic that meets your breaker control application needs.

To open the circuit breaker by command, type **OPE <ENTER>**. The prompt "Open Breaker (Y/N) ?" is displayed. Then "Are you sure (Y/N) ?". Typing **N <ENTER>** after either of the above prompts aborts the opening operation with the message "Command Aborted."

If the main board jumper JMP6B is not in place, the relay responds: "Aborted: Breaker Jumper Not in Place."

```
==>OPE<ENTER>
Open Breaker  (Y/N) ? Y<ENTER>
Are you sure (Y/N) ? Y<ENTER>
Breaker OPENED
==>
```

PAS (Passwords)

Access Level 2

The **PASSWORD** command allows you to inspect or change existing passwords.

The factory default passwords for Access Levels 1, B, and 2 are:

Access Level	Factory Default Password
1	OTTER
B	EDITH
2	TAIL

Use **PAS<ENTER>** to inspect passwords. The password for Level 1, B, and 2 are displayed.

```
=>>PAS<ENTER>
1:OTTER
B:EDITH
2:TAIL
=>>
```

WARNING

This device is shipped with default passwords. Default passwords should be changed to private passwords at installation. Failure to change each default password to a private password may allow unauthorized access. SEL shall not be responsible for any damage resulting from unauthorized access.

To change a password, use the following syntax:

PAS n newpas<ENTER>

The two parameters are required:

- **n** specifies the Access Level (1, B, or 2).
- **newpas** specifies the new password. If **newpas** is **DISABLE**, the prompt is disabled.

Designate which access level password to change with the n = 1, B, or 2. The new password designated by newpas can be up to six characters. The following example changes the level one password to Ot3579. The passwords are case sensitive.

```
=>>PAS 1 Ot3579<ENTER>
Set
=>>
```

Similarly, **PAS B** and **PAS 2** can be used to change the Level B and Level 2 passwords, respectively.

The relay sets the password, pulses the ALARM relay closed for approximately one second, and transmits the response "Set" to the display.

Passwords may contain up to six characters and include any combination of letters, numbers, periods, or hyphens. Upper- and lower-case letters are treated as different characters. Strong passwords consist of six characters, with at least one special character or digit and mixed-case sensitivity, but do not form a name, date, acronym, or word. Passwords formed in this manner are less susceptible to password guessing and automated attacks. Examples of valid, distinct strong passwords include:

Ot3579 A24.68 Ih2dcs 4u-Iwg .0351r

To disable the password protection for a particular access level, type **PAS n DISABLE <ENTER>**. The relay responds with "Password Disabled."

After entering new passwords, type **PAS<ENTER>** to inspect them. Make sure they are what you intended, and record the new passwords.

If the passwords are lost, or you wish to operate the relay completely without password protection, install main board jumper JMP6A. With no password protection, you may gain access without knowing the passwords and view or change active passwords and settings.

PUL n (Pulse)

Access Level B

The **PULSE n k** command asserts the selected output contact n for k seconds. The k parameter is optional. If k is not specified, the output contact is pulsed for one second. Main board breaker jumper JMP6B must be in place. After issuing the **PULSE** command, the relay asks for confirmation of the operation, and then asks if you are sure. An invalid output contact name or incorrect k value produces an error message. The ALARM output is pulsed by issuing **PUL !ALARM<ENTER>**. While a contact is being pulsed, no other output contact may change state.

Parameter n may be any existing output contact element name such as OUT201. Parameter k must be a number ranging from 1 to 30 seconds.

```
=>>PUL OUT201<ENTER>
Pulse contact OUT201 for 1 second(s) (Y/N) ? Y<ENTER>
Are you sure (Y/N) ? Y<ENTER>
=>>
```

QUI (Quit)

Access Level 1

The **QUIT** command returns the relay to Access Level 0 from Level 1, B, or 2. The command displays the relay setting TRMID, date, and time of **QUIT** command execution.

Use the **QUI** command when you finish communicating with the relay to prevent unauthorized access. The relay automatically returns to Access Level 0 after a certain inactivity time dependent on the SET P setting TIMEOUT.

```
==>QUI<ENTER>

EXAMPLE: BUS B, BREAKER 3     Date: 02/01/93    Time: 15:15:32.161
=
```

R_S (Restore Factory Default Settings)

Access Level 2

The **R_S** command restores the factory default settings of the relay. The relay is shipped with default settings that are the same in all three setting groups. Use the **R_S** command to return all three setting groups to the factory default settings. This command is useful when settings have been changed, but the desired settings are similar to the factory default settings. **R_S** is only available from the calibration access level during normal operation.

After flash upgrades for new firmware, the relay may require that the **R_S** command be issued to reset its memory of the settings. In this case, the **R_S** command is available from Access Level 2.

```
==>>R_S<ENTER>
Restore factory default settings (Y/N) ? Y<ENTER>
I/O BOARD        TYPE     INPUTS    OUTPUTS
Main              00        6         7
1                 21        8         16
2                 00        No Board Connected

=
```

The relay will pulse the ALARM output when entering Access Level 2 and the calibration access level. When the **R_S** command is issued, the relay is disabled and the ALARM output contact closes until the process is complete, unless an alarm condition already exists.

SER (Sequential Events Records)

Access Level 1

The **SER** command displays the last 512 sequential event records. To limit the number of records displayed, use date parameters with the **SER** command. **SER d1** shows only events triggered on or after the date specified by d1. **SER d1 d2** shows only events triggered on or between the specified dates. The following is an example of the SER report. See ***Section 10: Event Reports and SER*** for a complete description of the report.

```
=>SER 11/12/96 11/13/96<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 11/14/96    Time: 10:35:55.498

FID=SEL-352-1-R100-V-D961101

Example Report Label

#      DATE         TIME           ELEMENT          STATE

1    11/12/96   10:33:54.873   TRIP3              Asserted
2    11/12/96   10:33:55.373   TRIP3              Deasserted
3    11/13/96   10:34:06.872   CLOSE              Asserted
4    11/13/96   10:34:07.372   CLOSE              Deasserted

=>
```

SER C (Clear Sequential Events Records)

Access Level 2

Clear the sequential event records from relay memory with the **SER C** command. The process may take up to 30 seconds under normal operation, or longer if the relay is busy processing a fault or protection logic.

```
=>>SER C<ENTER>
Clear the SER
Are you sure (Y/N) ? Y
Clearing Complete

=>>
```

CAUTION

Automated clearing of the SER buffer should be limited to reduce the possibility of wearing out the nonvolatile memory. Limit automated **SER C** commands to once per week or less.

SET (Edit Settings)

Access Level 2

Configure the relay using the **SET** command. The entire syntax of the **SET** command follows:

SET n setting TERSE<ENTER>

All parameters are optional and perform the following functions:

- **n** specifies the setting group (1, 2, or 3). The default is the active setting group.
- **setting** specifies the setting name to immediately jump to. The default is the first setting.
- **TERSE** disables the display of the new settings at the end of the setting procedure.

If a setting is hidden because that section of the settings is turned OFF, you cannot jump to that setting. TERSE is very useful when making small changes to the settings. For example, the following procedure is recommended when making a change to one setting:

Change the 50FT Setting

```
=>>SET 50FT TERSE<ENTER>
Group 1


Fault Current Logic Settings
Fault Current Detector (0.5-45.0 A Sec)          50FT   = 8.60      ? 8.5<ENTER>
Fault Current Logic (OFF, 1-5, CUSTOM)           FTLOG  = 1         ? END<ENTER>
Save Changes? Y<ENTER>
Settings saved
```

Verify the 50FT Setting

```
=>>SHO 50FT<ENTER>
Group 1


Fault Current Logic Settings
50FT   = 8.50      FTLOG  = 1
TTdo   = 2.000     FCpu   = 4.000
```

Issue <CONTROL>X to Stop Scrolling

```
=>>
```

Table 8.4 lists the editing keys that you can use with the **SET** command.

Table 8.4: Editing Keys for SET Commands

Press Key(s)	Results
^ <ENTER>	Moves to previous entry in a setting category until you get to the first entry in the category, and then it moves to previous category.
< <ENTER>	Moves to previous settings category when making group settings.
> <ENTER>	Moves to next settings category when making group settings.
<ENTER>	Moves to next entry.
END <ENTER>	Exits editing session and displays all settings. Prompts: "SAVE CHANGES (Y/N)?". Type **Y <ENTER>** to save changes and exit, **N <ENTER>** to exit without saving.
<CONTROL> X	Aborts editing session without saving changes.
OFF <ENTER>	Flags a setting as not applicable. Only applies to certain settings.

After you enter a setting, you are prompted for the next setting. Press **<ENTER>** to move from setting to setting. The settings are arranged into families of related settings to simplify setting changes. You can start at a specific setting by entering the setting name as a parameter.

The relay checks each entry to make certain that it is within the allowable input range. If it is not, an "Out of Range" message is generated, and the relay prompts for the setting again.

When you have made all the necessary setting changes, it is not necessary to scroll through the remaining settings. Type **END<ENTER>** at the next setting prompt to display the new settings and request for confirmation.

Answer **Y<ENTER>** to the confirmation request to approve the new settings. If you violate a rule for setting relationships, a fail message is displayed, and the settings prompt moves to the first setting that affects the failure. While the active settings are updated, the relay is disabled, all output contacts return to their normal state (A contacts open, B contacts close), the ALARM output contacts close, and all timers and relay elements reset. The relay logic is fully functional while editing settings. The relay is only disabled for approximately one second when settings are saved.

Refer to the **SHO** command for a list of the factory default settings. Refer to ***Section 7: Setting the Relay*** for all default settings and settings worksheets.

SET G (Edit Global Settings)

Access Level 2

Configure the relay global settings using the **SET G** command. The global settings include the input assignments, relay configuration settings, the front-panel time-out, and the group switching time delay. The entire syntax of the **SET G** command follows:

SET G setting TERSE<ENTER>

The two parameters are optional and perform the following functions:

- **setting** specifies the setting name to immediately jump to. The default is the first setting.
- **TERSE** disables the display of the new settings at the end of the setting procedure.

The **SET G** procedure works just like the **SET** procedure. Table 8.4 lists the editing keys that you can use with the **SET** command.

Refer to the **SHO G** command for a list of the factory default settings. Refer to ***Section 7: Setting the Relay*** for all default settings and settings worksheets.

SET P (Edit Port Settings)

Access Level 2

Configure the relay port settings using the **SET P** command. The port settings include the communication and protocol settings. The entire syntax of the **SET P** command follows:

SET P n setting TERSE<ENTER>

The two parameters are optional and perform the following functions:

- **n** specifies the serial port number (1, 2, 3, or 4). Default is the port issuing the command.
- **setting** specifies the setting name to immediately jump to. The default is the first setting.
- **TERSE** disables the display of the new settings at the end of the setting procedure.

The **SET P** procedure works just like the **SET** procedure. Table 8.4 lists the editing keys that you can use with the **SET** command.

Refer to the **SHO P** command for a list of the factory default settings. Refer to ***Section 7: Setting the Relay*** for all default settings and settings worksheets.

SET R (Edit Report Settings)

Access Level 2

Configure the relay report settings using the **SET R** command. The report settings include the alias name assignments, the breaker alarms, a report label, and sequential event record trigger conditions. The entire syntax of the **SET R** command follows:

SET R setting TERSE<ENTER>

The two parameters are optional and perform the following functions:

- **setting** specifies the setting name to immediately jump to. The default is the first setting.
- **TERSE** disables the display of the new settings at the end of the setting procedure.

The **SET R** procedure works just like the **SET** procedure. Table 8.4 lists the editing keys that you can use with the **SET** command.

Refer to the **SHO R** command for a list of the factory default settings. Refer to ***Section 7: Setting the Relay*** for all default settings and settings worksheets.

Note: Make Sequential Events Recorder (SER) Settings With Care

The relay triggers a row in the Sequential Events Recorder (SER) event report for any change of state in any one of the elements listed in the SER1, SER2, or SER3 trigger settings. Nonvolatile memory is used to store the latest 512 rows of the SER event report so they can be retained during power loss. The nonvolatile memory is rated for a finite number of "writes." Exceeding the limit can result in an EEPROM self-test failure. An average of 1 state change every 3 minutes can be made for a 25-year relay service life.

SET T (Edit Display Text Settings)

Access Level 2

Configure the front-panel Local Bit and Display Point settings using the **SET T** command. The Local Bit settings are NLBn (function name label), CLBn ("clear bit" label), SLBn ("set bit" label), and PLBn ("pulse bit" label). The Display Point settings are DPn_1 and DPn_0, the text displays for the two logic states of variable DPn. (Note: the DPn variables are set using the standard **SET** command.) See ***Section 9: Front-Panel Interface*** for more information on these settings. The entire syntax of the **SET T** command follows:

SET T setting TERSE<ENTER>

The two parameters are optional and perform the following functions:

- **setting** specifies the setting name to immediately jump to. The default is the first setting.
- **TERSE** disables the display of the new settings at the end of the setting procedure.

The **SET T** procedure works just like the **SET** procedure. Table 8.4 lists the editing keys that you can use with the **SET** command.

Refer to the **SHO T** command for a list of the factory default settings. Refer to ***Section 7: Setting the Relay*** for all default settings and settings worksheets.

SHO (Show Settings)

Access Level 1

SHOWSET displays the relay settings of the currently selected group. The entire syntax of the **SHO** command follows:

SHO n setting A<ENTER>

- **n** specifies the setting group (1, 2, or 3). The default is the active setting group.
- **setting** specifies the setting name to immediately jump to. The default is the first setting.
- If **setting = A,** then hidden settings are shown in addition to the regular settings.

Control characters provide control over the scrolling of the data:

Temporarily Stop Scrolling:	**<CTRL>Q**	(hold down the Control key and press Q)
Restart Scrolling:	**<CTRL>S**	(hold down the Control key and press S)
Cancel Scrolling Completely:	**<CTRL>X**	(hold down the Control key and press X)

Settings cannot be entered or modified with this command. Change settings with the **SET** command from Access Level 2. The following example shows the factory default settings for a nominal 5 A relay. Refer to ***Section 7: Setting the Relay*** for a list of all settings.

```
=>SHO<ENTER>
Group 1

RELID  =EXAMPLE SEL-352-1
TRMID  =EXAMPLE CIRCUIT BREAKER
Topen  = 33        Tclose = 66        SlowTr = 42.0      SlowCl = 83.0
CTR    = 600.0     XPTR   = 4300.0    YPTR   = 4300.0

SALOG  = OFF

50FT   = 8.60      FTLOG  = 2
FCpu   = 4.000

50LD   = 0.50      50N    = 0.50      LDLOG  = 1
LPpu   = 3.25      LDpu   = 5.50

37OP   = 2.07      47Q    = 18.7      87TH   = 4.3
VNpu   = 10.00     Kmag   = 5.0       Kang   = 10.0      THLOG  = ON
OPpu   = 3.00
26CP   = 1.11      26CF   = 1.45      26TP   = 3.49      26TF   = 4.56
CRTC   = 80        TRTC   = 80

87H    = 57.0      87FO   = 4.0       59H    = 100.0     FOLOG  = 1
FPpu   = 25.00     FFpu   = 30.00

46UB   = 16        UBLOG  = ON
UCpu   = 6.00      UPpu   = 50.00     UFpu   = 60.00
DELOG  = OFF

59L    = 57.0      27D    = 10.0      CLSLOG = 1         CLSdo  = 5.00
RCApu  = 0.00      RCBpu  = 0.00      RCCpu  = 0.00

RTPLOG = 1

SBLOG  = OFF

M86T   =FBF + LBF + TTF + CTF + FOBF + UBBF
50MD   = 0.10      TRLOG  = 2
M2pu   = 600.000   M3pu   = 600.000
MER    =UBPF + LPF + FOPF + LODPF + TRIPA + TRIPB + TRIPC +
        CLOSE + MCLOSE + 26CPA + 26CPB + 26CPC + 26TPA + 26TPB +
        26TPC + MDT

OUT101 =86BFT
OUT102 =86BFT
OUT103 =BALRM
OUT104 =!50MNA*!50MNB*!50MNC*!52AA*!52AB*!52AC
OUT105 =MDT
OUT106 =LPF + FOPF + UBPF
OUT107 =86RS

DP1    =IN104
DP2    =0
DP3    =0
DP4    =0
DP5    =0
DP6    =0
DP7    =0
DP8    =0
DP9    =0
DP10   =0
DP11   =0
DP12   =0
DP13   =0
DP14   =0
DP15   =0
DP16   =0
```

SHO G (Show Global Settings)

Access Level 1

SHOWSET G displays the relay global settings of the currently selected group. The global settings include the input assignments, relay configuration settings, the front-panel time-out, and the group switching time delay. The syntax of the **SHO G** command follows:

SHO G setting<ENTER>

- **setting** specifies the setting name to immediately jump to. The default is the first setting.

Settings cannot be entered or modified with this command. Change settings with the **SET G** command from Access Level 2. The following example shows the factory default settings. Refer to ***Section 7: Setting the Relay*** for a list of all settings.

```
=>SHO G<ENTER>
SS1    =0
SS2    =0
TRIPA  =IN101 + TCMD + LB1
TRIPB  =IN102 + TCMD + LB1
TRIPC  =IN103 + TCMD + LB1
TRIP3  =IN101*IN102*IN103 + TCMD + LB1
52AA   =IN104
52AB   =IN104
52AC   =IN104
MODST  =IN105
CLOSE  =IN106
MCLOSE =IN106 + CCMD + LB2
LOD1   =NA
LOD2   =NA
LODCT  =NA
LER    = 30        PRE    = 2         NFREQ  = 60        PHROT  = ABC
DATE_F = MDY       FP_TIMEOUT= 5      TGR = 5

=>
```

SHO P (Show Port Settings)

Access Level 1

SHOWSET P displays the relay serial port settings. The port settings include the communications and protocol settings. The syntax of the **SHO P** command follows:

SHO P n setting<ENTER>

The two parameters are optional and perform the following functions:

- **n** specifies the serial port number (1, 2, 3, or 4). Default is the port issuing the command.
- **setting** specifies the setting name to immediately jump to. The default is the first setting.

Settings cannot be entered or modified with this command. Change settings with the **SET P** command from Access Level 2. The following example shows the factory default settings. Refer to ***Section 7: Setting the Relay*** for a list of all settings.

```
=>SHO P<ENTER>

PROTO  = SEL
SPEED  = 2400      D_BITS = 8         PARITY = N         STOP   = 1
TIMEOUT= 5         AUTO   = N         RTS_CTS= N         FAST_OP= N
=>
```

SHO R (Show Report Settings)

Access Level 1

SHOWSET R displays the relay report settings. The report settings include the alias name assignments, the breaker alarms, a report label, and sequential event record trigger conditions. The syntax of the **SHO R** command follows:

SHO R setting<ENTER>

- **setting** specifies the setting name to immediately jump to. The default is the first setting.

Settings cannot be entered or modified with this command. Change settings with the **SET R** command from Access Level 2. The following example shows the factory default settings. Refer to ***Section 7: Setting the Relay*** for a list of all settings.

```
=>SHO R<ENTER>
ALIAS1 =NA
ALIAS2 =NA
ALIAS3 =NA
ALIAS4 =NA
ALIAS5 =NA
ALIAS6 =NA
ALIAS7 =NA
ALIAS8 =NA
ALIAS9 =NA
ALIAS10=NA
ALIAS11=NA
ALIAS12=NA
ALIAS13=NA
ALIAS14=NA
ALIAS15=NA
ALIAS16=NA
ALIAS17=NA

Press RETURN to continue
ALIAS18=NA
ALIAS19=NA
ALIAS20=NA
BALRM  =FTRS FCRS 52ACV CWO TWO BDNC BPF CAMT MCC ST SC PTD
LABEL  =Example Report Label
SER1   =NA
SER2   =NA
SER3   =NA

=>
```

SHO T (Show Display Text Settings)

Access Level 1

View the front-panel Local Bit and Display Point settings using the **SHO T** command. The Local Bit settings are NLBn (function name label), CLBn ("clear bit" label), SLBn ("set bit" label), and PLBn ("pulse bit" label). The Display Point settings are DPn_1 and DPn_0, the text displays for the two logic states of variable DPn. (Note: the DPn variables are viewed using the standard **SHO** command.) See ***Section 9: Front-Panel Interface*** for more information on these settings. The entire syntax of the **SHO T** command follows:

SHO T setting <ENTER>

- **setting** specifies the setting name to immediately jump to. The default is the first setting.

Settings cannot be entered or modified with this command. Change settings with the **SET T** command from Access Level 2 (**SET** command for DPn variables). The following example shows the factory default text settings. Refer to ***Section 7: Setting the Relay*** for all default settings and settings worksheets.

```
=>SHO T<ENTER>

Text Settings
NLB1   =MANUAL TRIP    CLB1   =RETURN  SLB1   =        PLB1   =TRIP
NLB2   =MANUAL CLOSE   CLB2   =RETURN  SLB2   =        PLB2   =CLOSE
NLB3   =               CLB3   =        SLB3   =        PLB3   =
NLB4   =               CLB4   =        SLB4   =        PLB4   =
NLB5   =               CLB5   =        SLB5   =        PLB5   =
NLB6   =               CLB6   =        SLB6   =        PLB6   =
NLB7   =               CLB7   =        SLB7   =        PLB7   =
NLB8   =               CLB8   =        SLB8   =        PLB8   =
NLB9   =               CLB9   =        SLB9   =        PLB9   =
NLB10  =               CLB10  =        SLB10  =        PLB10  =
NLB11  =               CLB11  =        SLB11  =        PLB11  =
NLB11  =               CLB11  =        SLB11  =        PLB11  =
NLB13  =               CLB13  =        SLB13  =        PLB13  =
NLB14  =               CLB14  =        SLB14  =        PLB14  =
NLB15  =               CLB15  =        SLB15  =        PLB15  =
NLB16  =               CLB16  =        SLB16  =        PLB16  =

DP1_1  =BREAKER CLOSED   DP1_0  =BREAKER OPEN
DP2_1  =                 DP2_0  =
DP3_1  =                 DP3_0  =
DP4_1  =                 DP4_0  =
DP5_1  =                 DP5_0  =
DP6_1  =                 DP6_0  =
DP7_1  =                 DP7_0  =
DP8_1  =                 DP8_0  =
DP9_1  =                 DP9_0  =
DP10_1 =                 DP10_0 =
DP11_1 =                 DP11_0 =
DP12_1 =                 DP12_0 =
DP13_1 =                 DP13_0 =
DP14_1 =                 DP14_0 =
DP15_1 =                 DP15_0 =
DP16_1 =                 DP16_0 =

=>>
```

STA (Status Report)

Access Level 1

The **STATUS** command displays a report of the self-test diagnostics. The relay automatically executes the **STATUS** command whenever the self-test software enters a warning or failure state. You may repeat the **STA** command by appending a number as a repeat count parameter. Type **STA 4<ENTER>** to view the status information four times.

If a warning or failure state occurs, the next time the **STA** command is issued, the warning state is reported. If a warning or failure occurs, it will not be cleared until relay power is cycled and the problem is fixed. Saving relay settings performs a warm boot of relay logic. This may clear some warnings, but do not ignore the warning; contact the factory.

The **STATUS** report format appears below:

```
=>STA<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 11/12/96    Time: 16:43:21.794

FID=SEL-352-2-X105-V0-Z101101-D20010116 CID=EBE8
SELF TESTS

W=Warn    F=Fail

       IA       IB       IC       VAX      VBX      VCX
OS      5       -5        2        1        3        3

       VAY      VBY      VCY      MOF
OS     -1        0       -2        1

       +5V_PS   +5V_REG  -5V_REG  +12V_PS  -12V_PS  +15V_PS  -15V_PS
PS      4.92     5.01    -5.00     12.09   -12.21    14.92   -14.92

       TEMP     RAM      ROM      A/D      CR_RAM   EEPROM   IO_BRD
        28.6    OK       OK       OK       OK       OK       OK

 Relay Enabled
=>
```

Refer to ***Section 6: Metering and Monitoring*** for a complete description of the status report.

TAR (Show Relay Word Targets)

Access Level 1

The **TARGET** command displays the default row of the Relay Word showing the Relay Word bit names and their values, either logical 1 (asserted) or logical 0 (deasserted). The syntax of the **TAR** command follows:

TAR n k X<ENTER>

- **n** specifies a new default Relay Word row by entering the number or the specific Relay Word bit name. If n is not specified, the last default row is displayed.
- **k** specifies a repeat count for the command. The default is 1.
- **X** allows viewing a Relay Word row without changing the default row.

The default row number can also be changed by the **TAR F** command, but each serial port has independent defaults. The default row number returns to 0 when the port times out, the **QUIT** command is executed, **TAR 0** command is executed, or the **TAR R** command is executed.

The **TARGET** command does not remap the front-panel LEDs. See the **TAR F** command.

The following examples demonstrate the **TARGET** command:

```
=>>TAR<ENTER>            Default Row is 0

EN      PF      86BFT   86RS    TRIP    CLOSE   52A     MOD
1       0       0       0       0       1       0       0
=>>TAR 8<ENTER>          Display and Change Default to Row 8

25M     25C     46C     46B     46A     50MD    50LD    50FT
0       0       0       0       0       0       0       0
=>>TAR<ENTER>            Default Row is 8

25M     25C     46C     46B     46A     50MD    50LD    50FT
1       1       0       0       0       0       1       0
=>>TAR 8 5<ENTER>        Display Row 8 Five Times

25M     25C     46C     46B     46A     50MD    50LD    50FT
1       1       0       0       0       0       1       0
1       1       0       0       0       0       1       0
1       1       0       0       0       0       1       0
0       0       0       0       0       0       0       0
0       0       0       0       0       0       0       0
=>>TAR 37OPA X<ENTER>    Display Row 9 (37OPA) But Do Not Change Default

Y47Q    X47Q    37OPC   37OPB   37OPA   87HC    87HB    87HA
0       0       0       0       1       0       0       0
=>>TAR<ENTER>

25M     25C     46C     46B     46A     50MD    50LD    50FT
0       0       0       0       0       0       0       0
=>>TAR R<ENTER>          Reset Default to Row 0

EN      PF      86BFT   86RS    TRIP    CLOSE   52A     MOD
1       0       0       0       0       0       0       0
=>>
```

Refer to ***Appendix F: Relay Word*** for a list of the Relay Word and the corresponding rows.

TAR F n (Show Relay Word Targets on Front Panel)

Access Level 1

The **TARGET F** command works like the **TARGET** command, but it also remaps the second row of target LEDs on the front panel to follow the default row. The syntax of the **TAR F** command follows:

TAR F n k X<ENTER>

- **n** specifies a new default Relay Word row by entering the number or the specific Relay Word bit name. If n is not specified, the last default row is displayed.
- **k** specifies a repeat count for the command for the serial port display. The default is 1.
- **X** allows remapping the LEDs to a Relay Word row without changing the default row.

The default row number returns to 0 when the serial port times out, the **QUIT** command is executed, the **TAR 0** command is executed, or the **TAR R** command is executed.

The front-panel LEDs remain remapped until the front panel times out, the **TAR R** command is executed, or the **<TARGET RESET>** button is pushed.

Refer to ***Appendix F: Relay Word*** for a list of the Relay Word and the corresponding rows.

TAR R (Reset Targets)

Access Level 1

The **TARGET R** command resets the default row for the **TAR** and **TAR F** commands to 0, and remaps the second row of front-panel LEDs to display Row 1, which is the standard target display.

Use the **TAR R** command to return the front-panel LEDs to the standard targets when you are done using the **TAR** or **TAR F** command for testing.

TIM (Time)

Access Level 1

The **TIME** command displays or sets the time stored by the internal clock. View the current time with **TIM<ENTER>.** To set the clock, type **TIM t1<ENTER>** where t1 is the new time in h:m:s and the seconds are optional. Separate the hours, minutes, and seconds with colons, semicolons, spaces, commas, or slashes. The following example sets the clock to 23:30:00:

```
=>TIM 23:30:00<ENTER>
23:30:00
=>
```

A quartz crystal oscillator provides the time base for the internal clock. You can also set the time clock automatically through the relay time-code input using a source of demodulated IRIG-B time-code.

Note: After setting the time, allow at least 60 seconds before powering down the relay or the new setting may be lost.

TRI (Trigger An Event)

Access Level 1

The **TRIGGER** command generates an event record. The command is a convenient way to record all inputs and outputs from the relay at any time you desire (e.g., testing or commissioning). The event type is recorded as INT for internal triggering any time the relay is triggered.

```
=>TRI<ENTER>
Triggered

=>
EXAMPLE CIRCUIT BREAKER              Date: 02/01/96    Time: 13:43:25.921

Event: INT        Frequency (Hz):  60.0

=>Alarm Conditions
```

The SEL-352 Relay asserts the ALARM output during power up until all self-tests pass and whenever a diagnostic test fails. In addition to these, the ALARM output pulses with the commands and conditions shown in Table 8.5.

Table 8.5: Commands With Alarm Conditions

Command	Condition
2AC	Entering Access Level 2 or Three wrong password attempts into Access Level 2
ACC	Three wrong password attempts into Access Level 1
BAC	Entering Breaker Access Level or Three wrong password attempts into Breaker Access Level
COP m n	Copying a setting group to the active setting group
GRO n	Changing the active setting group
PAS n newpas	Any password is changed
SET commands	Changing the SET G settings, the SET R settings, or the active group SET settings (SET P does not alarm)

Main Board Jumpers

The main board jumpers listed in Table 8.6 affect the commands shown.

Table 8.6: Main Board Jumpers

Jumper	Comment
JMP6A	Disables password protection when installed
JMP6B	Enables **CLO**, **OPE**, and **PUL** commands when installed

SEL-352-1, -2 RELAY COMMAND SUMMARY

ASCII Command	Command Description	Minimum Access Level	Front-Panel Equivalent
2AC ACC BAC	Enter Access Level 2, 1, or B. Install main board password jumper JMP6A to disable password protection.	1, B 0 1	Relay prompts if necessary
BRE	Display detailed breaker pole operations, summary, and alarms.	1	EVENTS
BRE C	Clear breaker pole operations, operation summary, and alarms.	2	
BRE R	Clear breaker pole operations, operation summary, and alarms (SEL-352-2 Relay only).	2	
BRE S	Display only breaker operation summary and alarms.	1	
BRE W	Preload breaker wear data (SEL-352-2 Relay only).	B	
CAL	Enter the calibration access level.	2	
CEVE	Display compressed version of EVE for SEL-5601 software.	1	
CLO	Assert the CCMD bit for 30 cycles. JMP6B must be in place.	B	CNTRL
CON n	Control Remote Bit RBn.	2	
COP m n	Copy settings from group m (1, 2, or 3) to group n (1, 2, or 3).	2	
DAT DAT d1	Display relay date according to the format setting DATE_F. Set relay date to d1. If the date format setting DATE_F = MDY, d1 is m/d/y. If DATE_F = YMD, d1 is y/m/d.	1	OTHER
EVE n A Ss Lc	Display an event report with VX and I channels. n specifies event number according to the HIS command. A specifies the alternate report showing VY (not VX and I). Ss specifies the samples per cycle (s = 4, 8, 16, 64). Lc specifies the length in cycles (c = 1 to LER setting). Unspecified options are n = 1, no A, s = 4, and c = LER.	1	
GRO GRO n	Display the active setting group number and group variable. Change the group variable to n (n = 1, 2, or 3).	1 2	GROUP GROUP
HEA k HEA C HEA R	Display the energy in the trip and close resistors k times. Reset the thermal model to zero. Reset the thermal model to zero.	1 2 2	
HIS n HIS C	Show the summaries of the n latest events. Clear all of the summaries and corresponding events.	1 2	EVENTS
INI	Initialize and display the inputs and outputs per I/O board.	1	
IRI	Attempt IRIG-B time-code input synchronization. The relay attempts synchronization automatically every minute.	1	
MET k	Display metering data k times.	1	METER
OPE	Assert the TCMD bit for 30 cycles. JMP6B must be in place.	B	CNTRL

ASCII Command	Command Description	Minimum Access Level	Front-Panel Equivalent
PAS	Show access level passwords.	2	
PAS n	Show Access Level n password (n = 1, 2, or B).	2	
PAS n pass	Change Access Level n password to pass (pass = up to 6 letters, numbers, periods, or hyphens).	2	SET
PUL n k	Pulse output contact n (n = output contact element name, i.e., OUT201) for k seconds (k = 1 to 30). If k is not specified, 1 second is used. JMP6B must be in place.	B	
QUI	Quit. Returns to Access Level 0.	0	OTHER
R_S	Restore factory default settings.	2	
SER d1 d2	Show rows in the Sequential Events Recorder (SER) from date d1 to date d2. No date parameters show all records. d2 defaults to d1 if not specified. Entry of dates is dependent on the Date Format setting DATE_F (= MDY or YMD).	1	EVENTS
SER C	Clear the sequential events records.	2	
SET n	Edit group n (n = 1, 2, or 3) relay settings.	2	SET
SET G	Edit global (inputs, relay configuration) settings.	2	
SET P n	Edit serial port n (n = 1 to 4) settings. Defaults to the port issuing the command.	2	SET
SET R	Edit reporting (Aliases, SER, BALARM) settings.	2	
SET T	Edit Local Bit and Display Point text settings.	2	
setting	Give a setting name to jump to that setting immediately.		
TERSE	The TERSE option disables the setting verification display.		
SHO n	Show group n (n = 1, 2, or 3) relay settings.	1	SET
SHO G	Show global (inputs, relay configuration) settings.	1	
SHO P n	Show serial port n (n = 1 to 4) settings. Defaults to the port issuing the command.	1	SET
SHO R	Show reporting (Aliases, SER, BALARM) settings.	1	
SHO T	Show Local Bit and Display Point text setting.	1	
setting	Give a setting name to jump to that setting immediately.		
A	The A option includes hidden settings in the display.		
STA	Display the relay self-test status.	1	STATUS
TAR n k	Display Relay Word row corresponding to n (n = row # or bit name) k times on the screen.	1	
TAR F n k	Same as TAR command, but the lower row of front-panel LEDs are remapped to follow the displayed Relay Word row.	1	
TAR R	Reset latching targets, display Relay Word Row 0 on the screen and display Relay Word Row 0 and Row 1 on the target LEDs.	1	TARGET RESET
X	View Relay Word Row without changing default row.	1	
TIM	Display relay time (24 hour time).	1	OTHER
TIM t1	Set relay time to t1 (t1 = h:m:s, seconds are optional)		OTHER
TRI	Trigger an event report. INT is reported for the event type.	1	

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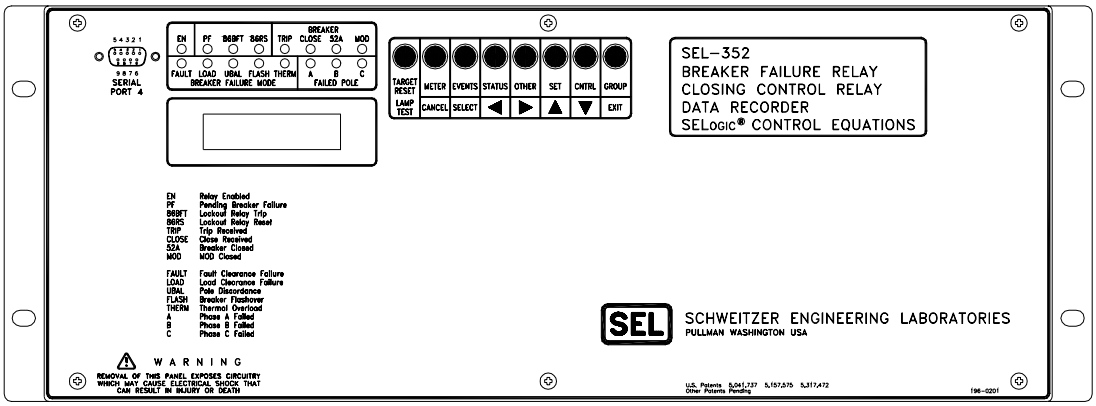
SECTION 9: FRONT-PANEL INTERFACE

FRONT-PANEL OPERATION

The SEL-352 Relay front panel, shown in Figure 9.1, includes a 2-line, 16-character LCD, 16 LED target/indicators and 8 pushbuttons for local communication.



DWG. M3521009

Figure 9.1: SEL-352 Relay Front-Panel Display

The LCD shows event, metering, setting, and relay self-test status information. The display is controlled with the eight multifunction pushbuttons. The target LEDs display relay target information as described by the legend.

Time-Out

If no buttons are pressed on the front panel, the relay waits a time period specified in the SET G setting FP_TIMEOUT and then takes the following actions:

- The front-panel LCD resets to the default metering display.
- The front-panel access level reverts to Access Level 1.
- The LCD back lighting is turned off.
- Any routine being executed via a front-panel command is interrupted.
- The target LEDs revert to the default targets.

FP_TIMEOUT is factory set to 5 minutes and can be set from 0 to 30 minutes. If zero is selected, the front panel will never time-out. A zero setting is useful when testing but do not leave the time-out set at zero. The back light will fail if lit for prolonged periods of time, and the target LEDs that may be changed using the **TAR F** command will not be reset to the default targets.

Displays

The LCD is controlled by the pushbuttons and automatic messages the relay generates. The **<EXIT>** button always returns the display to the default display. The default display consists of the following: (1) a message "Press CNTRL for Local Control", if any of the Local Bit settings have been specified; (2) Display Point messages which have been activated by the logical state of a Display Point variable; or (3) a metering display showing the primary current values of IA, IB, and IC, if neither Local Bits nor Display Points have been specified. Local Bits and Display Points are discussed later in this section.

Error messages such as self-test failures are displayed on the LCD in place of the default metering display when they occur. Do not power down the relay if this occurs; refer to ***Section 11: Testing and Troubleshooting*** for further instructions.

During power up and when executing the **R_S** command to reset factory default settings, the LCD displays "Initializing." This message will remain until the relay is again enabled.

Menu choices on the LCD are listed horizontally on the second line. The first character of the menu choice is underlined. The left and right arrow buttons move the underline to the adjacent menu selection. Once the underline indicates your selection, use the **<SELECT>** button to select it.

Special characters are displayed when viewing the SER reports. Figure 9.2 shows symbols for asserted and deasserted bits.

Figure 9.2: Front-Panel Symbols for Asserted and Deasserted Bits

Local Bits (LB1–LB16)

Local Bits are used for local control from the front panel. They are intended to replace manual switches and pushbuttons normally installed for control of specific functions. There are 16 Local Bits, LB1 to LB16. These designations appear as elements in the Relay Word, for use in SELOGIC® control equations. Like Remote Bits, described in ***Section 5: Control Logic***, Local Bits can be set on or off, or they can be pulsed for one processing interval to mimic a momentary pushbutton.

Local Bits are specified using the **SET T** command through a serial port. This command is used for defining the associated text which is to appear on the LCD, to inform the user what function is being performed by the Local Bit, and the position (state) of the bit. For each Local Bit LBn, there are four settings:

NLBn: Local Bit Name label (max. 14 characters)
CLBn: Local Bit Clear (OFF) label (max. 7 characters)
SLBn: Local Bit Set (ON) label (max. 7 characters)
PLBn: Local Bit Pulse (MOMENTARY) label (max. 7 characters)

There are four combinations of these settings that the relay will accept:

NLBn, CLBn, SLBn: function label, OFF, ON
NLBn, CLBn, PLBn: function label, OFF, MOMENTARY
NLBn, CLBn, SLBn, PLBn: function label, OFF, ON, MOMENTARY
All four settings set to NA, or "null": unused Local Bit

An example of how these settings are used is illustrated by the default LB1 settings stored in the relay at the factory. A **SHO T** serial port command reveals that the LB1 settings are:

NLB1 = MANUAL TRIP
CLB1 = RETURN
SLB1 = (null)
PLB1 = TRIP

When the CNTRL pushbutton is pushed, the display shows the following:

MANUAL TRIP ← →
Position: RETURN

This shows that a Local Bit has been assigned to the trip function, using NLB1 as the label, and that the bit is presently OFF, using the CLB1 label. The right/left arrows are used to scroll to other Local Bit functional displays that have been specified.

If the user decides to trip the relay using this Local Bit, he pushes the SELECT button. The display then changes to:

MANUAL TRIP
TRIP? Yes No ← →

If Yes, the user employs the left arrow to underline Yes, then the SELECT button to perform the trip. While the Local Bit is being asserted (pulsed) to perform the trip, the TRIP target lights, and the display briefly appears as follows:

MANUAL TRIP ← →
Position: TRIP

This indicates, using the PLB1 setting, that the bit is being pulsed. After the bit returns to the OFF state, the display returns to the original display:

MANUAL TRIP ← →
Position: RETURN

For tripping or any other function to occur, the LBn Relay Word bit must be assigned to the appropriate SELOGIC control equations for the desired function.

The relay stores the Local Bit states in nonvolatile memory. They will remain intact through loss of dc power to the relay and through settings changes, provided the settings changes themselves do not redefine the Local Bits or alter the conditions for operating them.

Display Points (DP1–DP16)

Programmable Display Points are customized messages which appear on the LCD in response to the logical state of the Display Point variable. Display Points serve a very useful function by providing specific visual status or alarm functions on the front panel LCD of the relay. There are 16 Display Point variables, DP1 through DP16. The settings are SELOGIC control equations that define when the variable DPn will be in a logical 1 or logical 0 state. There are two additional settings to define what is to be displayed in response to each logical state, denoted DPn_1 and DPn_0. The user can specify either or both of these settings for a defined DPn. The variables DP1 to DP16 are set using the **SET** serial port command. The text messages DPn_1 and DPn_0 are defined using the **SET T** serial port command.

Referring to the default values stored in the relay at the factory, a **SHO** serial port command reveals that the variable DP1 = IN104. The DP1 Display Point variable is set to respond to whether IN104, connected to a breaker 52a contact, is asserted or deasserted. DP1 thus indicates breaker position. A **SHO T** serial port command reveals that DP1_1 = BREAKER CLOSED and DP1_0 = BREAKER OPEN. Since both text messages are defined, there will always be one of them shown on the default display, depending on whether the IN104 input (and the DP1 variable) is asserted or deasserted. If only one of the text messages is defined, the relay will only display a message when DP1 is in the proper state for the defined message. The front panel scrolls through all active displays, showing two lines of messages for two seconds at a time before moving on to the next messages.

Target LEDs

The target LEDs are an indication of what the relay has detected on the power system. The front-panel legend gives a brief description of each target, but ***Section 5: Control Logic*** describes each target LED in detail and provides a logic diagram.

The only time the target LEDs do not illuminate according to their labels is when the **TAR F** command is issued through one of the serial ports. The **TAR F** command remaps the second row of LEDs to follow a particular row in the Relay Word. Refer to ***Section 8: Serial Port Communications and Commands*** for a complete description of the **TAR F** command.

Password Access

Commands that are at Access Level 2 (**2AC**) or the Breaker Access Level (**BAC**) are password protected from the front panel. If you issue a command from the front panel that requires a password, and you are not at an access level that allows execution of that command, the relay prompts you for a password. After you enter the password, you remain at that access level until the front panel times out, you move to a higher access level, or you enter **QUIT** from the **<OTHER>** menu.

If the password jumper is installed, you will not be prompted for a password. If the password has been disabled with **PAS n DISABLE<ENTER>** you will not be prompted for a password.

When prompted for a password, enter the BAC or 2AC password, depending on the requirements of the command. All commands are available using the 2AC password.

PUSHBUTTONS

Eight multifunction pushbuttons control the front-panel display. The button legend defines the primary function in the top row and the secondary function in the bottom row. The primary functions are for command selection and the secondary functions are for cursor movements and specific commands within dialogues.

TARGET RESET

The left-most button is dedicated to the **<TARGET RESET>** function. Except while viewing or editing settings, pressing **<TARGET RESET>** causes the front-panel LEDs to illuminate for a one-second lamp test and then clear all target LEDs except for the EN LED, which is illuminated if the relay is enabled. While viewing or editing settings, the **<TARGET RESET>** button displays specific information about the displayed setting.

METER

The **<METER>** display is updated every two seconds. Three meter values are displayed at a time. Use the **<↑>** and **<↓>** keys to move between meter values.

The **<METER>** button performs the **MET** serial port command.

EVENTS

Push the **<EVENTS>** button to display short event summaries, SER events, and breaker operation data. Use the **<←>** and **<→>** buttons to scroll between His, SER, and Breaker. Press the SELECT button when the cursor is on the desired record type.

If no records exist after selecting one of the record type options, the display gives an error message and terminates the command. If there are records to view, the display prompts for the date of the desired records. Use the **<←>** and **<→>** buttons to scroll through the available dates, and press **<SELECT>** when on the desired date. After selecting a date, use the **<↑>** and **<↓>** keys to move between data records on that date.

The **<EVENTS>** button performs the **HIS**, **SER**, and **BRE** serial port commands.

STATUS

The **<STATUS>** button displays the relay status information. Use the **<↑>** and **<↓>** buttons to move between different status fields and the **<←>** and **<→>** buttons to scroll the FID data.

The **<STATUS>** button performs the **STA** serial port command.

OTHER

The **<OTHER>** button is used to select the following functions: date, time, and quit. Use the **<←>** and **<→>** buttons to scroll between DATE, TIME, and QUIT. The **<SELECT>** button selects which function to use. The QUIT function returns the relay to Access Level 1. The TIME and DATE functions display and set the relay's internal clock.

When the date and time are displayed, the cursor identifies which character can be modified. Use the **<←>** and **<→>** buttons to move to a different character. Use the **<↑>** and **<↓>** buttons to change the characters value. Push the **<SELECT>** button to accept the changes.

The **<OTHER>** button performs the **DAT**, **TIM**, or **QUI** serial port commands.

SET

To show or set relay settings, press the **<SET>** button. There are three set/show options: GROUP, PORT, and PASS. GROUP is the default for both set and show. Use the **<←>** and **<→>** buttons to move to the desired option, and select it with the **<SELECT>** button.

Selecting GROUP or PORT will prompt for the setting group or port number to modify. Once the number is selected, a SET/SHOW menu is displayed. SHOW is the default. Selecting either set or show displays the settings. Pressing the **<TARGET RESET>** button anytime while scrolling through or changing the settings will display a help message.

When changing the group settings, the setting category is first displayed. Use the **<↑>** and **<↓>** buttons to scroll through the setting categories. Select a category and the appropriate settings will be displayed one at a time. Again, use the **<↑>** and **<↓>** buttons to scroll through the settings. A setting must first be selected before a change can be made.

Selecting PASS will prompt for which access level password to set. Once the level is selected, a password may be entered. The password must be terminated by a space if it is less than 6 characters long.

The **<SET>** button performs the **SET**, **SET P**, **PAS**, **SHO**, or **SHO P** serial port commands.

CNTRL

Use the CNTRL button to perform control functions specified in the settings for Local Bits LB1-LB16. The default is to use the CNTRL button to open or close the breaker through the LB1 and LB2 Local Bits. Select MANUAL TRIP or MANUAL CLOSE using the **<←>** and **<→>** buttons, and then press SELECT. Confirm by using the **<←>** and **<→>** buttons to underscore Yes or No then press SELECT. Selecting Yes will attempt the desired operation, while selecting No cancels the command.

The operation pulses the LB1 or LB2 bits for 30 cycles. The breaker can be controlled only if these bits are used in the relay trip and close logic. For example, you could specify the SET G setting TRIPA = ... + LB1 + ... to include the LB1 bit as shown.

The **<CNTRL>** button performs the **OPE** or **CLO** serial port commands in the default mode.

GROUP

When you select the **<GROUP>** button, the relay presents a SET/SHOW menu. Selecting SHOW displays the active group and the group variable. Selecting **<SET>** allows you to set the group variable by using the **<↑>** and **<↓>** buttons. When the desired group variable is displayed, press SELECT. The display prompts with: “Are you sure?”

If you choose **<SELECT>** again, the group variable changes to the group selected. The group variable is only used to change the active setting group if SS1 and SS2 are not asserted or not assigned.

The **<GROUP>** button performs the **GRO** serial port command.

CANCEL

The **<CANCEL>** button returns the display to the previous menu. Use the **<CANCEL>** button to go back after issuing a **<SELECT>**. If there is no previous menu, the default display is shown. If the **<CANCEL>** button is pushed while in the default metering display mode, the relay interprets the button as the **<METER>** button.

SELECT

The **<SELECT>** button is used within dialogues to select a menu choice. Once the choice is identified with the arrow buttons, use the **<SELECT>** button to select that choice. Under the group variable change, you are prompted "Are You Sure?" to change the setting group variable. The **<SELECT>** button accepts the change.

Arrows

The arrow buttons are used throughout the front-panel displays for scrolling through lists of items, identifying menu choices by moving the cursor, and scrolling to the left or right for more information.

EXIT

If you push the **<EXIT>** button at any time within one of the dialogues, the procedure is interrupted, and the display reverts to the default metering display.

Table 9.1: Front-Panel Button Serial Port Equivalents

Button	Similar Serial Port Commands
TARGET RESET	**TAR R**
METER	**MET**
EVENTS	**HIS**, **SER**, **BRE**
STATUS	**STA**
OTHER	**DAT**, **TIM**, **QUI**
SET	**SET**, **SET P**, **SHO**, **SHO P**, **PAS**
CNTRL	**OPE**, **CLO** (default)
GROUP	**GRO**

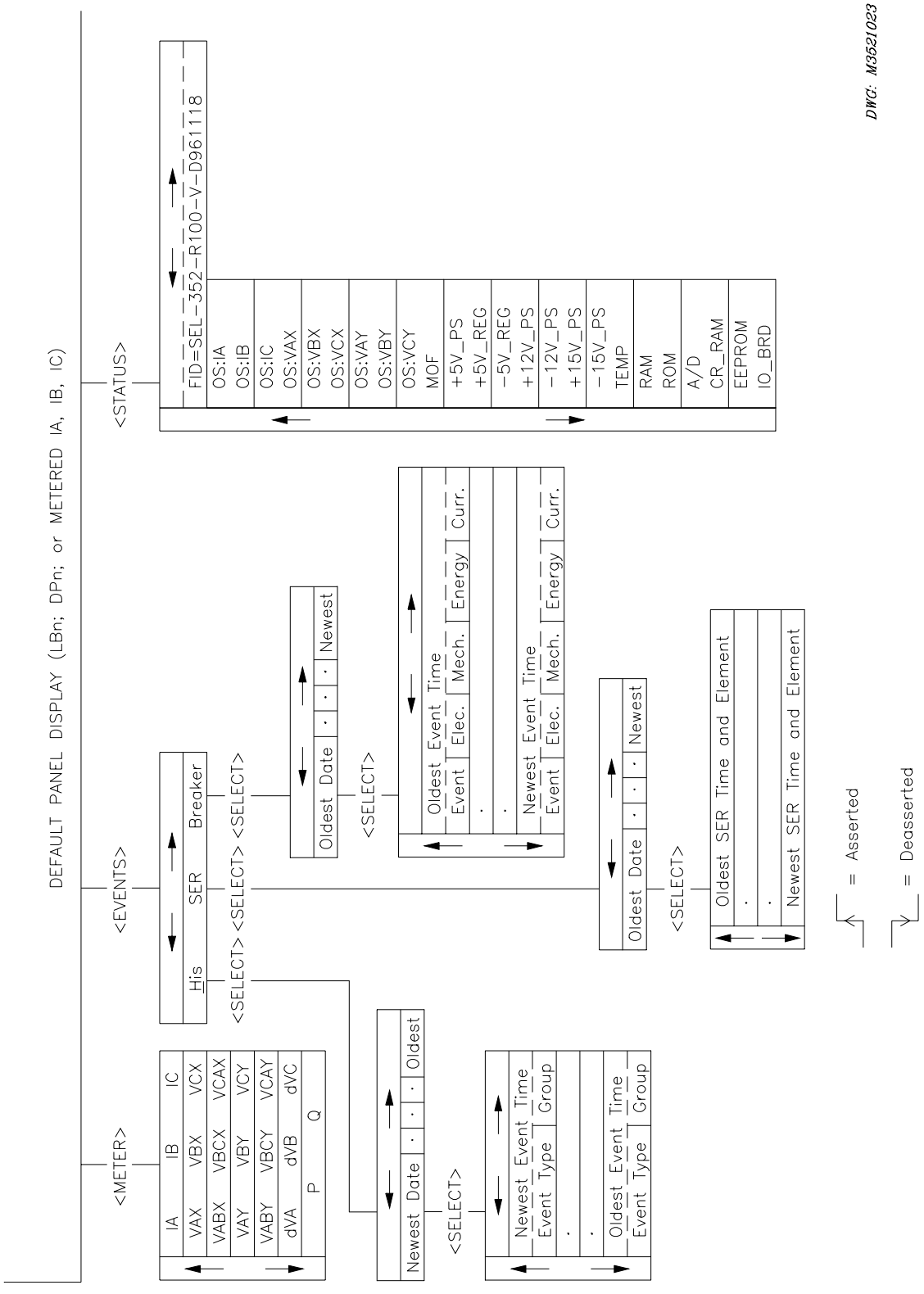


Figure 9.3: Front-Panel Operation Map

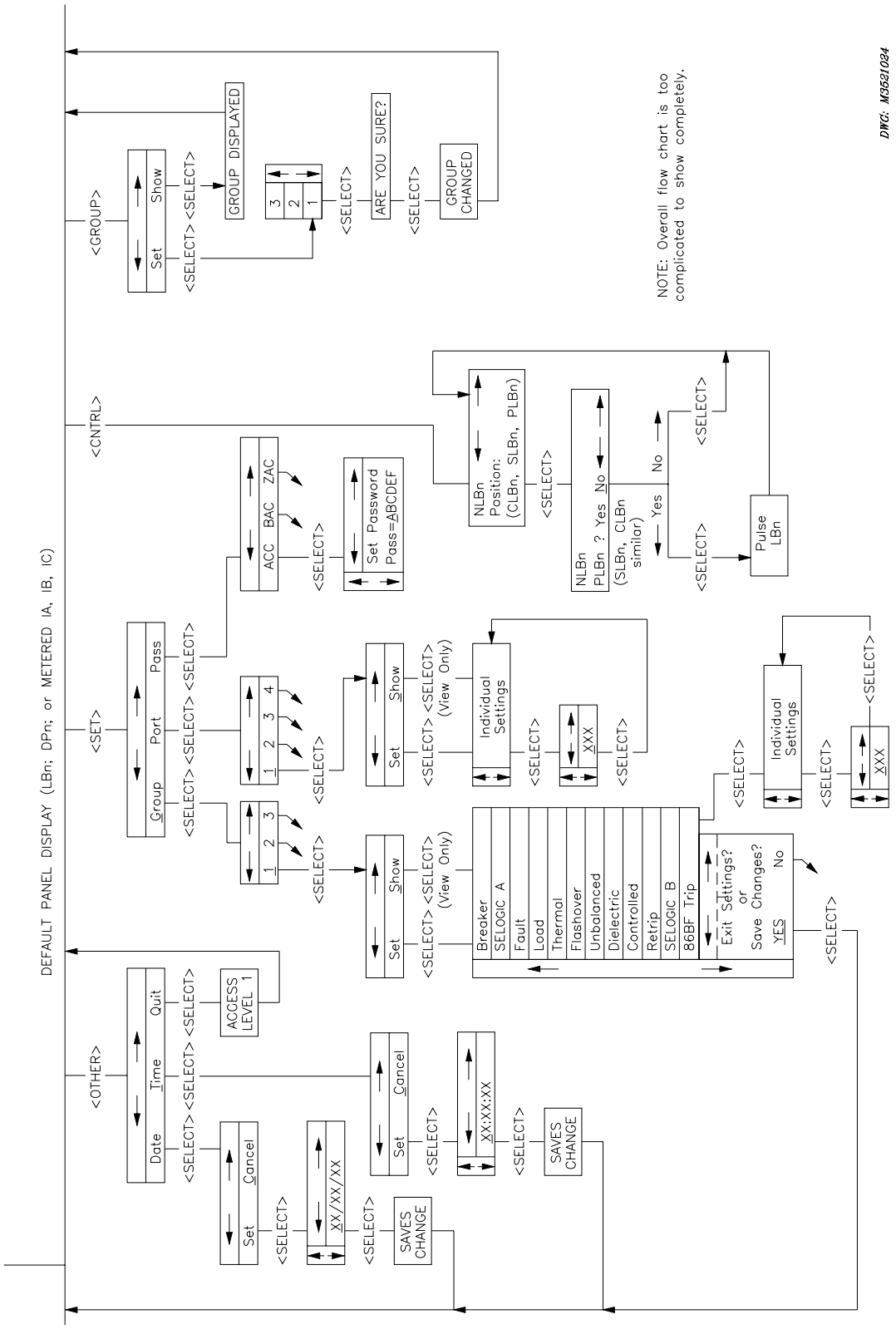


Figure 9.4: Front-Panel Operation Map (Continued)

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SECTION 10: EVENT REPORTS AND SER

INTRODUCTION

Many different settings control the SEL-352 Relay data recording functions. This section discusses the purpose and recommendations for each setting. Use simple three-letter commands with the SEL-352 Relay to access many different reports for viewing power system data:

- 10 seconds of programmable length, selectable resolution, event reports (EVE)
- As many as 40 short summaries of event reports (HIS)
- 512-tow Sequential Events Recorder (SER) report

These reports contain such information as date, time, currents, voltages, differential voltages, resistor thermal conditions, breaker alarms, breaker operations, relay element status, optoisolated input status, output contact status, and relay status.

DATA RECORDING SETTINGS

Global Settings (SET G Command)

LER

The LER setting defines the length of each event report. Set LER to 15, 30, or 60 cycles depending on your application. Use 15 cycles for high-speed breaker failure operations. Use 30 cycles for breaker failure and most closing operations. If your primary application is for synchronism checking or oscillography, use 60 cycles. If your applications are diverse enough to need different lengths, use 60 cycles. You can store as many as ten 60-cycle event reports in nonvolatile memory. The main advantage to using shorter event reports is that you can store more reports.

PRE

The PRE setting is related to the LER setting. It defines the number of cycles in the event report that are pre-event, or pre-trigger. Set PRE within a range from one to LER-1 cycles.

Report Settings (SET R Command)

ALIAS1–ALIAS20

Assign as many as 20 different aliases to Relay Word bits for customizing settings and reports. The following example defines an alias for the 50FT Relay Word bit. Make the assignment by entering the Relay Word bit, followed by a **<SPACE>**, followed by the alias name.

```
ALIAS1 = 50FT FAULT_CURRENT
```

When the 50FT label displays in SELOGIC® control equations or in the SER report, the alias of "FAULT_CURRENT" is used.

Use words common for your company to develop alias names to make your SER report easy to read. Use as many as 15 continuous letters, numbers, and/or the underscore character (no spaces or other characters are allowed). The relay converts all letters to uppercase.

LABEL

The SER report header includes the LABEL setting. As many as 59 keyboard characters can be entered in the LABEL setting. The relay converts all lower-case letters to upper case.

SER1–3

The SER1, SER2, and SER3 settings define what Relay Word bits trigger the SER report. Refer to SER triggering later in this section.

Port Settings (SET P Command)

AUTO

Reports such as short event summaries display automatically for certain conditions. There is an AUTO setting for each serial communications port that determines if these automatic messages display. Refer to ***Automatic Messages*** in ***Section 8: Serial Port Communications and Commands*** for further information on the individual reports. If AUTO is set to "Y" or "YES" for a port, the automatic messages display on that port.

EVENT REPORTS (EVE)

Each triggered event consists of two separate reports. The **EVE** command displays the X-side voltages, currents and standard digitals; the **EVE A** command displays the Y-side voltages and an alternate set of digitals. The header of each event report gives the date and time stamps of the trigger condition and relay identification. Each event report contains unfiltered analog measurements and selected digital relay logic elements. The relay reports event type, system frequency, and voltage nulling calculations just before the settings. A listing of the settings appears at the end of each report for verification.

The relay stores 64 samples per cycle of unfiltered data. Display options allow you to view the event in a 4-, 8-, 16-, or 64-sample per cycle format, and to display 1 to 60 cycles of data depending on the LER setting.

Event Report Triggering

The SEL-352 Relay saves an event report in nonvolatile memory when any of the following occur:

- Relay Word bit 86BFT asserts
- Relay Word bit MER asserts
- You execute the **TRIGGER** command

The relay generates a second event report as a continuation of the first if either of the MER or 86BFT bits did not assert at the time of the first trigger but asserted at the end of the first event report. This function is intended to trigger a second event when the MER generated the first event, but the 86BFT also asserts sometime during the event. In this case, the second event will provide the necessary information to verify bus clearing times.

Relay Word Bit 86BFT

Any assertion of the 86BFT bit triggers an event report. The 86BFT SELOGIC control equation setting controls the 86BFT bit. Use the **SHO A 86BFT <ENTER>** command to view this setting. This setting typically is assigned to the latch output. The latch typically is set to follow the M86T equation, which usually is assigned to the failure output elements of the individual protection logic. The relevant settings for the default relay settings follow:

M86T = FBF + LBF + TTF + CTF + FOBF + UBBF	asserts M86T bit
L3MS = M86T	asserts L3MQ bit
86BFT = L3MQ	asserts 86BFT bit

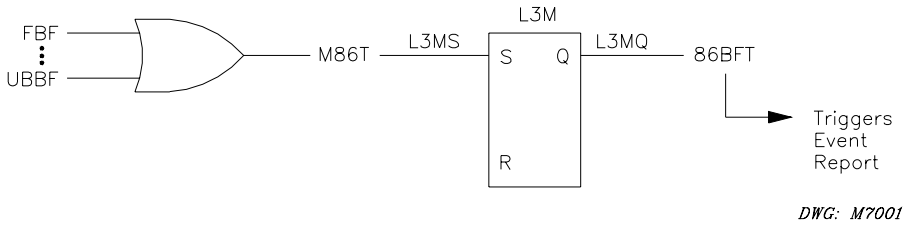

Figure 10.1: Typical 86BFT Assertion

The assertion of Relay Word bit 86BFT automatically triggers an event report.

Triggering of 86BFT is rising-edge sensitive (logical 0 to logical 1 transition). For example, if 86BFT asserts because latch L3MQ is asserted, an event will be triggered. The 86BFT Relay Word bit cannot trigger another event until it deasserts and another rising edge is detected.

Relay Word Bit MER

The MER element is processed every 1/8 cycle. Trigger automatic event reports using the MER SELOGIC control equation setting. The trigger time stamp accuracy is ±2 ms. The MER setting equation controls the MER Relay Word bit. MER is set to trigger event reports for conditions other than 86BFT tripping conditions. The factory settings are:

MER = UBPF + LPF + FOPF + LODPF + TRIPA + TRIPB + TRIPC + CLOSE + MCLOSE + 26CPA + 26CPB + 26CPC + 26TPA + 26TPB + 26TPC + MDT

MER is factory set with pending failure conditions, input conditions, and the MOD trip condition. Thus, when the pending failure condition asserts, an input is received. When the MOD tripping element (MDT) asserts, an event report is triggered.

MER triggering is rising-edge sensitive (logical 0 to logical 1 transition). For example, if a trip input is received (TRIPA logical 0 to logical 1 transition), this receipt of a trip input will trigger an event report. If TRIPA remains asserted and then 26TPA asserts a short time later, assertion of 26TPA will not generate a second report. MER is already at logical 1 because of the initial assertion of TRIPA.

TRIGGER Command

The sole function of the **TRIGGER** command is to generate an event report, primarily for testing purposes. This command will trigger an event report regardless of the state of MER or 86BFT.

Event Report Setup

Event reporting has three user-selectable configurations:

Event Length	# of Events Stored
15 Cycles	40
30 Cycles	20
60 Cycles	10

Each of these configurations provides 10 seconds of total event reports. The longer the event reports, the longer it takes to store and retrieve these reports. Neither of these processes interrupt relay protection operation, but these processes do inhibit serial communications.

Using the **SET G** command, set LER = 15, 30, or 60 to designate the length of each event report that is triggered. Each time the LER setting changes, the events clear, but the relay retains event summaries.

Retrieving Event Reports

The **EVE** command displays an event report. The relay stores latest event reports in nonvolatile memory according to the LER setting. Optional parameters are specified to determine the event displayed and the format in which it will appear.

The entire syntax of the **EVE** command is as follows:

EVE n A Ss Lc<ENTER>

The parameters may be entered in any order after the three-letter command **EVE**, but these parameters must be separated by spaces or commas. The following is a summary of the parameters and some examples:

- n n specifies event number according to the **HIS** command.
- A A specifies the alternate report showing VY (not VX and I).
- Ss Ss specifies the samples per cycle (s = 4, 8, 16, 64).
- Lc Lc specifies the length in cycles (c = 1 to LER setting).

EVE (Defaults)	Display
	Most recent event (EVE 1)
	VX and I analogs, standard digitals
	4 samples per cycle
	All available cycles

EVE A 3 S8	Display
	Event number 3
	VY analogs, alternate digitals
	8 samples per cycle
	All available cycles

EVE S8 L5 10	Display
	Event number 10
	VX and I analogs, standard digitals
	8 samples per cycle
	First 5 cycles of the event

The n parameter specifies the event number to display based on the **HIS** command. The **HIS** command displays an event summary of all of the events stored in memory. Each summary is numbered. The number of event reports stored is dependent on the SET G setting LER.

To select one of the events stored in relay memory, enter the **EVE** command with a number, with 1 being the newest event recorded. If no event report is selected, the relay defaults n = 1 to display the newest event report. Type **EVE 9 <ENTER>** to display event number 9.

Include the A as a parameter to display the alternate Y-side voltages and an alternate set of digital channels. If the A is unspecified, the standard X-side voltages and currents with the standard digitals are displayed.

Specify the number-of-samples-per-cycle resolution of the event with the Ss parameter. The small s can be 4, 8, 16, or 64. If the Ss parameter is unspecified, the relay defaults to S4. The relay stores the event with 64-sample-per-cycle resolution. When displaying the event, select the most appropriate resolution for your application. Some recommendations follow:

- Overview of relay operation: S4 (provides quickest display of general information)
- Diagnostics using digital channels: S8 (the relay processes the digital channels every 1/8-cycle)
- Best resolution for SEL-2020 event storage: S16 (largest event the SEL-2020 can store)
- Detailed analysis of analog channels: S64 (the relay samples analog channels every 1/64-cycle)

Use the Lc parameter to specify the length of the event displayed. The c can be any integer from 1 to LER in cycles. If LER = 30, then L30 is the largest value that may be entered. If the Lc parameter is unspecified, the relay defaults to the LER setting. Any attempt to enter a length

greater than the LER setting will produce an error message. If the LER setting has changed, previous event information is no longer accessible.

Event Report Description

Refer to the example event reports that follow. These example event reports display rows of information each quarter-cycle. Retrieve such reports with the **EVE n** and **EVE A n** commands.

```
=>EVE<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 11/18/96    Time: 14:12:28.257

FID=SEL-352-1-R100-V-D961101

   X VOLTAGES (kV pri)       CURRENTS (pri)                          OUT  IN

                                                                 8    1111 111
                                                      5555XX43 FLLUURM86TC5 0000 000
                                                      00005567 BBPBBTD6BRL2 1357 135
     VAX     VBX     VCX     IA     IB     IC  FLMN99PO FFFBP TRFISA &&&& &&&
                                                 TDD HL P    FF  STP   246A 246

  -220.1   410.3  -167.1   6126    976   -327  .33*.3.. ..........3 .... .45
  -325.3   -36.0   376.1  -4943     21    827  A33*.3.. ..........3 .... .45
   220.5  -409.4   167.7  -6025   -764    382  A33*.3*. ..........3 .... .45
   325.9    36.9  -375.7   5044    187   -764  A33*.3*. ..........3 .... .45

  -219.8   410.3  -167.5   6131    980   -327  A33*.3*. ..........3 .... .45
  -325.5   -35.6   375.9  -4938     25    827  A33*.3*. ..........3 .... .45
   220.2  -409.4   168.0  -6033   -764    382  A33*.3*. ..........3 .... .45
   326.2    36.2  -375.4   5036    182   -768  A33*.3*. ..........3 .... .45

  -219.1   410.4  -168.2   6139    976   -322  A33*.3*. .........A.3 .... 145
  -325.6   -35.4   375.8  -4934     21    827  A33*.3*. .....A...A.3 .... 145
   220.0  -409.4   168.3  -6033   -764    386  A33*.3*. .....A...A.3 .... 145
   326.4    35.7  -375.2   5028    182   -764  A33*.3*. .....A...A.3 .... 145
                          •
                          •  3 cycles of data not shown
                          •
  -217.9   410.5  -169.7   6160    972   -331  A33*.3*. *.*..A..*A.3 B36. 145
  -326.8   -33.1   374.9  -4904     21    823  A33*.3*. *.*..A..*A.3 B36. 145
     0.2     0.4     0.2     47     98     25  .33*.2** ..*..A..*A.3 B36. 145
     0.3     0.5     0.2     51    102     25  .33*..** ..*..A..*A.3 B36. 145

     0.2     0.4     0.2     42     98     21  .23*..** ..*..A..*..3 B36. .4.
     0.2     0.4     0.2     42     98     21  .A2*..** ..*.....*..3 B36. .4.
     0.2     0.4     0.1     47    102     30  ..A....* ..*.....*..3 B36. .4.
     0.3     0.5     0.2     51    106     30  ........ ........*..3 B3.. .4.

     0.3     0.4     0.2     47     98     25  ........ ........*..3 B3.. .4.
     0.2     0.4     0.1     47     98     25  ........ ........*..3 B3.. .4.
     0.3     0.4     0.2     47    102     30  ........ ........*..3 B3.. .4.
     0.3     0.5     0.2     51    102     30  ........ ........*..3 B3.. .4.
                          •
                          •  6 cycles of data not shown
                          •
Event: 86BFT      Frequency (Hz):  60.0

Voltage Nulling Factor     Magnitude     Angle (deg)
Phase A                        1.000         0.000
Phase B                        1.000         0.000
Phase C                        1.000         0.000

Group 1                    Group settings are displayed here (SET, SHO)

Global                     Global settings are displayed here (SET G, SHO G)

SER                        Report settings are displayed here (SET R, SHO R)
```

```
=>EVE A<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 11/18/96    Time: 14:12:28.257

FID=SEL-352-1-R100-V-D961101

   Y VOLTAGES (kV pri)

                                        LL
                           52882224K FFTCCOO
                           97776657T OOTTCDD
     VAY      VBY      VCY  LDTFCTTQR BPFF BP
                           33HOFF  K FF   FF

  -224.3   409.6  -163.6  B........ .......
  -322.7   -41.0   377.6  B........ .......
   224.3  -409.4   163.8  B........ .......
   322.9    41.1  -377.5  B........ .......

  -223.9   409.6  -164.0  B........ .......
  -323.0   -40.5   377.4  B........ .......
   224.1  -409.4   164.1  B........ .......
   323.3    40.5  -377.3  B........ .......

  -223.3   409.7  -164.6  B........ .......
  -323.1   -40.3   377.3  B........ .......
   223.8  -409.4   164.3  B........ .......
   323.6    40.0  -377.1  B........ .......
                           •
                           •  3 cycles of data not shown
                           •
  -222.1   409.8  -166.0  B........ .......
  -324.3   -38.2   376.5  B........ .......
     0.0     0.1     0.0  ..22..... .......
     0.1     0.2     0.0  ..33..... .......

     0.1     0.1     0.0  ..33..... .......
     0.0     0.1     0.0  ..33..... .......
     0.1     0.1     0.0  .Y33..... .......
     0.1     0.2     0.1  .B....... .......

     0.0     0.1     0.0  .B....... .......
     0.0     0.1     0.0  .B....... .......
     0.1     0.1     0.1  .B....... .......
     0.1     0.2     0.1  .B....... .......
                           •
                           •  6 cycles of data not shown
                           •
Event: 86BFT      Frequency (Hz):  60.0

Voltage Nulling Factor     Magnitude     Angle (deg)
Phase A                       1.000         0.000
Phase B                       1.000         0.000
Phase C                       1.000         0.000

Group 1                    Group settings are displayed here (SET, SHO)

Global                     Global settings are displayed here (SET G, SHO G)

SER                        Report settings are displayed here (SET R, SHO R)
```

Each event consists of the following:

- Heading
- Columns of data displayed according to the **EVE** command parameters
- Event type
- Frequency tracking
- Voltage nulling values
- Settings, if they have not changed since the event

The columns contain voltage, current, element, input, and output information. The voltage and current columns show unfiltered instantaneous samples of the analog value scaled in primary amperes and kilovolts. The other columns show a number, letter, or symbol to indicate the condition of the elements, inputs, and outputs.

A "greater than" (>) symbol appears next to the sampled row where the event report triggered for the 8-, 16-, and 64-sample-per-cycle reports, between the analog columns and the digital columns. It does not display for the 4-samples-per-cycle reports because triggering resolution is better than the 4-samples-per-cycle display. At the time of trigger, the relay records date and time, the frequency tracking, and the voltage nulling values. The event type is based on elements that pick up any time during the event.

Heading

Each event report begins with information about the relay and the event. The TRMID setting is displayed so the event can be easily identified with the terminal the relay is monitoring. The FID string identifies the relay model, flash firmware version, and the date code of the firmware. Refer to ***Appendix A: Firmware Versions in This Manual*** for a description of the FID string. A date and time stamp indicates the time that the event report triggered according to the internal clock. You can connect the internal clock to an external IRIG-B time synchronization source.

The event report column labels follow the event identification information. The element and digital information labels are single-character columns. Read these from top to bottom. The following section explains these columns of data.

Data Columns

The analog columns show unfiltered sampled voltage and current in primary kilovolts and amperes, respectively. The values are scaled to an RMS value. Multiply by $\sqrt{2}$ to obtain the actual instantaneous values. The digital columns show relay elements, outputs, and inputs. The column headings, data symbols, and descriptions are listed in Table 10.1 and Table 10.2.

Table 10.1: Event Report Columns (EVENT n Command)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
VAX			A-phase, X-side unfiltered analog voltage
VBX			B-phase, X-side unfiltered analog voltage
VCX			C-phase, X-side unfiltered analog voltage
IA			A-phase unfiltered analog current
IB			B-phase unfiltered analog current
IC			C-phase unfiltered analog current
All digital columns		.	Element/input/output not picked up or not asserted, unless otherwise stated
50FT 50LD 50MD	50FTA, 50FTB, 50FTC 50LDA, 50LDB, 50LDC 50MDA, 50MDB, 50MDC	A B C 2 3	A-phase overcurrent element picked up B-phase overcurrent element picked up C-phase overcurrent element picked up Two overcurrent elements picked up Three overcurrent elements picked up
50N	50N	*	Residual overcurrent element picked up
X59H X59L	X59HA, X59HB, X59HC X59LA, X59LB, X59LC	A B C 2 3	A-phase overvoltage element picked up B-phase overvoltage element picked up C-phase overvoltage element picked up Two phase overvoltage elements picked up All three-phase overvoltage elements picked up
46P	46P	*	Current unbalance element picked up
37OP	37OP	*	Overpower element picked up
FBF LBF LPF UBBF UBPF	FBF LBF LPF UBBF UBPF	*	Failure or pending failure asserted
RT	RTA, RTB, RTC	A B C 2 3	A-phase retrip element asserted B-phase retrip element asserted C-phase retrip element asserted Two retrip elements asserted All three retrip elements asserted
MDT	MDT	*	Motor operated disconnect trip element asserted
86RS	86RS	*	Lockout relay reset element asserted
86BFT	86BFT	*	Lockout relay trip element asserted

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
TRIP	TRIPA, TRIPB, TRIPC	A B C 2 3	A-phase trip element asserted B-phase trip element asserted C-phase trip element asserted Two trip elements asserted All three trip elements asserted
CLS	CLOSE, MCLOSE	C M B	CLOSE element asserted MCLOSE element asserted Both CLOSE and MCLOSE asserted
52A	52AA, 52AB, 52AC	A B C 2 3	A-phase breaker auxiliary input element asserted B-phase breaker auxiliary input element asserted C-phase breaker auxiliary input element asserted Two breaker auxiliary input elements asserted Three breaker auxiliary input elements asserted
OUT 101&2	OUT101, OUT102	1 2 B	Output contact OUT101 asserted Output contact OUT102 asserted Both OUT101 and OUT102 asserted
OUT 103&4	OUT103, OUT104	3 4 B	Output contact OUT103 asserted Output contact OUT104 asserted Both OUT103 and OUT104 asserted
OUT 105&6	OUT105, OUT106	5 6 B	Output contact OUT105 asserted Output contact OUT106 asserted Both OUT105 and OUT106 asserted
OUT 107&A	OUT107, ALARM	7 A B	Output contact OUT107 asserted ALARM output contact asserted Both OUT107 and ALARM asserted
IN 101&2	IN101, IN102	1 2 B	Optoisolated input IN101 asserted Optoisolated input IN102 asserted Both IN101 and IN102 asserted
IN 103&4	IN103, IN104	3 4 B	Optoisolated input IN103 asserted Optoisolated input IN104 asserted Both IN103 and IN104 asserted
IN 105&6	IN105, IN106	5 6 B	Optoisolated input IN105 asserted Optoisolated input IN106 asserted Both IN105 and IN106 asserted

Table 10.2: Event Report Columns (EVENT A n Command)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
VAY			A-phase, Y-side unfiltered analog voltage
VBY			B-phase, Y-side unfiltered analog voltage
VCY			C-phase, Y-side unfiltered analog voltage
All digital columns		.	Element/input/output not picked up or not asserted, unless otherwise stated
59L3	X59L3, Y59L3	X	All three X-side phase overvoltage elements picked up
		Y	All three Y-side phase overvoltage elements picked up
		B	All three phase overvoltage elements picked up for both the X and Y side
27D3	X27D3, Y27D3	X	All three X-side phase undervoltage elements picked up
		Y	All three Y-side phase undervoltage elements picked up
		B	All three phase undervoltage elements picked up for both the X and Y side
87TH	87THA, 87THB, 87THC	A	A-phase voltage differential element picked up
87FO	87FOA, 87FOB, 87FOC	B	B-phase voltage differential element picked up
		C	C-phase voltage differential element picked up
		2	Two voltage differential elements picked up
		3	Three voltage differential elements picked up
26CF	26CFA, 26CFB, 26CFC	A	A-phase close or trip resistor thermal failure element asserted
26TF	26TFA, 26TFB, 26TFC	B	B-phase close or trip resistor thermal failure element asserted
		C	C-phase close or trip resistor thermal failure element asserted
		2	Two thermal elements picked up
		3	Three thermal elements picked up
25T	25T	*	Synchronism checking element picked up
47Q	47Q	*	Negative-sequence overvoltage (V_2) element picked up (47Q=X47Q+Y47Q)

Column Heading	Corresponding Elements (Relay Word Bits)	Symbol	Definition
KTRK	KTRK	*	Voltage nulling tracking enable element asserted
FOBF FOPF TTF CTF	FOBF FOPF TTF CTF	*	Failure or pending failure elements asserted
CC	CCA, CCB, CCC	A B C 2 3	A-phase close output element asserted B-phase close output element asserted C-phase close output element asserted Two close output elements asserted All three close output elements asserted
LODBF LODPF	LODBF LODPF	*	Loss-of-dielectric failure or pending failure elements asserted

Event Type

The "Event" field shows the event type. Determination of event type depends upon the bits that assert any time during the event report. The conditions that determine the possible event types are shown in Table 10.3. If more than one condition asserts during the event, the relay reports the event type listed first (higher in the table).

Table 10.3: Event Types

Event	Event Triggered by:
86BFT	Assertion of Relay Word bit 86BFT
TRIP3	Assertion of all Relay Word bits TRIPA, TRIPB, and TRIPC
TRIPAB	Assertion of Relay Word bits TRIPA and TRIPB
TRIPBC	Assertion of Relay Word bits TRIPB and TRIPC
TRIPCA	Assertion of Relay Word bits TRIPC and TRIPA
TRIPA	Assertion of Relay Word bit TRIPA
TRIPB	Assertion of Relay Word bit TRIPB
TRIPC	Assertion of Relay Word bit TRIPC
CLOSE	Assertion of Relay Word bit CLOSE or MCLOSE
INT	Assertion of Relay Word bit MER or execution of **TRIGGER** command

Frequency Tracking

At the time of event report trigger, the relay records the tracking frequency of the relay. This frequency value does not correspond to the synchronism checking elements. This frequency is the value that the relay processor tracks. The tracking frequency follows the A-phase voltage frequency of the voltage source that is greater than the 59L setting. If both X- and Y-voltage sources satisfy this criterion, the relay calculates an average.

Voltage Nulling Factor

At the time of event report trigger, the relay records voltage nulling factors. The relay reports magnitude (in per unit) and angle (in degrees) of the voltage nulling factor for each phase. After a settable time delay (VNpu), the SEL-352 Relay determines the appropriate multiplication factor for the X voltages to null any steady-state difference between the X and Y potential transformers.

History of Event Reports

Each time the relay generates an event report, it also generates a corresponding event summary. Event summaries as displayed by the **HIS** command contain the following information:

- Event number at the time the **HIS** command was issued
- Date and time when the event was triggered
- Event type
- Setting group the relay was using at the time of trigger

```
=>HIS<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 09/04/96    Time: 20:53:30.788

#      DATE         TIME        EVENT    GROUP

1    09/04/96   20:53:18.617   INT        1
2    09/04/96   20:46:14.617   TRIPA      1

=>
```

The relay stores as many as 40 of the latest 40 event summaries in nonvolatile memory. These event summaries correspond to the latest event reports stored in nonvolatile memory according to the LER setting.

Clearing Event Report Buffer

The **HIS C** command clears the event summaries and corresponding event reports from nonvolatile memory. The clearing process may take as long as 30 seconds under normal operation. This process may be even longer if the relay is busy processing a fault or other protection logic.

Automated clearing of the event buffer should be limited to reduce the possibility of wearing out the nonvolatile memory. Limit automated **HIS C** commands to once per week or less.

SEQUENTIAL EVENTS RECORDER (SER) REPORT

A sequential events recorder provides a chronological record of relay decisions, operations, and external connections. Use the SER for testing and quick operation reviews.

SER Report Row Triggering

The relay triggers (generates) a row in the SER event report for any change of state in any one of the bits listed in the SER1, SER2, and SER3 trigger settings. The relay looks at each Relay Word bit individually to see if it asserts or deasserts. Any assertion or deassertion of a listed bit triggers a row in the SER event report.

SER Report Trigger Settings

Set any SER trigger setting (SER1, SER2, or SER3) with as many as 24 Relay Word bits. You can, therefore, monitor as many as 72 elements altogether for SER event report triggering. Three SER settings are provided to separate the long list of bits for easier editing. All three settings perform the same function.

The SER1, SER2, and SER3 elements are processed every 1/8 cycle. Trigger a sequential events record using these three SELOGIC control equation settings. The time-stamp accuracy of the record is ±ms.

In developing SER settings, use spaces as delimiters between elements. For example, to trigger the SER for all breaker auxiliary status changes, set SER1 as follows:

```
SER1 = 52AA 52AB 52AC
```

When setting the SER equations consider the following:

- Put similar Relay Word bits in the same SER setting for easier editing
- Only select bits that are part of the enabled logic
- Do not use redundant bits such as IN104 and 52AA when 52AA = IN104
- Output contacts (i.e., OUT101) cannot be put in MER but can be put in the SERs
- Use the SER for testing
- Reset the SER after testing (SER C)

Retrieving SER Report

The relay stores the latest 512 rows of the SER event report in nonvolatile memory. Row 1 is the oldest row, and the greatest row number is the most recent SER trigger. You can access these lines with the **SER** command as follows:

Example SER Serial Port Commands	Format
SER	If **SER** is entered without dates, all available rows are displayed (up to row number 512). They display with the oldest row (Row 1) at the beginning (top) of the report and the latest row (up to 512) at the end (bottom) of the report. Chronological progression is down the page and in ascending row number.
SER 3/30/96	If **SER** is entered with one date (date 3/30/96 in this example), all the rows on that date or later are displayed, if they exist. They display with the earliest row at the beginning (top) of the report and the latest row at the end (bottom) of the report. Chronological progression is down the page and in ascending row number.
SER 2/17/96 3/23/96	If **SER** is entered with two dates, all the rows between (and including) dates 2/17/96 and 3/23/96 are displayed, if they exist. They display with the earliest row (date 2/17/96) at the beginning (top) of the report and the latest row (date 3/23/96) at the end (bottom) of the report. Chronological progression is down the page and in ascending row number.

The date entries in the above example **SER** commands are dependent on the date format setting DATE_F. If setting DATE_F = MDY, then the dates are entered as described above (Month/Day/Year). If setting DATE_F = YMD, then the dates are entered Year/Month/Day.

Clearing the SER Report

The **SER C** command clears the SER report from nonvolatile memory. The clearing process may take up to 30 seconds under normal operation. It may be even longer if the relay is busy processing a fault or other protection logic.

Automated clearing of the SER buffer should be limited to reduce the possibility of wearing out the nonvolatile memory. Limit automated **SER C** commands to once per week or less.

SER Report Headings

The TRMID setting, date and time the SER report was displayed, the relay identification string, and the LABEL setting are all displayed in the SER header.

SER Report Column Definitions

Refer to the example SER event report that follows to view SER event report columns. Each row in the SER event report contains date, time, Relay Word bit name or alias, and the state of the bit.

```
=>SER<ENTER>
EXAMPLE CIRCUIT BREAKER              Date: 09/26/96    Time: 13:22:35.297

FID=SEL-352-1-R100-D960828

Example Report Label

#      DATE         TIME           ELEMENT          STATE

1    09/26/96   13:22:04.004   50FAULT            Asserted
2    09/26/96   13:22:04.033   TRIP               Asserted
3    09/26/96   13:22:04.050   RETRIP             Asserted
4    09/26/96   13:22:04.100   BFR_TRIP           Asserted
5    09/26/96   13:22:04.116   TRIP               Deasserted
6    09/26/96   13:22:04.125   50FAULT            Deasserted
7    09/26/96   13:22:04.195   RETRIP             Deasserted
8    09/26/96   13:22:14.097   MOD_TRIP           Asserted
9    09/26/96   13:22:24.097   BFR_TRIP           Deasserted
10   09/26/96   13:22:29.096   BFR_RESET          Asserted
11   09/26/96   13:22:30.097   MOD_TRIP           Deasserted
12   09/26/96   13:22:30.097   BFR_RESET          Deasserted
```

Date and Time

The date and time displayed in the SER are the time the Relay Word bit changed state. The time stamp is accurate to within ±1 ms.

Element

The Relay Word bit name or alias is listed under the element column. The Relay Word bit name is normally displayed when it is in the SER setting and it changes state. If an alias is defined by the ALIAS settings using the **SET R** command, then the alias will display in place of the Relay Word bit name.

State

The state of the Relay Word bit displays as either “Asserted” or “Deasserted”. If the bit transitions from a logical 0 to a logical 1, then “Asserted” is displayed. If the bit transitions from a logical 1 to a logical 0, then “Deasserted” is displayed.

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FIGURES

SECTION 11: TESTING AND TROUBLESHOOTING

TEST PROCEDURES

Test Aids Provided by the Relay

The following features assist you during relay testing and calibration:

METER Command	The **MET** command shows the voltages and currents presented to the relay in primary values. The relay calculates megawatts (MW) and megavars (MVAR) from these voltages and currents. These quantities are useful for comparing relay calibration against other meters of known accuracy.
TARGET, **TARGET F**, Commands	Use the **TAR** command to display certain Relay Word bits' status on the terminal screen. Use the **TAR F** command to reassign the bottom row of front-panel target LEDs to display certain Relay Word bits. The target LEDs will pick up and drop out in the same manner that the Relay Word bit operates.
EVENT, **EVENT A**, Commands	The relay generates a 15-, 30-, or 60-cycle event report (LER setting) in response to assertion of the 86BFT element or selected triggering conditions specified in the MER SELOGIC® control equation setting. Each event report contains analog and digital information for analyzing the relay operations. View the standard and alternate event reports using the **EVE** and **EVE A** commands.
Programmable Outputs	Programmable outputs allow you to isolate individual relay elements. See the **SET** command in ***Section 8: Serial Port Communications and Commands***.
SER Command	Use the Sequential Event Recorder for timing tests by setting the SER trigger settings (SER1, SER2, or SER3) to trigger for specific elements asserting or deasserting. View the SER with the **SER** command.

Test Methods

There are three means of determining the pickup and dropout of relay elements: target LED illumination, output contact operation, and the sequential event recorder (SER).

Target LED Illumination

During testing, use target LED illumination to determine relay element status. Using the **TAR F** command, set the front-panel targets to display the element under test. Monitor element pickup and dropout by observing the target LEDs.

For example, the fault level overcurrent element 50FT appears in Relay Word Row 8. When you type the command **TAR F 50FT <ENTER>**, the terminal displays the labels and status for each bit in the Relay Word Row (8), and the LEDs display their status. Thus, with these new targets

displayed, if the fault level overcurrent element (50FT) asserts, the far right LED illuminates. See ***Appendix F: Relay Word*** for a list of all Relay Word elements.

Be sure to reset the front-panel targets to the default targets after testing before returning the relay to service. This can be done by pressing the front-panel **<TARGET RESET>** button or by issuing the **TAR R** command from the serial port.

Output Contact Assertion

To test using this method, set one programmable output contact to assert when the element under test picks up. With the **SET n** command, enter the Relay Word bit name of the element under test.

For an "a" contact, when the condition asserts, the output contact closes. When the condition deasserts, the output contact opens.

For a "b" contact, when the condition asserts, the output contact opens. When the condition deasserts, the output contact closes.

Programmable contacts can be changed to "a" or "b" contacts with a solder jumper. Refer to ***Section 2: Installation*** for jumper locations. Using contact operation as an indicator, you can measure element operating characteristics, stop timers, etc.

Tests in this section assume an "a" output contact.

Sequential Events Recorder (SER)

To test using this method, set the SER to trigger for the element under test. Using the **SET R** command, put the element name in the SER1, SER2, or SER3 setting.

Whenever an element asserts or deasserts, a time stamp is recorded. View the SER report with the **SER** command. Clear the SER report with the **SER C** command.

Low-Level Test Interface

The SEL-352 Relay has a low-level test interface between the calibrated input module and the separately calibrated processing module. You may test the relay in either of two ways: conventionally, by applying ac current signals to the relay inputs; or by applying low magnitude ac voltage signals to the low-level test interface. Access the test interface by removing the relay front panel.

Figure 11.1 shows the low-level interface connections. This drawing also appears on the inside of the relay front panel. Remove the ribbon cable between the two modules to access the outputs of the input module and the inputs to the processing module (relay main board).

You can test the relay processing module using signals from the SEL-RTS Low-Level Relay Test System. Never apply voltage signals greater than 9 V peak-to-peak to the low-level test interface. Figure 11.1 shows the signal scaling factors.

CAUTION

The relay contains devices that are sensitive to electrostatic discharge (ESD). When working on the relay with front or top cover removed, work surfaces and personnel must be properly grounded or equipment damage may result.

You can test the input module two different ways:

Measure the outputs from the input module with an accurate voltmeter, and compare the readings to accurate instruments in the relay input circuits,

or

Replace the ribbon cable, press the front-panel **<METER>** button, and compare the relay readings to other accurate instruments in the relay input circuits.

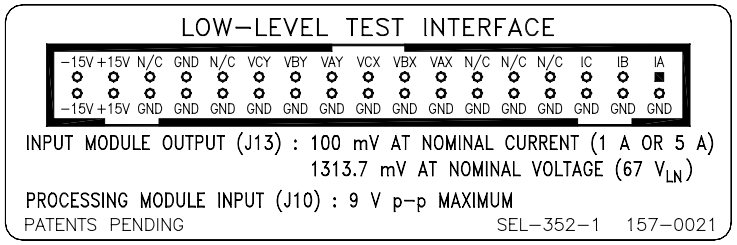


Figure 11.1: Low-Level Test Interface

INITIAL CHECKOUT

You should familiarize yourself with the relay and make certain that all functions are operational during the initial checkout procedure. For a complete understanding of the relay's capabilities, refer to the individual sections within the rest of the instruction manual.

Equipment Required

The following equipment is necessary for initial checkout:

1. A terminal or computer with terminal emulation with EIA-232 serial interface
2. Interconnecting data cable between terminal and relay
3. Source of relay control power
4. Source of three-phase voltages and at least two currents
5. Ohmmeter or contact opening/closing sensing device

Checkout Procedure

In the procedure below, you will use several relay commands. ***Section 8: Serial Port Communications and Commands*** provides a full explanation of all commands. However, the following information should allow you to complete the checkout without referring to the detailed descriptions.

Note: In this manual, commands to type appear in bold/upper case: **SET**. Terminal keys or relay front-panel buttons to press appear in bold/upper case/brackets: **<ENTER>, <TARGET RESET>**

The following format represents relay output on your terminal screen.

```
Example 500 kV Line                    Date: 6/1/96    Time: 01:01:01
```

Step 1. Purpose: Be sure you received the relay in satisfactory condition.

Method: Inspect the instrument for physical damage such as dents or rattles.

Step 2. Purpose: Verify requirements for relay logic inputs, control power voltage level, and voltage and current inputs.

Method: Refer to the information sticker on the rear panel of the relay. Figure 11.2 provides an example. Check the information on this sticker before applying power to the relay or starting tests. Be sure your dc supply is correctly adjusted for the control and logic input requirements.

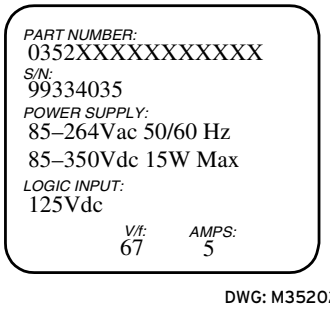


Figure 11.2: Relay Part Number and Hardware Identification Sticker

Step 3. Purpose: Verify the communications interface setup.

Method: Connect a computer terminal to Port 2, 3, or 4 of the relay.

Communication Parameters: 2400 Baud, 8 Data Bits, 1 Stop Bit, N Parity

Cables: SEL-C234A for 9-pin male computer connections
SEL-C227A for 25-pin male computer connections

Step 4. Purpose: Establish control power connections.

Method: Connect a frame ground to terminal marked GND on the rear panel and connect rated control power to terminals marked + and –. Relays supplied with 125 or 250 V power supplies may be powered from a 115 Vac wall receptacle for testing.

Step 5. Purpose: Apply control voltage to the relay, and start Access Level 0 communications.

Method: Turn on the relay power. The enable target (EN) LED should illuminate. If not, be sure that power is present. Type <ENTER> from your terminal

to get the Access Level 0 response from the relay. The = prompt should appear, indicating that you have established communications at Access Level 0.
The ALARM relay should pull in, holding its "b" contacts open.

If the relays pull in, but your terminal does not respond with the equals sign, check the terminal configuration. If neither occurs, turn off the power, and refer to the Troubleshooting Guide later in this section.

The = prompt indicates that communications with the relay are at Access Level 0, the first of four possible levels. The only command accepted at this level is **ACC <ENTER>**, which opens communications on Access Level 1.

Note: If you are using a battery simulator, be sure the simulator voltage level is stabilized before turning the relay on.

Step 6. Purpose: Establish Access Level 1 communications.

Method: Type **ACC <ENTER>**. At the prompt, enter the Access Level 1 password and press **<ENTER>**. (See ***PAS (Passwords)*** in ***Section 8: Serial Port Communications and Commands*** for factory default passwords.) The => prompt should appear, indicating that you have established communications at Access Level 1.

Step 7. Purpose: Verify relay self-test status.

Method: Type **STA <ENTER>**. The following display should appear on the terminal:

```
=>STA<ENTER>

EXAMPLE CIRCUIT BREAKER               Date: 01/01/96    Time: 14:52:30.997

FID=SEL-352-1-R100-D960612
SELF TESTS

W=Warn    F=Fail

        IA       IB       IC       VAX      VBX      VCX
OS      -1        4       -1       -4       -4       -4

        VAY      VBY      VCY      MOF
OS      -4       -4       -4        1

        +5V_PS   +5V_REG  -5V_REG  +12V_PS  -12V_PS  +15V_PS  -15V_PS
PS       4.90     5.00    -5.04     12.06   -12.25    14.89   -15.05

        TEMP     RAM      ROM      A/D      CR_RAM   EEPROM   IO_BRD
         29.8    OK       OK       OK       OK       OK       OK

 Relay Enabled

=>
```

Step 8. Purpose: View factory settings entered before shipment.

Method: The relay is shipped with factory settings; type **SHOWSET <ENTER>** to view the settings. The terminal display should look similar to the following:

```
=>SHO<ENTER>
Group 1

RELID  =EXAMPLE SEL-352-1
TRMID  =EXAMPLE CIRCUIT BREAKER
Topen  = 33       Tclose = 66       SlowTr = 42.0      SlowCl = 83.0
CTR    = 600.0    XPTR   = 4300.0   YPTR   = 4300.0

SALOG  = OFF

50FT   = 8.60     FTLOG  = 2
FCpu   = 4.000

50LD   = 0.50     50N    = 0.50     LDLOG  = 1
LPpu   = 3.25     LDpu   = 5.50

37OP   = 2.07     47Q    = 18.7     87TH   = 4.3
VNpu   = 10.00    Kmag   = 5.0      Kang   = 10.0      THLOG  = ON
OPpu   = 3.00
26CP   = 1.11     26CF   = 1.45     26TP   = 3.49      26TF   = 4.56
CRTC   = 80       TRTC   = 80

87H    = 57.0     87F0   = 4.0      59H    = 100.0     FOLOG  = 1
FPpu   = 25.00    FFpu   = 30.00

46UB   = 16       UBLOG  = ON
UCpu   = 6.00     UPpu   = 50.00    UFpu   = 60.00

DELOG  = OFF

59L    = 57.0     27D    = 10.0     CLSLOG = 1        CLSdo   = 5.00
RCApu  = 0.00     RCBpu  = 0.00     RCCpu  = 0.00

RTPLOG = 1

SBLOG  = OFF

M86T   =FBF + LBF + TTF + CTF + FOBF + UBBF
50MD   = 0.10     TRLOG  = 2
M2pu   = 600.000  M3pu   = 600.000

MER    =UBPF + LPF + FOPF + LODPF + TRIPA + TRIPB + TRIPC +
        CLOSE + MCLOSE + 26CPA + 26CPB + 26CPC + 26TPA + 26TPB +
        26TPC + MDT

OUT101 =86BFT
OUT102 =86BFT
OUT103 =BALRM
OUT104 =!50MNA*!50MNB*!50MNC*!52AA*!52AB*!52AC
OUT105 =MDT
OUT106 =LPF + FOPF + UBPF
OUT107 =86RS

DP1    =IN104
DP2    =0
DP3    =0
DP4    =0
DP5    =0
DP6    =0
DP7    =0
DP8    =0
DP9    =0
DP10   =0
DP11   =0
DP12   =0
DP13   =0
DP14   =0
DP15   =0
DP16   =0
```

Section 7: Setting the Relay includes a complete description of the settings.

Step 9. Purpose: Connect simulated power system secondary voltages to the relay.

Method: Turn power off, and connect a source of three-phase voltages to the X and Y voltage inputs. Parallel the voltage connections by connecting to the relay at terminals marked VAX and VAY, VBX and VBY, and VCX and VCY. Connect the voltage neutral lead to terminals marked VNX and VNY. Apply 67 volts per phase (line-to-neutral) in positive-sequence rotation. Refer to Figure 11.3 and Figure 11.4 for connection diagrams.

Step 10. Purpose: Verify correct voltage levels.

Method: Turn on the relay, and use the **ACCESS** command to reach Access Level 1. Use the **METER** command to measure the voltages applied in Step 9. With applied voltages of 67 V per phase and a potential transformer ratio of 4300:1 (**SHO XPTR <ENTER>** displays the PT ratios, **<CTRL> X** cancels scrolling), the displayed line-to-neutral voltages should be 288 kV. Current readings should all be zero. All line-to-line quantities should be balanced, differing from the line-to-neutral measurements by a factor of 1.73. Real power P and reactive power Q should be approximately 0. When finished, turn off the simulated power system secondary voltage sources.

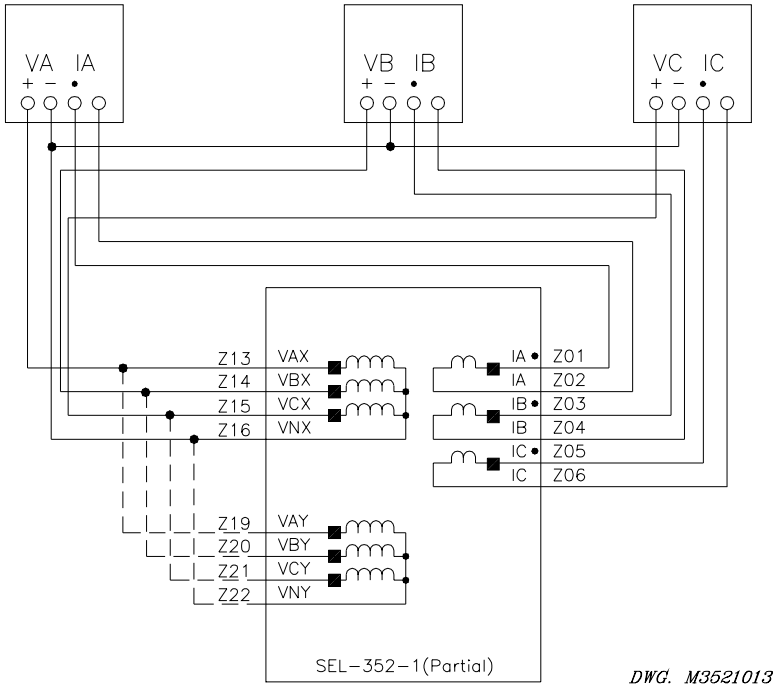


Figure 11.3: Test Connections With Three-Phase Voltage and Three-Phase Current Sources

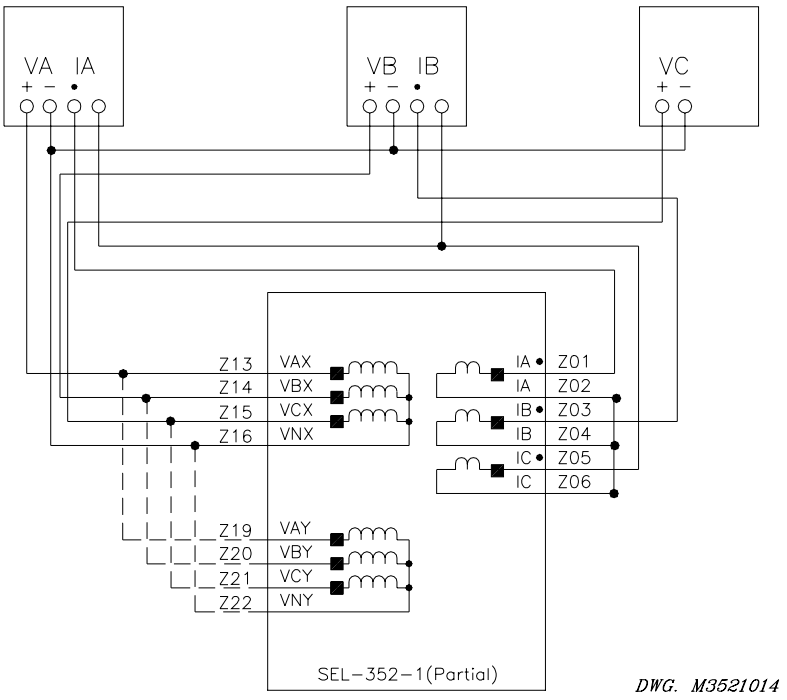


Figure 11.4: Test Connections With Three-Phase Voltage and Two-Phase Current Sources

Step 11. Purpose: Connect simulated power system secondary current sources to the relay.

Method: Turn power off to the relay and connect current sources. If three current sources are available, connect them to the relay in four-wire wye, as shown in Figure 11.3. If only two current sources are available, wye-connect the sources as shown in Figure 11.4 to generate balanced positive-sequence currents:

a. Connect the A-phase and B-phase current sources to the dotted A and B current input terminals.

b. Connect both undotted A and B current input terminals to the undotted C current input terminal.

c. Connect the dotted C current input terminal to both the A and B current source returns.

Set the current sources to deliver one ampere at the same angle as their corresponding phase voltages.

Step 12. Purpose: Verify correct current levels.

Method: Turn relay power on, and use the **METER** command to measure the currents applied in Step 11. With applied currents of one ampere per phase and a current transformer ratio of 600:1 (**SHO CTR <ENTER>** displays the CT ratio, **<CTRL> X** cancels scrolling), the displayed

line-to-neutral currents should be 600 amperes. All line-to-line quantities should be balanced, differing from the line-to-neutral measurements by a factor of 1.73. Real power P and reactive power Q should be approximately 0.

Step 13. Purpose: Verify current and voltage connections.

Method: Reduce the current source output to 0.40 A per phase. Set the voltage source outputs to deliver 5 V per phase, balanced voltages, in phase with the currents applied. Turn on the voltage sources. Execute the **METER** command. Verify the voltage and current magnitudes, recalling the relay PTR and CTR settings. Power P should read approximately 15 MW; Q should read approximately 0 MVAR. If you inadvertently switch a pair of voltages or currents or roll the polarity of a current input, the meter reading should be incorrect. Turn the voltage and current sources off.

Step 14. Purpose: Verify that logic inputs assert when control voltage is applied across the respective terminal pair.

Method:

1. Set the target LEDs to display the contact inputs by typing **TARGET F IN101 <ENTER>**. The bottom row of the front-panel LEDs should now follow contact inputs IN101 through IN106, which is Relay Word Row 17.
2. Apply control voltage to each input and make sure the corresponding target LED turns on.
3. Repeat this step for each input. Use the **TARGET F** command to display the appropriate input elements. For example, to see the row of the Relay Word that has IN301, type **TAR F IN301<ENTER>**. The relay will not display input elements that your interface board does not support.

Step 15. Purpose: Verify that contact outputs assert when you execute the **PULSE** command.

Method:

1. Set the target LEDs to display the contact outputs by typing **TAR F OUT101 <ENTER>**. The front-panel LEDs should now follow Row 73 of the Relay Word where OUT101 is listed.
2. Execute the **PULSE n** command for each output contact. Verify that the corresponding target LED illuminates and output contact closes for approximately one second. For example, type **PUL OUT101 <ENTER>** to test output contact 101.
3. Repeat this step for each output. Use the **TARGET F** command to display the appropriate output elements. For example, to see the row of the Relay Word that has OUT301, type **TAR F OUT301 <ENTER>**. The relay will not display output elements that your interface board does not support.

Step 16. Purpose: Verify the 87H element pickup, the 50LDA element pickup, and the flashover detection logic.

Method:

1. Verify the 87H, 50LD, and FFpu settings by typing **SHO 87H <ENTER>**, **SHO 50LD <ENTER>** and **SHO FFpu <ENTER>. <CTRL X>** cancels the scrolling after each command.
2. Remove the parallel connection of the X and Y voltage inputs to the relay. These are shown in Figure 11.3 and Figure 11.4 as dotted lines.
3. Set the target LEDs to display the high set differential voltage condition by typing **TARGET F 87H <ENTER>**. The front-panel LEDs should now follow Row 7 of the Relay Word where 87H is listed.
4. Increase A-phase voltage until the 87H LED illuminates. This should occur when the voltage reaches the 87H setting. Leave the voltage 10 V higher than this level.
5. Set the target LEDs to display the load condition overcurrent element by typing **TAR F 50LD <ENTER>**. The front-panel LEDs should now follow Row 8 of the Relay Word where 50LD is listed.
6. Increase A-phase current until the 50LD LED illuminates without flashing. This should occur when the current reaches the 50LD setting. Now remove the current from the relay, but leave the current source at two times this level.
7. Set the target LEDs to display the output contacts by typing **TAR F OUT101 <ENTER>**. The front-panel LEDs should now follow Row 73 of the Relay Word where OUT101 is listed.
8. From Access Level 2, set up the Sequential Events Recorder by typing **SET R SER1 <ENTER>**. Enter **87H <SPACE> 86BFT <ENTER>.** Type **END <ENTER>,** and save the settings.
9. Simulate a flashover condition. When a flashover occurs, the voltage across a breaker collapses and current flows. To simulate a flashover condition, turn off the voltage and apply the current at the same time. You have a 5-cycle window for these two conditions to occur, and the current must remain for the FFpu timer setting.
10. Output contact 101 should close at this time, and OUT101 LED should illuminate. The relay default settings have OUT101=86BFT, and the flashover protection output FOBF is part of the M86T equation, which sets the 86BFT element.

Step 17. Purpose: Examine the Sequential Events Records.

Method: Type **SER <ENTER>**. The relay displays up to 512 SERs. The last few SERs correspond to your most recent test. The SER time stamps each assertion or deassertion of the elements you programmed in the SER1

equation. Find the deassertion of the 87H and the assertion of the 86BFT. The difference between the two time stamps should correspond to the Ffpu timer setting plus any delay in the assertion of the current and pickup of the 50LD element.

This checkout procedure demonstrates only a few relay features. For a complete understanding of relay capabilities, study the functional description in ***Section 5: Control Logic***. For more test procedures, see the ***Full Functional Test*** portion of this section.

FULL FUNCTIONAL TEST

This procedure tests relay protective and control functions more fully than the initial checkout procedure.

Equipment Required

The following equipment is necessary to complete a full functional test:

1. A terminal or computer with terminal emulation with EIA-232 serial interface
2. Interconnecting data cable between terminal and relay
3. Source of relay control power
4. Source of synchronized three-phase voltages and at least two currents
5. Ohmmeter or contact opening/closing sensing device
6. Timer with contact inputs for start and stop

What Should Be Tested

A full functional test includes the initial checkout procedure and the additional steps described below. In general, these tests assure that the relay settings match your application rather than checking relay performance. For commissioning purposes, your company policy may require you to perform the full functional test. For maintenance purposes, a quick test of selected relay functions should suffice. For example, test operation of the Failure to Trip for Fault Current logic, each relay contact input, and each contact output.

SETTING TEST

Purpose: Verify that the relay accepts settings.

Method: 1. Gain Level 2 Access (see **ACCESS** and **2ACCESS** commands in ***Section 8: Serial Port Communications and Commands***).

2. Change one setting. For example, change the 47Q pickup setting. Type **SET 47Q TERSE** and press **<ENTER>**. The "TERSE" parameter instructs the SEL-352 Relay to immediately prompt "Save Changes?" following an entry of "END."

   Following the 47Q prompt, type the new setting and press **<ENTER>**.

3. To complete the setting procedure, type **END** and press **<ENTER>**. Type **Y <ENTER>** at the prompt: Save Changes ?

The relay computes internal settings and compares them against fixed limits. If all settings fall within acceptable ranges, the ALARM contact closes momentarily (unless an alarm condition already exists) as the new settings are enabled.

4. Use the **SHOWSET** command to inspect the settings and verify that the change you made in Step 2 was accepted. Type **SHO <ENTER>**.

5. Use **SET** and **SHOWSET** again to restore the initial values and check the settings.

METER TEST

Purpose: Verify the magnitude accuracy. This test uses two or three current and three voltage sources, but it only requires a single voltage and current source.

Method:

1. Connect simulated power system secondary current and voltage. See Figure 11.3 and Figure 11.4 for the test connections.

2. Apply a phase-to-neutral voltage of 50 Vac for each voltage input and a current of 1 A for each current input. The phase angle of the voltage and current sources should all be set to 0°.

3. Use the **METER** command to inspect measured voltages, currents, and power. Voltages VAX, VBX, VCX, VAY, VBY, and VCY should equal the applied voltage times the potential transformer ratio setting. With the Example 500 kV Line settings, you should obtain:

   VA = VB = VC = (50 V)(4300) = 215 kV

   AB, BC, and CA voltages for VX and VY should read less than 1.5 kV because each phase-to-neutral voltage is at the same angle.

   Similarly, currents IA, IB, and IC should equal the applied current times the current transformer ratio. With the Example 500 kV Line settings, you should obtain:

   IA = IB = IC = (1 A)(600) = 600 A

   Difference currents IAB, IBC, and ICA should be less than 20 A. The power reading, P (MW), should read:

   P = (VA)(IA) + (VB)(IB) + (VC)(IC) = 387 MW.

   The reactive power reading Q (MVAR) should be less than 20 MVAR.

   Simultaneous application of voltage and current to the relay could cause the breaker resistor thermal elements to operate. Use the **HEAT R** command to reset the energy levels of the resistor thermal models after completing this test.

PHASE OVERCURRENT ELEMENT TESTS

Purpose: Verify the pickup thresholds of the 50LD, 50MD, and 50FT phase overcurrent elements.

Method:

1. Using the **TAR F** command with the element name, set the bottom row of the front-panel target LEDs to display the nondirectional instantaneous phase overcurrent element. Select one of the phase overcurrent elements from the Relay Word as indicated below: Many of the elements appear in the same Relay Word row so they can be monitored simultaneously.

Setting	Elements
Fixed at 0.1 A (5 A) or 0.02 A (1 A)	50MNA, 50MNB, 50MNC
50LD	50LD, 50LDA, 50LDB, 50LDC
50MD	50MD, 50MDA, 50MDB, 50MDC
50FT	50FT, 50FTA, 50FTB, 50FTC

2. Ramp current on the phase(s) under test and observe the pickup and dropout of each element. Record the results.

3. Verify the test results with the appropriate setting. Use the **SHO** command to check the setting.

GROUND OVERCURRENT ELEMENT TEST

Purpose: Verify the pickup threshold of the 50N ground overcurrent element.

Method:

1. Type **TAR F 50N <ENTER>** to set the fifth LED from the left of the bottom row of the front-panel target LEDs to display the nondirectional instantaneous ground overcurrent element.

Setting	Element
50N	50N

2. Ramp current on the phase under test, and observe the pickup and dropout of the element. Record the results.

3. Verify the test results with the appropriate setting. Use the **SHO** command to check the setting. The 50N element operates on $3I_0$. If current is applied to only one phase, the pickup point should equal the setting.

PHASE VOLTAGE ELEMENT TESTS

Purpose: Verify the pickup thresholds of the phase voltage elements.

Method: 1. Using the **TARGET F** command with the element name, set the bottom row of the front-panel target LEDs to display the appropriate phase voltage element. Select one or more of the phase voltage elements from the Relay Word as indicated below. Many of the elements appear in the same Relay Word row, so they can be monitored simultaneously.

Setting	Elements
27D	X27D3, X27DA, X27DB, X27DC, Y27D3, Y27DA, Y27DB, Y27DC
59L	X59L3, X59LA, X59LB, X59LC, Y59L3, Y59LA, Y59LB, Y59LC
59H	X59H, X59HA, X59HB, X59HC

2. Apply voltage to one phase and observe the pickup and dropout of each element. Record the results. The elements with a 3 at the end of the label require all three phase elements to be picked up.

3. Verify the results with the indicated setting.

NEGATIVE-SEQUENCE OVERVOLTAGE ELEMENT TEST

Purpose: Verify the pickup threshold of the negative-sequence overvoltage elements.

Method: 1. Using the **TARGET F** command with the element name, set the bottom row of the front-panel target LEDs to display the appropriate negative sequence overvoltage element. Select one of the negative-sequence overvoltage elements from the Relay Word as indicated below:

Setting	Elements
47Q	47Q, Y47Q, X47Q

2. Apply voltage to one phase of the X voltage input. Increase the phase voltage and observe the pickup and dropout of the 47Q element. Record the results. Repeat for one phase of the Y voltage input.

3. Verify the results with the indicated setting. Negative-sequence voltage V_2 equals one-third of the applied single-phase voltage. Thus, with a 47Q setting of 10 V, the elements pick up when you apply a single-phase voltage of 30 V.

PHASE CURRENT UNBALANCE ELEMENT TEST

Purpose: Verify the pickup threshold of the phase current unbalance elements (Reference: Figure 3.23).

Method:

1. Using the **TARGET F** command with the element name, set the bottom row of the front-panel target LEDs to display the appropriate current unbalance element. Select one of the current unbalance elements from the Relay Word as indicated below:

Setting	Elements
46UB	46P, 46A, 46B, 46C

2. Apply balanced three-phase current. Decrease the current of the phase under test until the 46 element for that phase asserts. Record the results.

3. Verify the results with the indicated setting. The phase element asserts when the sum of the three-phase current magnitudes divided by the 46UB setting exceeds the current magnitude of the phase under test. This translates to the following equation, for a phase A test:

$$|I_A| \leq \frac{|I_B| + |I_C|}{(46\,UB - 1)}$$

The 46P asserts when any of the phase elements assert.

PHASE OVERPOWER ELEMENT TEST

Purpose: Verify the pickup threshold of the phase overpower elements (Reference: Figure 3.19).

Method:

1. This test requires applying voltage to only one set of voltage inputs. Remove the parallel jumpers for the voltage inputs. These jumpers are shown in Figure 11.3 and Figure 11.4 as dotted lines.

2. Using the **TARGET F** command with the element name, set the bottom row of the front-panel target LEDs to display the appropriate phase overpower element. Select one of the phase overpower elements from the Relay Word as indicated below:

Setting	Elements
37OP	37OP, 37OPA, 37OPB, 37OPC

3. Apply 10 V to the voltage input of the phase under test. Increase phase current (I) slowly and observe element pickup and dropout. Record the results.

4. Verify the results with the indicated setting. The target LED should pick up when 10 V • I = 37OP setting. Test each phase element in this manner. You may wish to test the elements at various values of input voltage as well, but this is not required.

DIFFERENTIAL VOLTAGE ELEMENT TESTS

Purpose: Verify the pickup thresholds of the differential voltage elements.

Method:

1. This test requires applying voltage to only one set of voltage inputs. Remove the parallel jumpers for the voltage inputs. These jumpers are shown in Figure 11.3 and Figure 11.4 as dotted lines.

2. Using the **TARGET F** command with the element name, set the bottom row of the front-panel target LEDs to display the appropriate differential voltage element. Select one or more of the phase voltage elements from the Relay Word as indicated below. Many of the elements appear in the same Relay Word row, so they can be monitored simultaneously.

Setting	Elements
87FO	87F, 87FOA, 87FOB, 87FOC
87TH	87TH, 87THA, 87THB, 87THC
87H	87H, 87HA, 87HB, 87HC

3. Apply voltage to one phase and observe the pickup and dropout of each element. Record the results. The elements without a phase indication assert when any phase is asserted.

Verify the results with the indicated setting.

SYNCHRONISM CHECKING ELEMENT TESTS

Purpose: Verify the pickup thresholds of the synchronism checking elements for angle and slip conditions (Reference: Figure 4.4).

Method:

1. This test requires two separate single-phase voltage sources, one connected to A-phase input of the X voltages (terminals: Z13 and Z16) and one connected to A-phase of the Y voltages (terminals: Z19 and Z22).

   The sources must have the ability to vary the angle of the voltage for the first half of the test and the ability to vary the frequency the second half of the test.

2. Using the **TARGET F** command with the element name, set the bottom row of the front-panel target LEDs to display the appropriate synchronism checking element. Select one of the phase voltage elements from the Relay Word as indicated below:

Setting	Elements
59H, 59L, 25SC, 25AC	25C, 25T
59H, 59L, 25SM, 25AM	25M, 25T

3. Apply a voltage to the X-voltage input that is greater than the 59L setting but less than the 59H setting. Set the angle to 0° and the frequency to your nominal frequency.

4. Apply a voltage to the Y-voltage input that is greater than the 59L setting. Set the angle to 0° and the frequency to your nominal frequency. The 25C, 25M, and 25T elements should all assert, illuminating the corresponding target LEDs.

5. Increase or decrease the angle of the Y-voltage input until the element under test deasserts (LED extinguishes). The 25T will only deassert after both 25M and 25C have dropped out. Record the results.

6. Verify the results with the indicated 25AC or 25AM setting.

7. Apply a voltage to the Y-voltage input that is greater than the 59L setting. Set the angle to 0° and the frequency to your nominal frequency. The 25C, 25M, and 25T elements should all assert, illuminating the corresponding target LEDs.

8. Increase or decrease the frequency of the Y-voltage input until the element under test deasserts (LED extinguishes). Record the results.

9. Verify the results with the indicated 25SC or 25SM setting. These settings are in slip (cycles/sec), which is the difference between the two source frequencies.

FAULT CURRENT BREAKER FAILURE, SCHEME 1 LOGIC TEST

Purpose: Verify operation of the Scheme 1 fault current breaker failure logic (Reference: Figure 3.6).

Method: 1. While the relay is capable of employing five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 1 by setting FTLOG = 1 in the relay setting group. Using the **SET** command, set an output to close when the FBF element asserts, and set the SER to trigger for the TRIPA, 50FT, and FBF elements. Verify the settings with the **SHO** command, and the **SHO G** command for TRIPA.

Setting	Elements
FTLOG, 50FT, FCpu, TTdo TRIPA	50FT, FBF

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in Step 1 asserts.

3. Apply A-phase current above the 50FT setting.

4. Assert the TRIPA input. This action causes the relay to start its 62FC timer. The external timer should also start.

5. Shortly after the TRIPA input asserts, the programmable output contact set in Step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the FCpu timer setting.

6. Shut off A-phase current.

7. Deassert the TRIPA input.

8. This step is optional. To test Scheme 1 logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

9. Repeat Steps 3, 4, 5, 6, 7, and 8 (optional) for phases B and C.

10. Assert the TRIPA input. This action should start the external timer.

11. Quickly apply A-phase current above the 50FT setting. When the TRIPA input is asserted before A-phase current is applied, A-phase current must be applied before the 62TTdo timer expires. This sequence simulates relay operation when used in a ring-bus application.

12. Shortly after applying current to the A-phase, the programmable output contact set in Step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the FCpu timer setting.

13. Deassert the TRIPA input and shut off A-phase current.

14. This step is optional. To test Scheme 1 logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 9 and 10. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

15. Repeat Steps 9, 10, 11, 12, 13, and 14 (optional) for phases B and C.

16. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the TTdo and FCpu timers. The TTdo timer is the time the FBF bit remains asserted after the TRIPA input was deasserted.

FAULT CURRENT BREAKER FAILURE, SCHEME 2 LOGIC TEST

Purpose: Verify operation of the Scheme 2 fault current breaker failure logic (Reference: Figure 3.8).

Method: 1. While the relay is capable of employing five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 2 by setting FTLOG = 2 in the relay setting group. Using the **SET** command, set an output to close when the FBF element asserts, and set the SER to trigger for the TRIPA, 50FT, and FBF elements. Verify the settings with the **SHO** command, and verify the **SHO G** command for TRIPA.

Setting	Elements
FTLOG, 50FT, FCpu, TRIPA	50FT, FBF

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in Step 1 asserts.

3. Apply A-phase current above the 50FT setting. The relay should generate an event report.

4. Assert the TRIPA input. This action causes the relay to start its 62FC timer. The external timer should also start.

5. Shortly after the TRIPA input asserts, the programmable output contact set in Step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the FCpu setting.

6. Deassert the TRIPA input, and shut off A-phase current.

7. This step is optional. To test Scheme 2 logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

8. Repeat Steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

9. For each test the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the FCpu timer. The time between TRIPA being asserted and FBF being asserted should be about the same as the FCpu setting.

FAULT CURRENT BREAKER FAILURE, SCHEME 3 LOGIC TEST

Purpose: Verify operation of the Scheme 3 fault current breaker failure logic (Reference: Figure 3.10).

Method: 1. While the relay can use five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 3 by setting FTLOG = 3 in the relay setting group. Using the **SET** command, set an output to close when the FBF

element asserts, and set the SER to trigger for the TRIPA, 50FT, and FBF elements. Verify the settings with the **SHO** command, and verify the **SHO G** command for TRIPA.

Setting	Elements
FTLOG, 50FT, FCpu, TRIPA	50FT, FBF

2. Connect an external timer, and set it to start when the TRIPA input asserts and stop when the programmable output you set in Step 1 asserts.
3. Apply A-phase current above the 50FT setting. The relay should generate an event report.
4. Assert the TRIPA input. This action causes the relay to start its 62FC timer. The external timer should also start.
5. Shortly after the TRIPA input asserts, the programmable output contact set in Step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the FCpu setting.
6. Deassert the TRIPA input, and shut off A-phase current.
7. This step is optional. To test Scheme 3 logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

   When Scheme 3 is enabled, the TRIP input is not latched. Thus, if TRIP input deassertion occurs while phase current is applied but before 62FC timer expiration, the relay does not assert the FBF bit.
8. Repeat Steps 3, 4, 5, 6, and 7 (optional) for phases B and C.
9. Set the external timer to start when you apply current to the relay and stop when the programmable contact set in Step 1 closes.
10. Assert the TRIPA input.
11. Apply A-phase current above the 50FT setting. As a result, the relay starts its 62FC timer. The external timer should also start.
12. Shortly after you apply A-phase current, the programmable output contact set in Step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the FCpu setting.
13. Deassert the TRIPA input and shut off A-phase current.
14. This step is optional. To test Scheme 3 logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 10 and 11. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

When Scheme 3 is enabled, the TRIPA input is not latched. Thus, if the TRIPA input deasserts while phase current is applied but before 62FC timer expiration, the relay does not assert the FBF bit.

15. Repeat Steps 10, 11, 12, 13, and 14 (optional) for phases B and C.

16. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the FCpu timer. The FCpu time is the time between the assertion of TRIPA and the assertion of FBF.

FAULT CURRENT BREAKER FAILURE, SCHEME 4 LOGIC TEST

Purpose: Verify operation of the Scheme 4 fault current breaker failure logic (Reference: Figure 3.12).

Method: 1. While the relay can use five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 4 by setting FTLOG = 4 in the relay setting group. Using the **SET** command, set an output to close when the FBF element asserts, and set the SER to trigger for the TRIPA, 50FT, and FBF elements. Verify the settings with the **SHO** command, and verify the **SHO G** command for TRIPA.

Setting	Elements
FTLOG, 50FT, TTpu, TTdo TRIPA	50FT, FBF

2. Connect an external timer and set it to start when the TRIPA input asserts and stop when the programmable output you set in Step 1 asserts.

3. Apply A-phase current above the 50FT setting. The relay should generate an event report.

4. Assert the TRIPA input. This action causes the relay to start its 62TT timer. The external timer should also start.

5. Shortly after the TRIPA input asserts, the programmable output contact set in Step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the TTpu setting.

6. Deassert the TRIPA input and shut off A-phase current.

7. This step is optional. To test Scheme 4 logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62TT timer expires. The FBF bit should not assert.

8. Repeat Steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

9. Assert the TRIPA input. Apply A-phase current TTpu cycles following TRIPA

input assertion, but before the TTdo time expires. The programmable output contact set in Step 1 should close, indicating FBF bit assertion.

10. Repeat Step 9 for phases B and C.

11. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the TTpu and TTdo timers. The TTpu timer is the time between the assertion of TRIPA and assertion of FBF. The TTdo timer is the time between FBF assertion and FBF deassertion.

FAULT CURRENT BREAKER FAILURE, SCHEME 5 LOGIC TEST

Purpose: Verify operation of the Scheme 5 fault current breaker failure logic (Reference: Figure 3.14).

Method: 1. While the relay can use five different fault current breaker failure schemes, only one is enabled at a time. Select Scheme 5 by setting Schm = FTLOG = 5 in the relay setting group. Using the **SET** command, set an output to close when the FBF element asserts, and set the SER to trigger for the TRIPA, 50FT, and FBF elements. Verify the settings with the **SHO** command, and verify the **SHO G** command for TRIPA.

Setting	Elements
FTLOG, 50FT, FCpu, TRIPA	50FT, FBF

2. Connect an external timer, and set it to start when the TRIPA input asserts and stop when the programmable output you set in Step 1 asserts.

3. Apply A-phase current above the 50FT setting. The relay should generate an event report.

4. Assert the TRIPA input. This action starts the relay 62FC timer. The external timer should also start.

5. Shortly after TRIPA input assertion, the programmable output contact set in Step 1 should close, indicating FBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the FCpu setting.

6. Deassert the TRIPA input and shut off A-phase current.

7. This step is optional. To test Scheme 5 logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62FC timer expires. The FBF bit should not assert.

8. When Scheme 5 is enabled, the TRIPA input is not latched. Thus, if the TRIPA input deasserts while phase current is applied but before 62FC timer expiration, the relay does not assert the FBF bit.

9. Repeat Steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

10. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the FCpu setting. The FCpu timer is the time between the assertion of TRIPA and assertion of FBF.

LOAD CURRENT BREAKER FAILURE, SCHEME 1 LOGIC TEST

Purpose: Verify operation of the Scheme 1 load current breaker failure logic (Reference: Figure 3.17).

Method: 1. While the relay can use two different load current breaker failure schemes, only one is enabled at a time. Select Scheme 1 by setting LDLOG = 1 in the relay setting group. Using the **SET** command, set an output to close when the LBF element asserts, and set the SER to trigger for the TRIPA, 50LD, LPF, and LBF elements. Verify the settings with the **SHO** command, and verify the **SHO G** command for TRIPA.

Setting	Elements
LDLOG, 50LD, LPpu, LFpu TRIPA	50FT, FBF

2. Connect an external timer, and set it to start when the TRIPA input asserts and stop when the programmable output you set in Step 1 asserts.

3. Apply A-phase current above the 50LD setting. (Current should not exceed the 50FT setting.)

4. Assert the TRIPA input. This starts the relay 62LP and 62LD timers. The external timer should also start.

5. Shortly after TRIPA input assertion, the programmable output contact set in Step 1 should close, indicating LBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the LDpu setting.

6. Deassert the TRIPA input, and shut off A-phase current.

7. This step is optional. To test logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 3 and 4. This time, turn off A-phase current 1.5 to 2.0 cycles before the 62LD timer expires. The LBF bit should not assert.

8. Repeat Steps 3, 4, 5, 6, and 7 (optional) for phases B and C.

9. In Step 5, 62LP timer expiration can generate an event report. You can set the LPF bit in a programmable output contact mask, and perform Steps 3, 4, 5, 6, and 7 to test the load current pending failure logic.

10. For each test, the relay generated a sequential events record for the elements

programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the LPpu and LFpu timers. The LPpu and LFpu times are the times between the assertion of TRIPA and the assertion of LPF and LBF, respectively.

LOAD CURRENT BREAKER FAILURE, SCHEME 2 LOGIC TEST

Purpose: Verify operation of the Scheme 2 load current breaker failure logic (Reference: Figure 3.18).

Method:

1. While the relay can use two different load current breaker failure schemes, only one is enabled at a time. Select Scheme 2 by setting LDLOG = 2 in the relay setting group. Scheme 2 includes all of Scheme 2 logic plus additional logic that monitors the breaker status. Perform Scheme 1 testing in addition to the following tests. Using the **SET** command, set an output to close when the LBF element asserts, and set the SER to trigger for the TRIPA, 52AA, LPF, and LBF elements. Verify the settings with the **SHO** command, and verify the **SHO G** command for TRIPA and 52AA.

Setting	**Elements**
LDLOG, APpu, AFpu TRIPA, 52A	50FT, FBF

2. Connect an external timer, and set it to start when the TRIPA input asserts and stop when the programmable output you set in Step 1 asserts.
3. Assert the 52AA input.
4. Assert the TRIPA input. This starts the relay 62AP and 62AF timers. The external timer should also start.
5. Shortly after TRIPA input assertion, the programmable output contact set in Step 1 should close, indicating LBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the LDpu setting.
6. Deassert the TRIPA and 52AA inputs.
7. This step is optional. To test logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 3 and 4. This time, deassert the 52AA input 1.5 to 2.0 cycles before the 62AF timer expires. The LBF bit should not assert.
8. Repeat Steps 3, 4, 5, 6, and 7 (optional) for phases B and C.
9. In Step 5, 62LP timer expiration can generate an event report. You can set the LPF bit in a programmable output contact and perform Steps 3, 4, 5, 6, and 7 to test the load current pending failure logic.
10. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time

stamps will also verify the APpu and AFpu timers. The APpu and AFpu times are the times between the assertion of TRIPA and the assertion of LPF and LBF respectively. Verify logic reset by looking for the deassertion of the LBF and LPF elements.

CIRCUIT BREAKER CLOSE RESISTOR THERMAL FAILURE LOGIC TEST

Purpose: Verify operation of the breaker close resistor thermal failure logic (Reference: Figure 3.19).

Method:

1. Using the **SET** command, set an output to close when the CTF element asserts, and set the SER to trigger for the elements listed below. Verify the settings with the **SHO** command and verify the **SHO G** command for 52AA, MCLOSE, and CLOSE. Note that THLOG must be set to ON.

Setting	Elements
THLOG, 50MN, 26CF, 37OP, 87TH, OPpu, 52AA, MCLOSE, CLOSE (47Q not used)	CTF, 50MNA, 37OPA, 87THA, OPAD, 52AA, MCLOSE, CLOSE

2. Use the **HEA R** command to reset the thermal models before each timing test.

3. Connect an external timer and set it to start when you apply A-phase current and stop when the programmable output you set in Step 1 asserts.

4. Assert the CLOSE and/or MCLOSE input by applying dc control voltage to the assigned input terminals.

5. Apply voltage greater than the 87TH setting to the A-phase voltage input. Calculate a current magnitude such that applied power (Pa) is greater than the 37OP setting. Pa is defined:

   $Pa = Va \bullet Ia\ W$

   Where:

   Pa = applied power
   Va = applied phase voltage magnitude
   Ia = applied phase current magnitude

   Note: Applied current (Ia) must exceed 0.1 A to operate the CTF bit.

6. Calculate an estimated time to trip (TTT) in seconds by dividing the 26CF setting by Pa:

$$TTT = \frac{26\,CF}{Pa} s$$

7. Apply A-phase current equal to the magnitude Ia calculated above. The external timer should start upon application of A-phase current.

8. Shortly after you apply phase current, the programmable output contact set in Step 1 should close, indicating CTF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the TTT value calculated above plus the OPpu timer setting.

9. Shut off phase current.

10. In Step 6, accumulation of breaker resistor energy equal to the 26CP thermal pending failure value can cause the relay to generate an event report. You can set the 26CPA bit in a programmable output contact mask and perform Steps 4, 5, 6, 7, 8, and 9 for the close resistor thermal pending failure logic.

11. You may wish to test this logic for various values of input voltage, current, and power. Use the **HEAT** command to display the per-unit energy content of the breaker resistor thermal models. Use the **HEA R** command to reset the thermal models before each timing test.

12. Repeat Steps 4–11 for B- and C-phases.

13. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the OPpu timer. The OPpu time is the time between the assertion of 37OPA and the assertion of OPAD.

CIRCUIT BREAKER TRIP RESISTOR THERMAL FAILURE LOGIC TEST

Purpose: Verify operation of the breaker trip resistor thermal failure logic (Reference: Figure 3.19).

Method: 1. Using the **SET** command, set an output to close when the TTF element asserts, and set the SER to trigger for the elements listed below. Verify the settings with the **SHO** command, and the **SHO G** command for 52AA and TRIPA. Note that THLOG must be set to ON.

Setting	Elements
THLOG, 50MN, 26TF, 37OP, 87TH, OPpu, 52AA, TRIPA (47Q not used)	TTF, 50MNA, 37OPA, 87THA, OPAD, 52AA, TRIPA

2. Use the **HEA R** command to reset the thermal models before each timing test.

3. Connect an external timer and set it to start when you apply A-phase current and stop when the programmable output you set in Step 1 asserts.

4. Assert the TRIPA input by applying dc control voltage to the input terminals.

5. Apply voltage higher than the 87TH setting to the A-phase voltage input.

Calculate a current magnitude such that applied power (Pa) is greater than the 37OP setting. Pa is defined:

$$Pa = Va \bullet Ia\ W$$

Where:

Pa = applied power
Va = applied phase voltage magnitude
Ia = applied phase current magnitude

Note: Applied current (Ia) must exceed 0.1 A to operate the TTF bit.

6. Calculate an estimated time to trip (TTT) by dividing the 26TF setting by Pa:

$$TTT = \frac{26\,TF}{Pa} s$$

7. Apply A-phase current equal to the magnitude Ia calculated above. The external timer should start upon application of A-phase current.

8. Shortly after you apply phase current, the programmable output contact set in Step 1 should close, indicating TTF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the TTT value calculated above plus the OPpu timer setting.

9. Shut off phase current.

10. In Step 6, accumulation of breaker resistor energy equal to the 26TP thermal pending failure value can generate an event report. You can set the 26TPA bit in a programmable output contact mask, and perform Steps 4, 5, 6, 7, 8, and 9 for the trip resistor thermal pending failure logic.

11. You may wish to test this logic for various values of input voltage, current, and power. Use the **HEAT** command to display the per unit energy content of the breaker resistor thermal models. Use the **HEAT R** command to reset the thermal models before each timing test.

12. Repeat Steps 4–11 for B- and C-phases.

13. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the OPpu timer. The OPpu time is the time between the assertion of 37OPA and the assertion of OPAD.

VOLTAGE NULLING LOGIC TEST

Purpose: Verify the voltage nulling logic (Reference: Figure 3.20).

Method: 1. Verify the settings with the **SHO** command and the **SHO G** command for TRIPA, CLOSE, MCLOSE, and 52AA. Set the SER to trigger for KTRK and 52AA.

Setting	Elements
59L, VNpu, TRIPA, CLOSE, MCLOSE, 52AA	KTRK, X59LA, Y59LA, MCLOSE, CLOSE, TRIPA, 52AA

2. Apply 67 V to VAX and VAY inputs, which should be above the 59L setting. Verify that these elements are asserted by typing **TAR X59LA<ENTER>** and **TAR Y59LA<ENTER>**.

3. Apply dc control voltage to the input assigned to 52AA.

4. Verify that the SEL-352 Relay is tracking the voltage by typing **TAR KTRK <ENTER>.** KTRK should be a logical one after the VNpu time delay. The default setting is VNpu = 10 minutes.

5. Trigger an event report by typing **TRI <ENTER>.**

6. View the event report by typing **EVE <ENTER>.** Use **<CTRL>X** to cancel the scrolling when the voltage nulling factors appear.

7. Verify that A-phase voltage nulling magnitude is 1 and the angle is 0.

8. Change the magnitude of the X or Y voltage to 70 V. Repeat Steps 4, 5, and 6. The nulling magnitude should now be approximately 1.04 or 0.96 depending on which value was changed.

9. Change the angle of the X or Y voltage by 2°. Repeat Steps 4, 5, and 6. The nulling angle should now be 2°.

10. Repeat Steps 2 through 9 for B and C phases.

11. Optional. Change the magnitudes and angles of the voltages and verify the voltage nulling tracking. The relay will not track (KTRK = 0) if either voltage is below the 59L setting or TRIPA, CLOSE, or MCLOSE are asserted. If any of these conditions disable the tracking, the K value is held at its most recent calculation. If KMAG is exceeded or KANG is exceeded, the K value is held at the maximum values, but the relay is still tracking (KTRK = 1).

12. Using the **SET** command, program an output contact to close when the KTRK bit is asserted.

13. Connect a timer to start timing when dc control voltage is applied to the input assigned to 52AA and stop when the output contact programmed in Step 12 closes.

14. Apply 67 V to the X and Y voltage inputs.

15. Apply dc control voltage to the input assigned to 52AA. This should start the timer. KTRK asserts VNpu minutes after the input is asserted. Verify your timer value with the VNpu setting.

16. View the SER using the **SER** command. The VNpu timer setting is the time between the assertion of 52AA and the assertion of KTRK.

FLASHOVER DETECTION LOGIC, SCHEME 1 LOGIC TEST

Purpose: Verify Scheme 1 for current through an open breaker logic (Reference: Figure 3.21).

Method: 1. While the relay can use two different flashover detection schemes, only one is enabled at a time. Select Scheme 1 by setting FOLOG = 1 in the relay setting group. Using the **SET** command, set an output to close when the FOBF element asserts, and set the SER to trigger for the elements listed below. Verify the settings with the **SHO** command, and verify the **SHO G** command for TRIPA, MCLOSE, and CLOSE.

Setting	Elements
FOLOG, FFpu, FPpu, 59H, 87H, 50LD, 87FO, TRIPA, CLOSE, MCLOSE	50LD, 87HA, 87FOA, 87FOB, 87FOC, FOBF, FOPF, CLOSE, MCLOSE, TRIPA

2. Connect an external timer, and set it to start when you apply A-phase current and stop when the programmable output you set in Step 1 asserts.

3. Apply voltage at least 10 V higher than the 87H setting to the X-side voltage inputs of the A-phase.

4. Turn the voltage source off (0.0 V) as you apply phase current above the 50LD setting. This action should start the external timer.

5. Shortly after you apply A-phase current, the programmable output contact set in Step 1 should close, indicating FOBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the FFpu setting.

6. Shut off A-phase current.

7. Repeat Steps 3, 4, and 6 four times. During the first repetition, assert the TRIPA input before applying phase voltage. During the second repetition, assert the CLOSE input (but not the TRIP input) before applying phase voltage. During the third repetition, assert the MCLOSE input, with no other inputs asserted, before applying phase voltage. On the fourth repetition, with no inputs asserted, reduce the voltage in Step 4 to some voltage above the 87FO setting but below the 87H setting. In these repetitions, the relay should not assert the FOBF bit.

8. Repeat Steps 3, 4, 5, 6, and 7 for B-phase and C-phase.

9. In Step 5, 62FP timer expiration can cause the relay to generate an event report. You can set the FOPF bit in a programmable output contact mask, and perform Steps 3, 4, 5, 6, and 7 for the flashover pending failure logic.

10. For each test, the relay generated a sequential events record for the elements

programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the FFpu and FPpu timers. The FFpu and FPpu times are the times between the assertion of the current and the assertion of FOBF and FOPF, respectively.

Note: Because this test involves simultaneous application of voltage and current to the relay, the breaker resistor thermal protection elements can acquire energy. To reset resistor thermal model energies to zero, type **HEA R <ENTER>** after each phase test.

FLASHOVER DETECTION LOGIC, SCHEME 2 LOGIC TEST

Purpose: Verify Scheme 2 for current through an open breaker logic (Reference: Figure 3.22).

Method:

1. While the relay can use two different flashover detection schemes, only one is enabled at a time. Select Scheme 2 by setting FOLOG = 2 in the relay setting group. Using the **SET** command, set an output to close when the FOBF element asserts, and set the SER to trigger for the elements listed below. Verify the settings with the **SHO** command, and verify the **SHO G** command for TRIPA, MCLOSE, CLOSE and 52AA.

Setting	Elements
FOLOG, FFpu, FPpu, 59L, 50LD, TRIPA, CLOSE, MCLOSE, 52AA	50LD, X59HA, FOBF, FOPF, CLOSE, MCLOSE, TRIPA, 52AA

2. Connect an external timer, and set it to start when you apply A-phase current and stop when the programmable output you set in Step 1 asserts.
3. Apply 67 V, which should be higher than the 59L setting, to the X-side voltage inputs of the phase under test.
4. Turn the voltage source off (0.0 V) as you apply phase current above the 50LD setting. This action should start the external timer.
5. Shortly after you apply A-phase current, the programmable output contact set in Step 1 should close, indicating FOBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the FFpu setting.
6. Shut off A-phase current.
7. Repeat Steps 3, 4, and 6 four times. During the first repetition, assert the TRIPA input before applying phase voltage. During the second repetition, assert the CLOSE input (but not the TRIP input) before applying phase voltage. During the third repetition, assert the MCLOSE input, with no other inputs asserted, before applying phase voltage. On the fourth repetition, assert the 52AA input (but no other inputs) before applying phase voltage. In these repetitions, the relay should not assert the FOBF bit.

8. Repeat Steps 3, 4, 5, 6, and 7 for B-phase and C-phase.

9. In Step 5, 62FP timer expiration can cause the relay to generate an event report. You can set the FOPF bit in a programmable output contact equation and perform Steps 3, 4, 5, 6, and 7 for the flashover pending failure logic.

10. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the FFpu and FPpu timers. The FFpu and FPpu times are the times between the assertion of 50LD and the assertion of FOBF and FOPF, respectively.

Note: Because this test involves simultaneous application of voltage and current to the relay, the breaker resistor thermal protection elements can acquire energy. To reset resistor thermal model energies to zero, type **HEA R <ENTER>** after each phase test.

CURRENT UNBALANCE, FAILURE TO CLOSE LOGIC TEST

Purpose: Verify operation of the current unbalance logic (Reference: Figure 3.23).

Method: 1. Using the **SET** command, set an output to close when the UBBF element asserts, and set the SER to trigger for the elements listed below. Verify the settings with the **SHO** command, and the **SHO G** command for MCLOSE and CLOSE. Note that UBLOG must be set to ON.

Setting	Elements
UBLOG, UCpu, UFpu, UPpu, 50LD, 46UB, MCLOSE, CLOSE	50LD, 46A, FOBF, FOPF, MCLOSE, CLOSE

2. Connect an external timer, and set it to start when you apply B- or C-phase current and stop when the programmable output you set in Step 1 asserts.

3. Assert the CLOSE and/or the MCLOSE input(s) by applying rated control voltage to the input terminals.

4. Apply B- and C-phase current above the 50LD setting. This action should start the external timer.

5. Shortly after you apply phase current, the programmable output contact set in Step 1 should close, indicating UBBF bit assertion. This action should stop the external timer. Record the timer reading. It should be close to the UFpu timer setting.

6. Shut off phase current.

7. Repeat Steps 3, 4, and 6 three times. During the first two repetitions, do not assert the CLOSE or MCLOSE inputs before applying phase current. During the second

repetition, apply phase current below the 50LD setting with at least one of the inputs asserted. In these repetitions, the relay should not assert the UBBF bit.

8. This step is optional. To test logic operation under conditions that could represent normal relay/breaker operation, repeat Steps 3 and 4. This time, turn on C-phase current 1.5 to 2.0 cycles before the UFpu timer expires. The UBBF bit should not assert.

9. Repeat Steps 3, 4, 5, 6, 7, and 8 (optional) for B-phase and C-phase, the phase under test being the phase with no current applied in Step 4.

10. In Step 5, UPpu timer expiration can cause the relay to generate an event report. You can set the UBPF bit in a programmable output contact and perform Steps 3, 4, 5, 6, 7, and 8 for the current unbalance pending failure logic.

11. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. These time stamps will also verify the UCpu, UFpu, and UPpu timers. The UFpu and UPpu times are the times between the assertion of 46A and the assertion of UBBF and UBPF, respectively. If current is applied before the CLOSE or MCLOSE input, the UCpu time is the time between the assertion of the input and the assertion of UBBF with the UFpu time subtracted out.

LOSS-OF-DIELECTRIC LOGIC TEST

Purpose: Verify the loss-of-dielectric logic (Reference: Figure 3.26).

Method: 1. Using the **SET** command, set one output to close when the LODBF element asserts and another output to close when LODPF element asserts, and set the SER to trigger for the listed elements. Verify the settings with the **SHO** and **SHO G** commands.

Setting	Elements
L2pu, LOD1, LOD2, LODCT	LODBF, LODPF, LOD1, LOD2, LODCT

2. Connect a timer to start when dc control voltage is applied to the LOD1 input and stop when the output contact programmed for LODBF closes.

3. Assert the LOD1 input by applying dc control voltage to the assigned input terminals. Verify that the output contact programmed for LODBF in Step 1 closes.

4. Record the time from Step 3. This time should be close to one second.

5. Reconnect the timer to start when dc control voltage is applied to the LOD2 input and stop when the output contact programmed for LODPF closes.

6. Assert the LOD2 input by applying dc control voltage to the assigned input terminals. Verify that the output contact programmed for LODPF in Step 1 closes.

7. Record the time from Step 6. This time should be close to the L2pu timer setting.

8. Reconnect the timer to start when dc control voltage is applied to the LODCT input and stop when the output contact programmed for LODPF closes.

9. Assert the LODCT input by applying dc control voltage to the assigned input terminals. Verify that the output contact programmed for LODPF in Step 1 closes.

10. Record the time from Step 6. This time should be close to one second.

11. Optional. LOD1 and LOD2 block assertion of LODPF and LODBF, respectively, once their corresponding timers pick up. Verify this by applying control voltage to these inputs to block the output.

12. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. Observe the times between the assertion of the inputs (LOD1, LOD2, and LODCT) and assertion of the corresponding outputs (LODBF and LODPF).

STAGGERED CLOSE LOGIC TEST

Purpose: Verify the staggered close logic (Reference: Figure 4.1).

Method: 1. While the relay can use two different closing schemes, only one is enabled at a time. Select Scheme 1 by setting CLSLOG = 1 in the relay setting group. Using the **SET** command, set an output to close when the CCA element asserts, and set the SER to trigger for the listed elements. It is recommended that one of the Fast High Current Interrupting Output contacts is used for accurate timing. Refer to Interface Board 5 specified in ***Section 2: Installation***. Verify the settings with the **SHO** and **SHO G** command.

Setting	**Elements**
CLSLOG, RCApu, CLSdo, CLOSE, MCLOSE	CLOSE, MCLOSE, CCA

2. Connect an external timer and set it to start when you assert the CLOSE or MCLOSE assigned input and stop when the programmable output you set in Step 1 closes.

3. Apply dc control voltage to the input assigned to CLOSE.

4. Verify that the timer reading is approximately the RCApu timer setting.

5. Connect an external timer, and set it to start when the programmable output you set in Step 1 closes and stop when the output opens.

6. Apply dc control voltage to the input assigned to CLOSE.

7. Verify that the timer reading is approximately the CLSdo timer setting.

8. Repeat Steps 2 through 7 for B-phase and C-phase.

9. Repeat Steps 2 through 8 using the input assigned to MCLOSE.

10. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. The RCApu timer setting should be the difference between assertion of the CLOSE or MCLOSE input and assertion of the CCA element. The CLSdo timer setting should be the difference between the assertion of the CCA element and the deassertion of the CCA element.

POINT-ON-WAVE CLOSE LOGIC TEST

Purpose: Verify the point-on-wave close logic (Reference: Figures 4.6–4.9).

Method: 1. While the relay can use two different closing schemes, only one is enabled at a time. Select Scheme 2 by setting CLSLOG = 2 in the relay setting group. Point-on-wave closing controls the output contacts faster than the processing interval of the relay. Use an oscilloscope to monitor the voltages and the output contact operation to verify the point at which the contacts close. Using the **SET R** command, set the SER to trigger for the listed elements. Using the **SET** command, set CLSA to control one of the fast high current interrupting output contacts. One of these fast high current interrupting outputs must be used for accurate timing.

   The following test uses the relay event report to verify point-on-wave closing to ±2 ms.

   Using the **SET R** command, set the SER to trigger for the listed elements. Using the **SET** command, set MER to CLOSE+MCLOSE. Using the **SET** command, set three outputs to follow the CTA, CTB, and CTC elements (i.e., OUT101 = CTA). Verify the settings with the **SHO** commands.

Setting	Elements
CLSLOG, 59L, CLSA, ZCApu, PCApu, CLSdo, TRIPA, CLOSE, MCLOSE	CTA, TRIPA, X59L3, Y59L3, XNTA, YNTA, XPTA, YPTA, CLOSE, MCLOSE

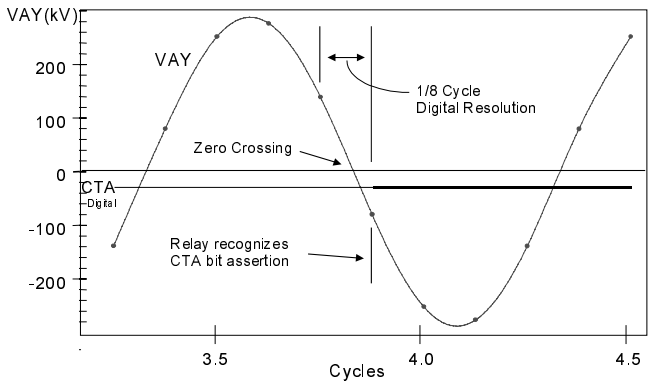
2. Apply a balanced 67 V to VAX, VBX, and VCX (each 120° out of phase).

3. Assert the CLOSE input to initiate point-on-wave closing.

4. Deassert the CLOSE input.

5. Verify that the CCA element asserted and deasserted by viewing the SER.

6. To verify the point on the wave when the output contact closed view the event report. EVE S8 displays the Y-side voltages in 8 samples per cycle for the most recent event generated. After the close input assertion (a greater than symbol indicates the trigger point), look for the sample that shows the outputs that were set in Step 1 (CTA, CTB, CTC) picking up. Verify that this sample also corresponds (±1 sample) to the negative going zero crossing of A-phase voltage. The A-phase voltage should transition from a positive number to a negative number.



7. Verify B- and C-phase by comparing the CTB output pick up to the B-phase voltage and the CTC output to the C-phase voltage.

8. Note that the zero-crossing detection is based on A-phase, and it is assumed that B and C are 120° and 240° out of phase.

9. Adjust the output timer settings such as ZCApu and PCApu for each phase to test these timers. Remember that the relay is assuming balanced phase voltages 120° apart for its timer calculations.

10. Repeat Tests 1 through 9, changing the trigger conditions. Use MCLOSE instead of CLOSE or live Y-side voltages instead of X side.

11. Repeat Tests 1 through 10 asserting TRIPA, TRIPB, or TRIPC inputs to disable the close logic.

12. Verify the 2-cycle dropout time of MCLOSE by viewing the SER. From assertion of MCLOSE to the deassertion of ZCNA should be 2 cycles.

13. Verify the CLSdo setting for the CLOSE input by viewing the SER. From assertion of CLOSE to the deassertion of ZCNA should be the CLSdo setting.

SYNCHRONISM CLOSE LOGIC TEST

Purpose: Verify the synchronism portion of the controlled close logic (Reference: Figure 4.4, Figure 4.5).

Method:

1. While the relay can use two different closing schemes, only one is enabled at a time. Select Scheme 2 by setting CLSLOG = 2 in the relay setting group. Using the **SET R** command, set the SER to trigger for the listed elements. Using the **SET** command, set an output contact to CCA. Verify the settings with the **SHO** commands.

Setting	Elements
CLSLOG, 59L, CLSdo, SYNCdo, TRIPA, CLOSE, MCLOSE	CCA, TRIPA, X59L3, Y59L3, 25M, 25C, CLOSE, MCLOSE, SYNCTD, MCTD

2. Connect a timer to start timing when the output contact programmed in Step 1 closes and stop when the output contact opens again.
3. Assert the MCLOSE input to initiate a manual close condition.
4. Verify the timer reading is approximately the CLSdo setting.
5. Apply 67 V to VAX and VAY.
6. Assert the CLOSE input to indicate an automatic synchronous close condition.
7. Assert the MCLOSE input to indicate a manual synchronous close condition.
8. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. The SYNCdo timer setting is the time from SYNCTD assertion to SYNCTD deassertion for all CLOSE operations. The MCLOSE operations use the MCTD bit that is the output of the fixed 2-cycle MCT timer.

TRAPPED CHARGE DETECTION LOGIC TEST

Purpose: Verify the trapped charge detection logic (Reference: Figure 4.6).

Method: At this time, the only method for testing the trapped charge detection logic is to replay actual system conditions through test equipment such as the SEL-AMS. The SEL-RTS Relay Test System includes an SEL-AMS and uses a COMTRADE format for data input. Contact a customer service representative for more information.

INSTANTANEOUS RETRIP, SCHEME 1 RETRIP LOGIC TEST

Purpose: Verify Scheme 1 of the retrip logic.

Method: 1. While the relay can use two different retrip schemes, only one is enabled at a time. Select Scheme 1 by setting RTPLOG = 1 in the relay setting group. Using the **SET** command, set an output to close when the RTA element asserts, and set the SER to trigger for the listed elements. Verify the TRIPA setting with the **SHO G** command.

Setting	Elements
RTPLOG, TRIPA	RTA, TRIPA

2. Assert the TRIPA input by applying dc control voltage to the assigned input terminals. Verify that the output contact set in Step 1 closes.

3. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. Observe the assertion of TRIPA and RTA.

4. Repeat Steps 2 and 3 for each phase.

TIME-DELAYED RETRIP, SCHEME 2 RETRIP LOGIC TEST

Purpose: Verify Scheme 2 of the retrip logic (Reference: Figure 4.11 Retrip logic diagram).

Method: 1. While the relay can use two different retrip schemes, only one is enabled at a time. Select Scheme 2 by setting RTPLOG = 2 in the relay setting group. Using the **SET** command, set an output to close when the RTA element asserts, and set the SER to trigger for the listed elements. Verify the TRIPA setting with the **SHO G** command.

Setting	Elements
RTPLOG, TRIPA	RTA, TRIPA

2. Connect an external timer, and set it to start when you assert the TRIPA input and stop when the programmable output you set in Step 1 asserts.

3. Apply balanced three-phase current above the 50LD setting. Assert the TRIPA input by applying dc control voltage to the TRIPA input terminals. This should start the external timer.

4. A moment later, the output contact you set in Step 1 should close, stopping the external timer. Take note of the time recorded. It should be approximately equal to the RTpu timer setting.

5. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. The RTpu time should be the time between assertion of TRIPA and assertion of RTA.

6. Repeat Steps 3, 4, and 5 for B-phase and C-phase.

LOCKOUT RELAY CONTROL, SCHEME 1 LOGIC TEST

Purpose: Verify Scheme 1 operation of the lockout relay control logic (Reference: Figure 4.12 and Figure 4.13).

Method: 1. While the relay can use two different lockout relay control schemes, only one is enabled at a time. Select Scheme 1 by setting TRLOG = 1 in the relay setting group. Using the **SET** command, set one output to close when the 86BFT element asserts and another output contact to close when the 86RS element asserts. Set the SER to trigger for the listed elements. Verify the settings with the **SHO** and the **SHO G** command.

Setting	Elements
TRLOG, LDLOG, M86T, 50MD, M2pu, 52AA, TRIPA, 86BFT, 86RS, CTF, TTF	LBF, 86BFT, 86RS, 52AA, 50MD, M86T, TRIPA, CTF, TTF

2. Enable Scheme 2 of the failure-to-trip load current logic using SET LDLOG. Save the settings. This logic sets the LBF bit based on the breaker status and the TRIPA input.

3. Connect an external timer, and set it to start when the output contact programmed in Step 1 for 86BFT closes and stop when the output opens.

4. Assert the 52AA input by applying dc control voltage to the assigned input terminals.

5. Assert the TRIPA input. This action starts the relay AFpu timer of the failure to trip load logic.

6. Shortly after TRIPA input assertion, the 86BFT output should close, indicating LBF bit assertion. This action should start the external timer.

7. Deassert the TRIPA input.

8. M2pu cycles after the 86BFT output asserts, it should deassert, stopping the timer. The timer reading should be approximately equal to the M2pu timer setting.

9. Reconnect the timer to stop when the programmable output contact set to indicate 86RS closes.

10. Repeat Steps 4, 5, and 6. Approximately 5 seconds after the 86BFT output opens, the 86RS bit should assert, causing the programmable output contact set in Step 1 to close, stopping the external timer.

11. Note the reading on the timer. Subtract the time recorded in Step 8 from the timer reading. The difference should be approximately 5 seconds (M4 fixed timer).

12. Reconnect the timer to start when the programmable output contact set to indicate 86RS closes and stop when that contact opens.

13. Repeat Steps 4, 5, and 6. Approximately 5 seconds after the 86BF TRIP output operates, the 86RS contact should close, then open.

14. Note the reading on the timer. The time recorded should be approximately 1 second (M1 fixed timer).

15. Optional. If you apply phase current above the 50MD setting before or while the 86BFT output is asserted, the relay delays deassertion of the 86BFT output and assertion of the 86RS element. Also, if either the trip or close thermal elements pickup (CTF, TTF) the 86RS element assertion will be delayed.

16. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. Verify M1 (60 cycles) from the assertion of 86RS to the deassertion of 86RS. Verify M2pu from the assertion of 86BFT to the deassertion of 86BFT. Verify M4 (300 cycles) from the deassertion of 86BFT to the assertion of 86RS.

LOCKOUT RELAY CONTROL, SCHEME 2 LOGIC TEST

Purpose: Verify Scheme 2 operation of the lockout relay control logic (Reference: Figure 4.14 and Figure 4.15).

Method: 1. While the relay can use two different lockout relay control schemes, only one is enabled at a time. Select Scheme 2 by setting TRLOG = 2 in the relay setting group. Using the **SET** command, set one output to close when the 86BFT element asserts, another output contact to close when MDT asserts, and another output contact to close when the 86RS element asserts. Set the SER to trigger for the listed elements. Verify the settings with the **SHO** and the **SHO G** commands.

Setting	Elements
LDLOG, TRLOG, M86T, 50LD, 50MD, M2pu, M3pu, 52AA, TRIPA, 86BFT, 86RS	LBF, 86BFT, 86RS, MDT, 52AA, 50LD, 50MD, M86T, MODST, TRIPA

2. Enable Scheme 2 of the failure-to-trip load current logic using SET LDLOG. Save the settings. This logic sets the LBF bit based on the breaker status and the TRIPA input.

3. Connect an external timer and set it to start when the output contact programmed in Step 1 for 86BFT closes and stop when the output opens.

4. Assert the 52AA input by applying dc control voltage to the assigned input terminals.

5. Assert the TRIPA input. This action starts the relay AFpu timer of the failure to trip load logic.

6. Shortly after TRIPA input assertion, the 86BFT output should close, indicating LBF bit assertion. This action should start the external timer.

7. Deassert the TRIPA input.

8. M2pu plus M3pu cycles after the 86BFT output asserts, it should deassert, stopping the timer. The timer reading should be approximately equal to the sum of M2pu and M3pu timer settings.

9. Reconnect the timer to stop when the programmable output contact set to indicate 86RS closes.

10. Repeat Steps 4, 5, 6, and 7. Approximately 5 seconds after the 86BFT output opens, the 86RS bit should assert, causing the programmable output contact set in Step 1 to close, stopping the external timer.

11. Note the reading on the timer. Subtract the time recorded in Step 8 from the timer reading. The difference should be approximately 5 seconds (M4 fixed timer).

12. Reconnect the timer to stop when the programmable output contact set to indicate MDT closes.

13. Repeat Steps 4, 5, 6, and 7. Approximately M2pu time after the 86BFT output opens, the MDT element should assert, causing the programmable output contact set in Step 1 to close, stopping the external timer.

14. The time recorded in Step 8 minus the time recorded in Step 13 should be approximately the M3pu timer setting.

15. Reconnect the timer to start when the programmable output contact set to indicate 86RS closes and stop when that contact opens.

16. Repeat Steps 4, 5, and 6. Approximately 5 seconds after the 86BF TRIP output operates, the 86RS contact should close, then open.

17. Note the reading on the timer. The time recorded should be approximately 1 second (M1 fixed timer).

18. Optional. If you apply phase current above the 50LD setting or you assert the MODST input before or while the 86BFT output is asserted, the relay delays deassertion of the 86BFT output and assertion of the 86RS element.

19. Optional. If you apply phase current above the 50MD setting you will delay assertion or deassert MDT, delay deassertion of 86BFT, and delay assertion of 86RS.

20. For each test, the relay generated a sequential events record for the elements programmed in Step 1. View the SER using the **SER** command. Verify M1 (60 cycles) from the assertion of 86RS to the deassertion of 86RS. Verify M2pu from the assertion of 86BFT to the assertion of MDT. Verify M3pu from the assertion of MDT to the deassertion of 86BFT. Verify M4 (300 cycles) from the deassertion of 86BFT to the assertion of 86RS.

SERIAL PORTS TEST

Purpose: Verify operation of each serial PORT.

Method: Step 3 of the initial checkout procedure describes serial port connections for Ports 2, 3, and 4. Following that same procedure, verify communications on each serial port. Port 1, the EIA-485 serial port, requires an EIA-232 to EIA-485 converter and cable to connect to a computer.

IRIG-B TIME-CODE INPUT TEST

Purpose: Verify operation of the IRIG-B clock input for Serial Port 2 and the connector of Serial Port 1.

Method:

1. Connect a source of demodulated IRIG-B time code to the relay Serial Port 2 (Pins 4 (+) and 6 (–)) in series with a resistor to monitor the current. Adjust the source to obtain an "ON" current of about 10 mA.
2. Execute the **IRIG** command. Make sure the relay clock displays the correct date and time.
3. Optional. Connect the demodulated IRIG-B time code to the relay as in Step 1, but through the Serial Port 1 connector (Pins 7(+) and 8 (–)).

POWER SUPPLY VOLTAGES TEST

Purpose: Verify that +5 Vdc is present on Port 2 and 3. This voltage is sometimes required by external devices that include a dc-powered modem.

Method:

1. Execute the **STATUS** command, and inspect the voltage readings for the power supply.
2. Verify that JMP1 is installed for Serial Port 3 and JMP2 is installed for Serial Port 2. Refer to ***Section 2: Installation*** for further information about the jumpers.
3. Use a voltmeter to read the +5 V output. Pin 1 of each port should have +5 Vdc on it when the jumpers mentioned above are installed.
4. Compare the +5 V readings from the status report and voltmeter. The voltage difference should be less than 50 mV, and both readings should be within ±0.15 V of 5 V.

CALIBRATION

The SEL-352 Relay is factory calibrated. If you suspect that the relay is out of calibration, please contact the factory.

TROUBLESHOOTING

Inspection Procedure

Complete the following inspection procedure before disturbing the system. After you finish the inspection, proceed to the Troubleshooting Table.

1. Measure and record control power voltage at terminals marked + and –.
2. Check to see that the power is on, but do not turn system off if it is on.
3. Measure and record the voltage at all control inputs.
4. Measure and record the state of all output relays.
5. Inspect the cabling to the serial communications ports and be sure a communications device is connected to at least one communications port.

Troubleshooting Table

All Front-Panel LEDs Dark

1. Power is off.
2. Blown power supply fuse.
3. Input power not present.
4. Self-test failure.
5. **TAR F** command improperly set.

Note: For 1, 2, 3, and 4 the ALARM relay contacts should be closed.

System Does Not Respond to Commands

1. Communications device not connected to system.
2. Relay or communications device at incorrect baud rate or other communication parameter incompatibility, including cabling error.
3. System is processing event record. Wait several seconds.
4. System is attempting to transmit information, but cannot due to handshake line conflict. Check communications cabling.
5. System is in the XOFF state, halting communications. Type **<CTRL>Q** to put system in XON state.
6. If the serial port or front-panel interface that does not respond was working before, Steps 1–5 above have been tried, and the meter command was the last issued command, the Digital Signal Processor may have failed, and you should call the factory.

Tripping Output Relay Remains Closed Following Fault

1. Auxiliary contact inputs improperly wired.
2. Output relay contacts burned closed.
3. Interface board failure.

No Prompting Message Issued to Terminal Upon Power Up

1. Terminal not connected to system.
2. Wrong baud rate.
3. Terminal improperly connected to system.
4. SET P AUTO setting set to N (factory default).
5. Main board or interface board failure.

System Does Not Respond to Faults

1. Relay improperly set. Review your settings with **SET** and **SET G** commands.
2. Improper test settings.
3. Potential transformer or current transformer connection wiring error.
4. Analog input cable between transformer-termination and main board loose or defective.
5. Check self-test status with **STA** command.
6. Check input voltages and currents with **MET** command and TRI and EVE sequence.

Time Command Displays the Same Time for Successive Commands

1. The digital signal processor has failed; contact the factory.

Terminal Displays Meaningless Characters

1. Baud rate set incorrectly.
2. Check terminal configuration. See ***Section 8: Serial Port Communications and Commands***.

"SELBOOT" on LCD Display and Serial Port Warning to Remove Jumper (at power-up)

1. A jumper is improperly positioned at location JMP6D. Remove the jumper and repower the relay.

Self-Test Failure: +5 V

1. Power supply +5 V output out-of-tolerance. See **STATUS** command.
2. A/D converter failure.

Self-Test Failure: +15 V

1. Power supply +15 V output out-of-tolerance. See **STATUS** command.
2. A/D converter failure.

Self-Test Failure: –15 V

1. Power supply –15 V output out-of-tolerance. See **STATUS** command.
2. A/D converter failure.

Self-Test Failure: Offset

1. Offset drift.
2. A/D converter drift.
3. Loose ribbon cable between transformers and main board.

Self-Test Failure: ROM

1. Memory failure. Contact the factory.

Self-Test Failure: RAM

1. Failure of static RAM IC. Contact the factory.

Self-Test Failure: CR_RAM

1. If an R_S or saving settings process was interrupted by loss of power or CTRL-X, issue the **R_S** command again. Settings will return to factory defaults.
2. If cause of the CR_RAM is unknown, contact the factory.

Self-Test Failure: A/D Converter

1. A/D converter failure.
2. RAM error not detected by RAM test.

Self-Test Failure: IO_BRD

1. I/O board has been changed. Execute the **INITIO** command.
2. Ribbon cable disconnected between I/O board and main board. Reconnect and execute **INITIO** command.
3. Interface Board Failure.

Self-Test Failure: CR_RAM, EEPROM, and IO_BRD

1. Self-test detected setting location movement due to flash firmware upgrade. Execute **R_S** command.
2. Main board failure, contact the factory.

Alarm Contacts Closed

1. Power is off.
2. Blown fuse.
3. Power supply failure.
4. Main board or interface board failure.
5. Other self-test failure.

Self-Test Failure: Temp After R_S Command

1. Record **STA** command and state of all outputs. Call the factory. Powering down the relay will reset the logic.

FACTORY ASSISTANCE

The employee-owners of Schweitzer Engineering Laboratories are dedicated to making electric power safer, more reliable, and more economical.

We appreciate your interest in SEL products, and we are committed to making sure you are satisfied. If you have any questions, please contact us at:

Schweitzer Engineering Laboratories
2350 NE Hopkins Court
Pullman, WA USA 99163-5603
Tel: (509) 332-1890
Fax: (509) 332-7990

We provide prompt, courteous, and professional service.

We appreciate receiving any comments and suggestions about new products or product improvements that would help us make your job easier.

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APPENDIX A: FIRMWARE VERSIONS IN THIS MANUAL

To find the firmware revision number in your relay, view the status report using the serial port **STATUS** command or the front-panel STATUS pushbutton. For firmware versions prior to April 20, 2001, the status report displays the Firmware Identification (FID) label:

FID=**SEL-352-1-Rxxx-Vx-Dxxxxxx**

For firmware versions with the date code of April 20, 2001, or later, the FID label will appear as follows with the Part/Revision number in bold:

FID=**SEL-352-1-Rxxx-Vx-Z001001-Dxxxxxxxx**

The firmware revision number is after the "R" and the release date is after the "D".

This manual covers SEL-352-1 and SEL-352-2 Relays that contain firmware bearing the following part numbers and revision numbers (most recent firmware listed at top):

Flash Firmware Part/Revision No.	Description of Firmware
SEL-352-2-R202-V0-Z101101-D20010420	These firmware versions differ from previous versions as follows: • Corrected Kang setting prompt. • Removed "*" as valid element name. • Added characters (= ; : ' , / \ ? ") that can be separators in the SER triggering. • Changed the CASCII command to Level 0. • Event reporting will now show current setting after message "Setting Changed Since Last Event." • Changed the **BRE W** command to Level B. • Added checksum to STATUS report. Supports the PROTO=DNP protocol setting option.
SEL-352-2-R102-V0-Z001001-D20010420	Does not support the PROTO=DNP protocol setting option.
SEL-352-1-R103-V-D20000629 SEL-352-2-R101-V-D20000629	This firmware makes: • Internal changes to support battery-backed clock hardware change.

Flash Firmware Part/Revision No.	Description of Firmware
SEL-352-2-R100	This firmware adds: • Breaker contact wear monitoring, alarm, and preload (**BRE W**) command. • RMS overcurrent element.
SEL-352-1-R102	This firmware corrects: • Firmware R101 which incorrectly reports 0 for 86BFT, MER for 86RS, and 86BFT for MDT in the event report (EVE command).
SEL-352-1-R101	This firmware includes: • Improved Subsidence Current Logic. Fixed bug in logic which could affect performance of VAX and VAY. • 59H range changed. • IHA, IHB, IHC now allow two decimal places in SELOGIC® control equation Compares.
SEL-352-1-R100	This firmware is the initial release for the SEL-352-1 Relay. Additions were made to the SEL-352 firmware version R102 to improve performance. These include: • Subsidence Current Logic for 50FT element • Programmable Display Points • Local Bits for front-panel control • Remote Bit control via **CON n** serial port command • Nonvolatile latches • Analog Compares for SELOGIC control equations

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APPENDIX B: FIRMWARE UPGRADE INSTRUCTIONS

FIRMWARE (FLASH) UPGRADE INSTRUCTIONS

SEL may occasionally offer firmware upgrades to improve the performance of your relay. The SEL-352 Relay stores firmware in Flash memory; therefore, changing physical components is not necessary. A firmware loader program called SELBoot resides in the SEL-352 Relay. These instructions give a step-by-step procedure to upgrade the relay firmware by downloading a file from a personal computer to the relay via a serial port.

IMPORTANT NOTE REGARDING SETTINGS

The firmware upgrade procedure may result in lost relay settings due to the addition of new features and changes in the way memory is used. It is imperative to have a copy of the original relay settings available in case they need to be reentered. Carefully following these upgrade instructions will minimize the chance of inadvertently losing relay settings.

REQUIRED EQUIPMENT

- Personal computer.
- Terminal emulation software that supports XMODEM/CRC protocol (e.g., Procomm® Plus, Relay/Gold, Microsoft® Windows® Terminal and HyperTerminal, SmartCOM, or CROSSTALK®).
- Serial communications cable (SEL-234A or equivalent).
- Disk containing firmware upgrade file.

UPGRADE PROCEDURE

The instructions below assume you have a working knowledge of your personal computer terminal emulation software. In particular, you must be able to modify your serial communications parameters (baud rate, data bits, parity, etc.), disable any hardware or software flow control in your computer terminal emulation software, select transfer protocol (i.e., XMODEM/CRC), and transfer files (e.g., send and receive binary files).

1. If the relay is in service, disable its control functions.

   Note: If the SEL-352 Relay contains History (HIS) data, Event (EVE) data, or Sequential Events Recorder (SER) data that you want to retain, retrieve this information prior to performing the firmware upgrade, because all of these data sets may be erased in the upgrade procedure.

2. Connect the personal computer to the relay serial port 2, 3, or 4, and enter Access Level 2 by issuing the **ACC** and **2AC** commands.

   Note: Disconnect any other serial port connections.

3. Execute the Show Calibration (**SHO C**) command to retrieve the relay calibration settings. Record the displayed settings (or save them to a computer file) for possible reentry after the firmware upgrade.

   If you do not already have copies of the Relay, Global, Port, and SER settings, use the following Show commands to retrieve the necessary settings: **SHO 1**, **SHO 2**, **SHO 3**, **SHO 4**, **SHO 5**, **SHO 6**, **SHO G**, **SHO P 1**, **SHO P 2**, **SHO P 3**, **SHO P 4**, and **SHO R**.

   Issue the Password (**PAS**) command and save the original password settings in case they are needed later.

   Saving settings is always recommended; depending on the previously installed firmware version and how the relay uses memory, the relay may not preserve settings that existed in the relay before the upgrade.

4. Issue the **L_D <ENTER>** command to the relay (L underscore D ENTER) to start the SELBoot program.

5. Type **Y <ENTER>** to the "Disable relay to send or receive firmware (Y/N)?" prompt and **Y <ENTER>** to the "Are you sure (Y/N)?" prompt. The relay will send the SELBoot prompt !>.

   Note: SELBoot does not echo nonalphabetic characters as the first character of a line. This may make it appear that the relay is not functioning properly when just the <ENTER> key is pressed on the connected PC, even though everything is OK.

6. Issue **HEL <ENTER>** (**?<ENTER>** in earlier relays) to list the commands available in SELBoot.

```
!>help
SELboot-3xx-R100

bau "rate"  ; Set baud rate to 300, 1200, 2400, 4800, 9600, 19200, or 38400 baud
era         ; Erase the existing relay firmware
exi         ; Exit this program and restart the device
fid         ; Print the relays firmware id
rec         ; Receive new firmware for the relay using xmodem
sen         ; Send the relays firmware to a pc using xmodem
hel         ; Print this list

FLASH Type : 040         Checksum = 370E  OK
```

7. Set up your communication connection to the highest possible baud rate. The relay will support speeds up to 38400 baud. Use the **BAU** command (e.g., **BAU 38400 <ENTER>**) to change the SPEED setting to the desired baud rate.

8. Make a copy of the firmware presently in the relay. This is recommended in case the new firmware download is unsuccessful. To make a backup of the firmware, you will need approximately 2.3 MB of free disk space. The procedure takes approximately 10 minutes at 38400 baud.

   Issue the Send (**SEN <ENTER>**) command to the relay to initiate the firmware transfer from the relay to your computer. No activity will be seen on the PC screen, because the relay is waiting for the PC to request the first XMODEM data packet. Select the

"Receive File" function with the XMODEM protocol in your terminal emulation software. Give the file a unique name to clearly identify the firmware version (e.g., 352R104.S19). After the transfer, the relay will respond: "Download completed successfully!"

9. Begin the transfer of the new firmware to the relay by issuing the Receive (**REC <ENTER>)** command to instruct the relay to receive new firmware.

   Note: If the relay power fails during a firmware receive after the old firmware is erased, the relay will restart in SELBoot, but the baud rate will default to 2400 baud. (If this happens, connect to the relay at 2400 baud and type BAUD 38400 at the SELBoot prompt. The firmware receive can be started again at Step 8.)

10. The relay will ask if you are sure you want to erase the existing firmware. Type **Y** to erase the existing firmware and load new firmware, or just **<ENTER>** to abort.

11. The relay then prompts you to press a key and begin the transfer. Press a key (e.g., **<ENTER>**).

    Note: The relay will display one or more "C" characters as it waits for your PC Terminal Emulation program to send the new firmware. If you do not start the transfer quickly enough (within about 18 seconds), it may time out and respond "Remote system is not responding." If this happens, begin again in Step 8, above.

12. Start the file transfer by selecting the "Send File" function in your terminal emulation software. Use the XMODEM or 1k-XMODEM (fastest) protocol and send the file that contains the new firmware (e.g., Relay.S19).

    Note: The file transfer takes approximately 10 minutes at 38400 baud using the 1k-XMODEM protocol. After the transfer completes, the relay will reboot and return to Access Level 0. The following screen capture shows the entire process.

```
=>>L_D <ENTER>
Disable relay to send or receive firmware(Y/N) ? Y <ENTER>
Are you sure (Y/N) ? Y <ENTER>
Relay Disabled
!>SEN <ENTER>
Download completed successfully!

!>REC <ENTER>
Caution! -  This command erases the relay's firmware.
If you erase the firmware, new firmware must be loaded into the relay
before it can be put back into service.

Are you sure you wish to erase the existing firmware? (Y/N)Y
Erasing
Erase successful
Press any key to begin transfer, then start transfer at the PC <ENTER>

Upload completed successfully. Attempting a restart
```

13. The relay illuminates the EN front-panel LED if the original relay settings were retained through the download. If the EN LED is illuminated, proceed to Step 14; otherwise, the relay may display various self-test failures because of changes in the way memory is used.

If this occurs, press **<ENTER>** to see if the level 0 prompt " = " appears on your terminal screen. If it does, enter Access Level 2 by issuing the **ACC** and **2AC** commands and proceed to self-test failure: **IO_BRD**, Step 13a.

If the relay does not display the level 0 " = " prompt, the Relay baud rate has reverted to the factory default of 2400 baud. Go to Self-test failure: **CR_RAM, EEPROM,** and **IO_BRD**, Step 13d.

Self-test failure: **IO_BRD**

a. Issue the Initialize (**INI)** command to reinitialize the I/O Board(s). If this command is not available, go to Step 13e.

b. Answer **Y <ENTER>** to the question: "Are the new I/O board(s) correct (Y/N)" After about ten seconds, the EN LED will illuminate. The original relay settings have been retained but should be checked for accuracy.

c. Enter Access Level 2 by issuing the **ACC** and **2AC** commands. Go to Step 14.

Self-test failure: **CR_RAM, EEPROM,** and **IO_BRD**

d. Set your communications software settings to 2400 baud, 8 data bits, 1 stop bit. Now enter Access Level 2 by issuing the **ACC** and **2AC** commands, (see ***PAS (Passwords)*** in ***Section 8: Serial Port Communications and Commands*** for factory default passwords).

e. Issue the Restore Settings (**R_S**) command to restore the factory default settings in the relay. For a 1 Amp relay, type **R_S 1**. This takes about two minutes, after which time the EN LED will illuminate.

Note: If the relay asks for a part number to be entered, use the number from the label on the firmware diskette, or from the new part number sticker (if supplied).

f. Enter Access Level 2 by issuing the **ACC** and **2AC** commands, (see ***PAS (Passwords)*** in ***Section 8: Serial Port Communications and Commands*** for factory default passwords).

g. Restore the original settings as necessary with each of the following commands: **SET 1**, **SET 2**, **SET 3**, **SET 4**, **SET 5**, **SET 6**, **SET G**, **SET P 1**, **SET P 2**, **SET P 3**, **SET P 4**, **SET R**.

h. Use the **PAS** command to set the original relay passwords you saved earlier in Step 3.

For example, **PAS 1:Ot3579 <ENTER>** sets the level 1 password to Ot3579. Use a similar format for **PAS B** and **PAS 2**. The **PAS** command is case-sensitive, so the lower- and upper-case letters are treated differently.

If any FAIL codes show on the Relay LCD, see ***Section 11: Testing and Troubleshooting.***

14. Verify the calibration settings by issuing the **SHO C** command. If the settings do not match the settings recorded in Step 3, reissue the settings with the **SET C** command.

(To change the calibration settings, you will need to first enter the calibration access level by typing **CAL <ENTER>**, and the password **CLARKE <ENTER>**.)

15. Execute the Status (**STA)** command to verify that all relay self-test parameters are within tolerance.

16. Apply current and voltage signals to the relay. Issue the **MET** command and verify that the current and voltage signals are correct. Issue the Trigger (**TRI)** and Event (**EVE)** commands. Verify that the current and voltage signals are correct in the event report.

The relay is now ready for your commissioning procedure.

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APPENDIX C: SEL DISTRIBUTED PORT SWITCH PROTOCOL (LMD)

The SEL Distributed Port Switch Protocol (LMD) enables multiple SEL relays to share a common communications channel. This protocol is appropriate for low-cost, low-speed port switching applications where updating a real-time database is not a requirement.

SETTINGS

Use the front-panel **SET P** command to activate the LMD protocol. Change the PROTOCOL port setting from the default SEL to LMD to reveal the following settings:

ADDRESS: Two character ASCII address. The range is "01" to "99". The default is "01".

PREFIX: One character to precede the address. This should be a character that does not occur in the course of other communications with the relay. Valid choices are one of the following: "@" "#" "$" "%" "&". The default is "@".

SETTLE TIME: Time in seconds that transmission is delayed after the request to send (RTS line) asserts. This delay accommodates transmitters with a slow rise time.

OPERATION

1. The relay ignores all input from this port until it detects the prefix character and the two-byte address.
2. Then, it asserts the RTS line, which you can use to key a serial data transmitter. The relay enables echo and message transmission. If the port had received an XOFF character, the relay performs as if it received an XON. The relay then issues the Access Level 0 prompt.
3. Until the relay connection terminates, you can use the standard commands that are available when PROTOCOL is set to SEL.
4. The **QUIT** command terminates the connection. If no ASCII (not *Fast Meter* or *Fast Operate*) data are sent to the relay before the port time-up period, it automatically terminates the connection. Receipt of a valid prefix character terminates the connection.
5. Terminating the connection aborts in-progress transmissions.
6. Enter the sequence CTRL-X QUIT <CR> before entering the prefix character if all relays in the multidrop network do not have the same prefix setting.

Note: You can use the front-panel **SET** command to change the port settings to return to SEL protocol.

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APPENDIX D: CONFIGURATION, *FAST METER*, AND *FAST OPERATE* COMMANDS

INTRODUCTION

SEL relays have two separate data streams that share the same serial port. The human data communications with the relay consist of ASCII character commands and reports that are intelligible to humans using a terminal or terminal emulation package. The binary data streams can interrupt the ASCII data stream to obtain information and then allow the ASCII data stream to continue. This mechanism allows a single communications channel to be used for ASCII communications (e.g., transmission of a long event report) interleaved with short bursts of binary data to support fast acquisition of metering data. The device connected to the other end of the link requires software that uses the separate data streams to exploit this feature. The binary commands and ASCII commands can also be accessed by a device that does not interleave the data streams.

SEL Application Guide AG95-10, Configuration and Fast Meter Messages, is a comprehensive description of the SEL binary messages. Below is a description of the messages provided in the SEL-352 Relay.

MESSAGE LISTS

Binary Message List

Request to Relay (hex)	Description of Response from Relay
A5C0	Relay Definition Block
A5C1	*Fast Meter* Configuration Block
A5D1	*Fast Meter* Data Block
A5B9	*Fast Meter* Status Acknowledge
A5CE	*Fast Operate* Configuration Block
A5E0	*Fast Operate* Remote Bit Control
A5E3	*Fast Operate* Breaker Control

ASCII Configuration Message List

Request to Relay (ASCII)	Description of Response from Relay
ID	ASCII Firmware ID, Terminal ID Setting (TRMID) and Modbus code
DNA	ASCII Names of Relay Word bits
BNA	ASCII Names of bits in the A5B9 Status Byte

MESSAGE DEFINITIONS

A5C0 Relay Definition Block

In response to the A5C0 request, the relay sends the following block:

Data	Description
A5C0	Command
2A	Length
02	Support three protocols, SEL, LMD, and DNP
01	Support one *Fast Meter* message
03	Three status flag commands
A5C1	*Fast Meter* configuration command
A5D1	*Fast Meter* command
0002	Self-test warning bit
5354410D0000(STA<CR>)	Check status (ASCII characters, <CR>, binary zeros)
0003	Self-test failure bit
5354410D0000(STA<CR>)	Check status (ASCII characters, <CR>, binary zeros)
0004	Settings change bit
A5C100000000	Reconfigure *Fast Meter* configuration (hex)
0100	SEL protocol, *Fast Operate*
0101	LMD protocol, *Fast Operate*
0005	DNP protocol
00	Reserved for future use
checksum	1-byte checksum of preceding bytes

A5C1 *Fast Meter* Configuration Block

In response to the A5C1 request, the relay sends the following block:

Data	Description
A5C1	*Fast Meter* command
94 (hex)	Length
01	One status flag byte
01	Scale factors in *Fast Meter* configuration message
03	Three scale factors
09	Nine analog input channels
04	Four samples per channel
50 (hex)	80 digital banks
02	Two calculation blocks
0004	Analog channel offset
004C	Time stamp offset
0054	Digital offset
564158000000	Analog channel name (VAX)
00	Analog channel type (integer)
01	Scale factor type (float)
008A	Scale factor offset (hex)
494100000000	Analog channel name (IA)
00	Analog channel type (integer)

01	Scale factor type (float)
0086	Scale factor offset (hex)
564159000000	Analog channel name (VAY)
00	Analog channel type (integer)
01	Scale factor type (float)
008E	Scale factor offset (hex)
564258000000	Analog channel name (VBX)
00	Analog channel type (integer)
01	Scale factor type (float)
008A	Scale factor offset (hex)
494200000000	Analog channel name (IB)
00	Analog channel type (integer)
01	Scale factor type (float)
0086	Scale factor offset (hex)
564259000000	Analog channel name (VBY)
00	Analog channel type (integer)
01	Scale factor type (float)
008E	Scale factor offset (hex)
564358000000	Analog channel name (VCX)
00	Analog channel type (integer)
01	Scale factor type (float)
008A	Scale factor offset (hex)
494300000000	Analog channel name (IC)
00	Analog channel type (integer)
01	Scale factor type (float)
0086	Scale factor offset (hex)
564359000000	Analog channel name (VCY)
00	Analog channel type (integer)
01	Scale factor type (float)
008E	Scale factor offset (hex)
00 or 01	00 - PHROT=ABC, 01 - PHROT=ACB
00	Standard power calculation using 6 channels
FFFF	No skew adjustment (-1)
FFFF	No Rs compensation (-1)
FFFF	No Xs compensation (-1)
01	Channel index IA
04	IB
07	IC
00	VAX
03	VBX
06	VCX
00 or 01	00 - PHROT=ABC, 01 - PHROT=ACB
02	Calculate 3 voltage channels only
FFFF	No skew adjustment (-1)
FFFF	No Rs compensation (-1)
FFFF	No Xs compensation (-1)
FF	Channel index No index (-1)
FF	No index (-1)
FF	No index (-1)

02	VAY
05	VBY
08	VCY
4-bytes	Current scale factor 200 * CTR /√2, (floating point)
4-bytes	X voltage scale factor 200 * XPTR /√2, (floating point)
4-bytes	Y voltage scale factor 200 * YPTR /√2, (floating point)
00	Reserved for future use
1-byte	Checksum of all preceding bytes

A5D1 *Fast Meter* Data Block

In response to the A5D1 request, the relay sends the following block:

Data	Description
A5D1	Command
A6	Message length (hex)
1-byte	Status byte
72 bytes	The first, second, fifth, and six quarter-cycle sample, with each sample sent as integers in the following order: VAX, IA, VAY, VBX, IB, VBY, VCX, IC, VCY
8-bytes	Time stamp
80-bytes	Relay Word bits (see DNA message for bit map)
1-byte	Reserved for future use
1-byte	Checksum of all preceding bytes

A5B9 *Fast Meter* Status Acknowledge Message

The relay clears the *Fast Meter* (message A5D1) Status Byte when it receives the A5B9 request. The Status Byte contains three active bits as follows:

Data	Name	Set Criteria	Reset Criteria
bit 2	STWARN	Self-test warning	A5B9 Status Acknowledge Message is received or Diagnostics pass after a power up
bit 3	STFAIL	Self-test failure	A5B9 Status Acknowledge Message is received or Diagnostics pass after a power up
bit 4	STSET	Settings change or power up	A5B9 Status Acknowledge Message is received

If Bit 2 or 3 are set as determined by the A5D1 *Fast Meter* Data Block, the data should be recorded and the relay inspected. A5B9 clears these bits, but the warning or failure is not cleared. The relay must be inspected. If Bit 4 is set as determined by the A5D1 *Fast Meter* Data Block, the external device should request the A5C1 *Fast Meter* Configuration Block. The external device can then determine if the scale factors or line configuration parameters have been modified.

A5CE *Fast Operate* Configuration Block

In response to the A5CE request, the relay sends the following block:

Data	Description
A5CE	Command
3C	Message length (hex)
01	Support one circuit breaker
0010	Support 16 remote bits
01	Allow remote bit pulse commands
00	Reserved for future use
31	Operate code, open breaker
11	Operate code, close breaker
00	Operate code, clear remote bit RB1
20	Operate code, set remote bit RB1
40	Operate code, pulse remote bit RB1
01	Operate code, clear remote bit RB2
21	Operate code, set remote bit RB2
41	Operate code, pulse remote bit RB2
02	Operate code, clear remote bit RB3
22	Operate code, set remote bit RB3
42	Operate code, pulse remote bit RB3
03	Operate code, clear remote bit RB4
23	Operate code, set remote bit RB4
43	Operate code, pulse remote bit RB4
04	Operate code, clear remote bit RB5
24	Operate code, set remote bit RB5
44	Operate code, pulse remote bit RB5
05	Operate code, clear remote bit RB6
25	Operate code, set remote bit RB6
45	Operate code, pulse remote bit RB6
06	Operate code, clear remote bit RB7
26	Operate code, set remote bit RB7
46	Operate code, pulse remote bit RB7
07	Operate code, clear remote bit RB8
27	Operate code, set remote bit RB8
47	Operate code, pulse remote bit RB8
08	Operate code, clear remote bit RB9
20	Operate code, set remote bit RB9
40	Operate code, pulse remote bit RB9
09	Operate code, clear remote bit RB10
29	Operate code, set remote bit RB10
49	Operate code, pulse remote bit RB10
0A	Operate code, clear remote bit RB11
2A	Operate code, set remote bit RB11
4A	Operate code, pulse remote bit RB11
0B	Operate code, clear remote bit RB12
2B	Operate code, set remote bit RB12
4B	Operate code, pulse remote bit RB12
0C	Operate code, clear remote bit RB13

2C	Operate code, set remote bit RB13
4C	Operate code, pulse remote bit RB13
0D	Operate code, clear remote bit RB14
2D	Operate code, set remote bit RB14
4D	Operate code, pulse remote bit RB14
0E	Operate code, clear remote bit RB15
2E	Operate code, set remote bit RB15
4E	Operate code, pulse remote bit RB15
0F	Operate code, clear remote bit RB16
2F	Operate code, set remote bit RB16
4F	Operate code, pulse remote bit RB16
00	Reserved
1-byte	Checksum of all preceding bytes

A5E0 *Fast Operate* Remote Bit Control

Fast Operate Remote Bit Control is suspended during relay setting changes, a setting group change, power-up, or if the relay is disabled. The external device sends the following message to perform a remote bit operation:

Data	Description
A5E0	Command
06	Message length (hex)
1-byte	Operate code: 00 - 0F clear remote bit RB1 - RB16 20 - 2F set remote bit RB1 - RB16 40 - 4F pulse (1/8 - cycle) remote bit RB1 - RB16
1-byte	Operate validation: 4 · Operate code + 1
1-byte	Checksum of all preceding bytes

The relay performs the specified remote bit operation if the following conditions are true:

- The Operate code is a valid code
- The Operate validation = 4 · Operate code + 1
- The message checksum is valid
- The FAST_OP port setting is set to Y
- The relay is enabled

Remote bit set and clear operations are latched by the relay. Remote bit pulse operations assert the remote bit for one processing interval (1/8 cycle).

A5E3 *Fast Operate* Breaker Control

The external device sends the following message to perform a fast breaker open/close:

Data	Description
A5E3	Command
06	Message length
1-byte	Operate code (hex): 31 - asserts the TCMD bit for 30 cycles to open the breaker 11 - asserts the CCMD bit for 30 cycles to close the breaker
1-byte	Operate Validation: 4 · Operate code + 1
1-byte	Checksum of all preceding bytes

The relay performs the specified breaker operation if the following conditions are true:

- The Operate code is a valid code
- The Operate validation = 4 · Operate code + 1
- The message checksum is valid
- The FAST_OP port setting is set to Y
- The relay is enabled
- The BREAKER jumper JMP6B is in place on the SEL-352 Relay main board

ID Command Response

In response to the **ID** command, the relay sends the firmware ID, relay TRMID setting, and the Modbus device code as follows:

<STX>"FID STRING ENCLOSED IN QUOTES","yyyy" <CR>
"TRMID SETTING ENCLOSED IN QUOTES","yyyy" <CR>
31, "yyyy" <CR>
<ETX>

where <STX> is the STX character (02)
<CR> is the carriage return character (13)
<ETX> is the ETX character (03)
yyyy is the 4-byte ASCII hex representation of the checksum for each line
31 is the SEL-2020 Modbus code to identify relay type

The ID message is available from Access Level 1 and higher.

DNA Command Response

In response to the **DNA** command, the relay sends names of the Relay Word bits transmitted in the A5D1 message. The first name is associated with the MSB, the last name with the LSB. Only the first row is shown as an example, but all labels are listed in ***Appendix F: Relay Word***. The **DNA** command response is formatted as follows:

<STX>"EN","PF","86BFT","86RS","TRIP","CLOSE","52A","MOD","0B43"<CR>

"xxxxx","xxxxx","xxxxx","xxxxx","xxxxx","xxxxx","xxxxx","xxxxx","yyyy"<CR>
:
: (A total of 80 rows of 8 digital element labels and their checksum)
:
"xxxxx","xxxxx","xxxxx","xxxxx","xxxxx","xxxxx","xxxxx","xxxxx","yyyy"<CR>
<ETX>

where <STX> is the STX character (02)
<CR> is the carriage return character (13)
<ETX> is the ETX character (03)
yyyy is the 4-byte ASCII hex representation of the checksum for the line
"*" indicates an unused bit location.

The **DNA** command is available from Access Level 1 and higher.

BNA Command Response

In response to the **BNA** command, the relay sends names of the bits transmitted in the Status Byte in the A5D1 message. The first name is the MSB, the last name is the LSB. The BNA message is:

<STX>"*","*","*","STSET","STFAIL","STWARN","*","*","0987"<CR>
<ETX>

where: "0987" is the 4-byte ASCII hex representation of the checksum
"*" indicates an unused bit location.

The **BNA** command is available from Access Level 1 and higher.

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APPENDIX E: COMPRESSED ASCII COMMANDS

INTRODUCTION

The SEL-352 Relay provides Compressed ASCII versions of some of the relay's ASCII commands. The Compressed ASCII commands allow an external device to obtain data from the relay, in a format which directly imports into spreadsheet or database programs, and which can be validated with a checksum.

The SEL-352 Relay provides the following Compressed ASCII commands:

Command	Description
CASCII	Configuration message
CSTATUS	Status report
CBREAKER	Breaker report
CHISTORY	History report
CTARGET	Target report
CEVENT	Event report

CASCII COMMAND

The compressed ASCII configuration message provides data for an external computer to extract data from other compressed ASCII commands. The following example includes the lines an SEL-352-2 Relay would send to describe the Percent Wear feature. To obtain the configuration message for the compressed ASCII commands available in the SEL-352 relay, type:

CAS <CR>

The relay sends:
<STX>"CAS",7,"01A8"<CR>
"CST",1,"01B7"<CR>
"1H","FID","022C"<CR>
"1D","35S","0210"<CR>
"7H","MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0E52"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"24H","IA","IB","IC","VAX","VBX","VCX","VAY","VBY","VCY","MOF","+5V_PS","+5V_REG","-5V_REG","+12V_PS","-12V_PS","+15V_PS","-15V_PS","TEMP","RAM","ROM","A/D","CR_RAM","EEPROM","IO_BRD","2A29"<CR>
"1D","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","9S","1885"<CR>
"CBR",1,"01A4"<CR>
"1H","FID","022C"<CR>
"1D","35S","0210"<CR>
"7H","MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0E52"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"3H","MONTH_CLRD","DAY_CLRD","YEAR_CLRD","0A5C"<CR>
"1D","I","I","I","0310"<CR>
"7H","TRIPA","TRIPB","TRIPC","CLOSEA","CLOSEB","CLOSEC","LABEL","0F0A"<CR>

"7D","F","F","F","F","F","F","10S","0653"<CR>
"4H","TRIPA","TRIPB","TRIPC","LABEL","088F"<CR>
"1D","I","I","I","10S","0434"<CR>
"CHI",1,"01A1"<CR>
"1H","FID","022C"<CR>
"1D","35S","0210"<CR>
"7H","MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0E52"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"10H","REC_NUM","MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","EVENT","
GROUP","126B"<CR>
"40D","I","I","I","I","I","I","I","I","7S","I","0893"<CR>
"CTA",1,"01A5"<CR>
"8h","6S","6S","6S","6S","6S","6S","6S","6S","08D8"<CR>
"1D","I","I","I","I","I","I","I","I","06AD"<CR>
"CEV",1,"01AB"<CR>
"1H","FID","022C"<CR>
"1D","35S","0210"<CR>
"7H","MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0E52"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"5H","FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","0E10"<CR>
"1D","F","I","I","I","7S","04C0"<CR>
"11H","VAY(kV)","VBY(kV)","VCY(kV)","VAX(kV)","VBX(kV)","VCX(kV)","IA","IB","IC
","TRIG","DIGITAL ELEMENT NAMES","yyyy"<CR>
"60D","F","F","F","F","F","F","F","F","F","1S","24S","099D"<CR>
"CEV C",1,"020E"<CR>
"1H","FID","022C"<CR>
"1D","35S","0210"<CR>
"7H","MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0E52"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"5H","FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","0E10"
"1D","F","I","I","I","7S","04C0"<CR>
"11H","VAY(kV)","VBY(kV)","VCY(kV)","VAX(kV)","VBX(kV)","VCX(kV)","IA","IB","IC
","TRIG","DIGITAL ELEMENT NAMES","yyyy"<CR>
"240D","F","F","F","F","F","F","F","F","F","F","1S","24S","09CD"<CR>
"CEV S64",1,"0288"<CR>
"1H","FID","022C"<CR>
"1D","35S","0210"<CR>
"7H","MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0E52"<CR>
"1D","I","I","I","I","I","I","I","05F4"<CR>
"5H","FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","0E10"<CR>
"1D","F","I","I","I","7S","04C0"<CR>
"11H","VAY(kV)","VBY(kV)","VCY(kV)","VAX(kV)","VBX(kV)","VCX(kV)","IA","IB","IC
","TRIG","DIGITAL ELEMENT NAMES","yyyy"<CR>
"960D","F","F","F","F","F","F","F","F","F","F","1S","24S","09D6"<CR>
<ETX>

where:
yyyy two byte ASCII checksum

DIGITAL ELEMENT NAMES
Names of digital elements separated by spaces.

#H identifies a header line to precede one or more data lines, '#' is the number of subsequent ASCII names. For example "21H" identifies a header line with 21 ASCII labels.

#h identifies a header line to precede one or more data lines, '#' is the number of subsequent format fields. For example "8h" identifies a header line with 8 format fields.

#D identifies a data format line, '#' is the maximum number of subsequent data lines, each format field contains one of the following type designators:

- I Integer data
- F Floating point data
- mS String of maximum m characters (e.g. 10S for a 10 character string)

A compressed ASCII command may require multiple header and data configuration lines.

If a compressed ASCII request is made for data that are not available, (e.g. the history buffer is empty or invalid event request), the relay responds with the following message:

<STX>"No Data Available","0668"<CR><ETX>

CSTATUS COMMAND

Display status data in compressed ASCII format by sending:

CST <CR>

The relay sends:
<STX>"FID","0143"<CR>
"FID=SEL-352-1-XXXX-DXXXXXX","yyyy"<CR>
"MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0D63"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"yyyy"<CR>
"IA","IB","IC","VAX","VBX","VCX","VAY","VBY","VCY","MOF","+5V_PS","+5V_REG","-5V_REG","+12V_PS","-12V_PS","+15V_PS","-15V_PS","TEMP","RAM","ROM","A/D","CR_RAM","EEPROM","IO_BRD","290B"<CR>
"xxxx","yyyy"<CR><ETX>

where xxxx are the data values corresponding to the first line labels and
yyyy is the 4-byte hex ASCII representation of the checksum.

CBREAKER COMMAND

The following example includes the lines an SEL-352-2 Relay would send to describe the Percent Wear feature. Display breaker summary data in compressed ASCII format by sending:

CBR <CR>

The relay sends:
<STX>"FID","0143"<CR>
"FID=SEL-352-1-XXXX-DXXXXXX","yyyy"<CR>
"MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0D63"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"yyyy"<CR>
"MONTH_CLRD","DAY_CLRD","YEAR_CLRD","0971"<CR>
xx,xx,xxxx,"yyyy"<CR>
"TRIPA","TRIPB","TRIPC","CLOSEA","CLOSEB","CLOSEC","LABEL","0E1B"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"OPERATIONS","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"AVE_ELECT","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"AVE_MECH","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"LAST_ELECT","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx"LAST_MECH","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"TOT_ENERGY","yyyy"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"TOT_CURR","yyyy"<CR>
"TRIPA","TRIPB","TRIPC","LABEL","07A3"<CR>
xxxx,xxxx,xxxx,"PCT_WEAR","yyyy"<CR>

<ETX>

where the second month, day, and year correspond to last time breaker summary was cleared

xxxx are the data values corresponding to the first line labels and
yyyy is the 4-byte hex ASCII representation of the checksum.

CHISTORY COMMAND

Display history data in compressed ASCII format by sending:

CHI <CR>

The relay sends:
<STX>"FID","0143"<CR>
"FID=SEL-352-1-XXXX-DXXXXXX","yyyy"<CR>
"MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0D63"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"yyyy"<CR>
"REC_NUM",MONTH","DAY","YEAR","HOUR","MIN","SEC","MSEC","EVENT","GROUP
","1130"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"xxxx",xxxx,"yyyy"<CR>
(the second line is then repeated for each record)
<ETX>

where xxxx are the data values corresponding to the first line labels and
yyyy is the 4-byte hex ASCII representation of the checksum.

CTARGET COMMAND

Display target data in compressed ASCII format by sending:

CTA n <CR>

where n is one of the target numbers or element names accepted by the **TAR** command. If n is omitted, 0 is used.

The relay sends:

<STX>"llll","llll","llll","llll","llll","llll","llll","llll","yyyy" <CR>
x,x,x,x,x,x,x,x,"yyyy" <CR><ETX>

where llll are the labels for the given target,
x is 0 or 1 corresponding to the first line labels, and
yyyy is the 4-byte hex ASCII representation of the checksum.

CEVENT COMMAND

The CEV report contains every digital element found in an EVE. Display event report in compressed ASCII format by sending:

CEV n m <CR>

where n is the number of the event report, as used in the **EVE** command, and m is the format selector(s), as seen above. If no parameters are specified, the relay defaults to four samples per cycle resolution and an event report length of 15 cycles. This default response is required for compatibility with the SEL-2020 and SEL-2030.

The relay sends:
<STX>"FID","0143"<CR>
"FID=SEL-352-1-XXXX-DXXXXXX","yyyy"<CR>
"MONTH_","DAY_","YEAR_","HOUR_","MIN_","SEC_","MSEC_","0D63"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,"yyyy"<CR>
"FREQ","SAM/CYC_A","SAM/CYC_D","NUM_OF_CYC","EVENT","0D23"<CR>
xxxx,xxxx,xxxx,xxxx,"xxxx","yyyy"<CR>
"VAY(kV)","VBY(kV)","VCY(kV)","VAX(kV)","VBX(kV)","VCX(kV)","IA","IB","IC","TRI
G","Y59L3 X59L3 50LDC 50LDB 50LDA 50FTC 50FTB 50FTA 87THA 87FOA Y27D3
X27D3 50N 50MDC 50MDB 50MDA 47Q 37OP 25T 46P 87THC 87FOC 87THB 87FOB
X59LC X59HC X27DB X59LB X59HB X27DA X59LA X59HA * * IN106 IN105 IN104 IN103
IN102 IN101 MCLOSE CLOSE TRIP3 TRIPC TRIPB TRIPA SS2 SS1 * LODCT LOD2 LOD1
MODST 52AC 52AB 52AA * KTRK 26TFC 26TFB 26TFA 26CFC 26CFB 26CFA UBBF
UBPF FOBF FOPF CTF TTF LBF LPF RTC RTB RTA CCC CCB CCA LODBF LODPF * * *
MER 86BFT 86RS MDT FBF !ALARM OUT107 OUT106 OUT105 OUT104 OUT103
OUT102 OUT101","8BBE"<CR>
xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,xxxx,z,"RLY_BITS","yyyy"<CR>

(the previous line is then repeated for each record)
<ETX>
where xxxx are the data values corresponding to the preceding label lines.
yyyy is the 4-byte hex ASCII representation of the checksum.
z is ">" for pre-fault record and empty for all others.
RLY_BITS refers to the relay element data in hex ASCII.

For example, if the RLY_BITS = “9B240000000000000000000” (1001101100100100...) then Y59L3, 50LDB, 50LDA, 50FTB, 50FTA, Y27D3, 50MDC would be set and the rest of the elements would be clear.

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TABLES

APPENDIX F: RELAY WORD

The SEL-352 Relay Word is a list of logical bits that indicate relay logic decisions. The following tables give the labels of each bit. The complete Relay Word is broken up into sections by relay logic element types. The row number is used with the **TARGET n <ENTER>** command for displaying the status of each bit in that particular row. A description of each bit listed alphabetically follows. Row 16 Relay Word bits (BCW, 50R, 50RA, 50RB, and 50RC) are only available in the SEL-352-2 Relay.

Table F.1: Relay Word

Row	Relay Word Labels							
	Front-Panel Targets (not for use in SELOGIC® Control Equations)							
0	EN	PF	86BFT	86RS	TRIP	CLOSE	52A	MOD
1	FAULT	LOAD	UBAL	FLASH	THERM	A	B	C
	General Elements							
2	Y59L3	X59L3	50LDC	50LDB	50LDA	50FTC	50FTB	50FTA
3	87THA	87FOA	Y27D3	X27D3	50N	50MDC	50MDB	50MDA
4	47Q	37OP	25T	46P	87THC	87FOC	87THB	87FOB
5	X59LC	X59HC	X27DB	X59LB	X59HB	X27DA	X59LA	X59HA
6	ZERO	Y27DC	Y59LC	Y27DB	Y59LB	Y27DA	Y59LA	X27DC
7	ONE	50MNC	50MNB	50MNA	87F	87H	87TH	X59H
8	25M	25C	46C	46B	46A	50MD	50LD	50FT
9	Y47Q	X47Q	37OPC	37OPB	37OPA	87HC	87HB	87HA
10	CCMD	TCMD	XNTC	XPTC	XNTB	XPTB	XNTA	XPTA
11	*	*	YNTC	YPTC	YNTB	YPTB	YNTA	YPTA
12	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1
13	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9
14	LB8	LB7	LB6	LB5	LB4	LB3	LB2	LB1
15	LB16	LB15	LB14	LB13	LB12	LB11	LB10	LB9
16	*	*	*	BCW	50R	50RC	50RB	50RA
17	*	*	IN106	IN105	IN104	IN103	IN102	IN101
18	IN208	IN207	IN206	IN205	IN204	IN203	IN202	IN201
19	IN216	IN215	IN214	IN213	IN212	IN211	IN210	IN209
20	IN308	IN307	IN306	IN305	IN304	IN303	IN302	IN301
21	IN316	IN315	IN314	IN313	IN312	IN311	IN310	IN309
22	MCLOSE	CLOSE	TRIP3	TRIPC	TRIPB	TRIPA	SS2	SS1
23	*	LODCT	LOD2	LOD1	MODST	52AC	52AB	52AA
	SELOGIC Control Equation SET A Elements							
24	L1CR	L1CS	L1BQ	L1BR	L1BS	L1AQ	L1AR	L1AS
25	*	T1CD	T1C	T1BD	T1B	T1AD	T1A	L1CQ
26	*	*	*	*	*	SAC	SAB	SAA
	Fault Current Protection Elements							
27	LFAR	LFAS	TTCD	TTC	TTBD	TTB	TTAD	TTA
28	*	LFCQ	LFCR	LFCS	LFBQ	LFBR	LFBS	LFAQ
29	*	*	FCCD	FCC	FCBD	FCB	FCAD	FCA

				Load Current Protection Elements				
30	LLCR	LLCS	LLBQ	LLBR	LLBS	LLAQ	LLAR	LLAS
31	LDA	LPCD	LPC	LPBD	LPB	LPAD	LPA	LLCQ
32	L52Q	L52R	L52S	LDCD	LDC	LDBD	LDB	LDAD
33	*	*	*	*	AFD	AF	APD	AP
				Resistor Thermal Protection Elements				
34	LTAR	LTAS	OPCD	OPC	OPBD	OPB	OPAD	OPA
35	*	LTCQ	LTCR	LTCS	LTBQ	LTBR	LTBS	LTAQ
36	*	*	CRMEC	CRMEB	CRMEA	TRMEC	TRMEB	TRMEA
37	*	KTRK	26TFC	26TFB	26TFA	26CFC	26CFB	26CFA
38	*	*	26TPC	26TPB	26TPA	26CPC	26CPB	26CPA
				Flashover Protection Elements				
39	F2AD	F2A	F1CD	F1C	F1BD	F1B	F1AD	F1A
40	F3BD	F3B	F3AD	F3A	F2CD	F2C	F2BD	F2B
41	LHBQ	LHBR	LHBS	LHAQ	LHAR	LHAS	F3CD	F3C
42	LVBR	LVBS	LVAQ	LVAR	LVAS	LHCQ	LHCR	LHCS
43	FPBD	FPB	FPAD	FPA	LVCQ	LVCR	LVCS	LVBQ
44	FFCD	FFC	FFBD	FFB	FFAD	FFA	FPCD	FPC
				Unbalance Protection Elements				
45	*	UPAD	UPA	LUQ	LUR	LUS	UCD	UC
46	UFBD	UFB	UFAD	UFA	UPCD	UPC	UPBD	UPB
47	*	*	*	*	*	*	UFCD	UFC
				Loss-of-Dielectric Protection Elements				
48	*	*	LT3D	LT3	LT2D	LT2	LT1D	LT1
				Controlled Close Elements				
49	MCT	RCCD	RCC	RCBD	RCB	RCAD	RCA	RCLS
50	PCPA	SCTD	SCT	SYNCTD	SYNCT	CCTD	CCT	MCTD
51	ZCPB	ZCNA	ZCPA	PCNC	PCPC	PCNB	PCPB	PCNA
52	*	SYNCEN	CTCD	CTBD	CTAD	ZCNC	ZCPC	ZCNB
				Breaker Alarm Elements				
53	CAMT	BPF	BDNC	TWO	CWO	52ACV	FCRS	FTRS
54	*	*	*	BALRM	PTD	SC	ST	MCC
				Circuit Breaker Retrip Elements				
55	LRTCR	LRTCS	LRTBQ	LRTBR	LRTBS	LRTAQ	LRTAR	LRTAS
56	*	RT3D	RT3	RT2D	RT2	RT1D	RT1	LRTCQ
				SELOGIC Control Equation SET B Elements				
57	L2CR	L2CS	L2BQ	L2BR	L2BS	L2AQ	L2AR	L2AS
58	L3CS	L3BQ	L3BR	L3BS	L3AQ	L3AR	L3AS	L2CQ
59	T2CD	T2C	T2BD	T2B	T2AD	T2A	L3CQ	L3CR
60	L4CR	L4CS	L4BQ	L4BR	L4BS	L4AQ	L4AR	L4AS
61	L5CS	L5BQ	L5BR	L5BS	L5AQ	L5AR	L5AS	L4CQ
62	T3CD	T3C	T3BD	T3B	T3AD	T3A	L5CQ	L5CR
63	L6CR	L6CS	L6BQ	L6BR	L6BS	L6AQ	L6AR	L6AS

64	L7CS	L7BQ	L7BR	L7BS	L7AQ	L7AR	L7AS	L6CQ
65	*	*	*	SBC	SBB	SBA	L7CQ	L7CR
				Logic Output Elements				
66	UBBF	UBPF	FOBF	FOPF	CTF	TTF	LBF	LPF
67	RTC	RTB	RTA	CCC	CCB	CCA	LODBF	LODPF
68	*	*	*	*	*	*	*	FBF
				86BF Trip and Reset Elements				
69	M2D	M2	L1MQ	L1MR	L1MS	M1D	M1	M86T
70	L3MQ	L3MR	L3MS	M3D	M3	L2MQ	L2MR	L2MS
71	*	MER	86BFT	86RS	MDT	M4D	M4	*
72	*	*	*	*	*	CTC	CTB	CTA
				Contact Output Elements and Display Points				
73	!ALARM	OUT107	OUT106	OUT105	OUT104	OUT103	OUT102	OUT101
74	OUT201	OUT202	OUT203	OUT204	OUT205	OUT206	OUT207	OUT208
75	OUT209	OUT210	OUT211	OUT212	OUT213	OUT214	OUT215	OUT216
76	OUT301	OUT302	OUT303	OUT304	OUT305	OUT306	OUT307	OUT308
77	OUT309	OUT310	OUT311	OUT312	OUT313	OUT314	OUT315	OUT316
78	DP8	DP7	DP6	DP5	DP4	DP3	DP2	DP1
79	DP16	DP15	DP14	DP13	DP12	DP11	DP10	DP9

Table F.2: Relay Word Bit Summary Table

Elements Alphabetically	Description	Relay Word Row
!ALARM	Asserted when there is no self-test ALARM condition	73
*	The asterisk symbol is a place holder for an unused element	Many
25C 25M 25T	Synchronism check element for C - automatic close, M - manual close, and T - either.	8 8 4
26CFA 26CFB 26CFC	Close resistor Failure for phase A, B, or C	37 37 37
26CPA 26CPB 26CPC	Close resistor Pending failure for phase A, B, or C	38 38 38
26TFA 26TFB 26TFC	Trip resistor Failure for phase A, B, or C	37 37 37
26TPA 26TPB 26TPC	Trip resistor Pending failure for phase A, B, or C	38 38 38

Elements Alphabetically	Description	Relay Word Row
37OP 37OPA 37OPB 37OPC	OverPower elements for A-, B-, or C-phase, and a general element for assertion of any phase	4 9 9 9
46A 46B 46C 46P	Current unbalance elements for A-, B-, or C-phase and a general element for assertion of any phase	8 8 8 4
47Q	Negative-sequence overvoltage element, Asserts when either X47Q or Y47Q asserts (operates on V_2)	4
50FT 50FTA 50FTB 50FTC	Overcurrent element for Fault conditions for A-, B-, or C-phase and a general element for assertion of any phase. 50FT=50FTA+50FTB+50FTC	8 2 2 2
50LD 50LDA 50LDB 50LDC	Overcurrent element for Load or Line charging current conditions for A-, B-, or C-phase and a general element for assertion of any phase.	8 2 2 2
50MD 50MDA 50MDB 50MDC	Overcurrent element for Motor operated disconnect conditions for A-, B-, or C-phase and a general element for assertion of any phase.	8 3 3 3
50MNA 50MNB 50MNC	Minimum current detector (1 A secondary) for A-, B-, or C-phase	7 7 7
50N	Ground overcurrent element (operates on $3I_0$)	3
50R 50RA 50RB 50RC	50RA +50RB +50RC Phase-A RMS overcurrent elements Phase-B RMS overcurrent elements Phase-C RMS overcurrent elements	16 16 16 16
52A	Breaker status target LED. View this bit with the **TAR** command, but it cannot be used in logic.	0
52AA 52AB 52AC	Breaker status auxiliary input function for A-, B-, or C-phase	23 23 23
52ACV	52A Contradicts Voltage alarm	53
86BFT 86RS	Lockout relay Breaker Failure Trip and Reset logic outputs	71 71

Elements Alphabetically	Description	Relay Word Row
86BFT 86RS	There is also an 86BFT and 86RS Target LED that may be viewed with the **TAR** command, but they cannot be used in logic.	0 0
87F 87FOA 87FOB 87FOC	Maximum voltage across breaker after Flashover for A-, B-, or C-phase and a general element indicating any phase	7 3 4 4
87H 87HA 87HB 87HC	Voltage across breaker required to cause pole flashover for A-, B-, or C-phase and a general element for assertion of any phase	7 9 9 9
87TH 87THA 87THB 87THC	Voltage across the breaker required to enable the Thermal model for A-, B-, or C-phase and a general element for assertion of any phase	7 3 4 4
A	A-phase Target LED indicates an A-phase operation condition. View this bit with the **TAR** command, but it cannot be used in logic.	1
AF AFD	Load current logic timer 62AF Input (AF) and output (AFD)	33 33
AP APD	Load current logic timer 62AP input (AP) and output (APD)	33 33
B	B-phase target LED indicates a B-phase operation condition. View this bit with the **TAR** command, but it cannot be used in logic.	1
BALRM	Breaker Alarm condition, see BALRM setting	54
BCW	Breaker Wear Alarm	16
BDNC	Breaker Did Not Close alarm	53
BPF	Blown Potential Fuse alarm	53
C	C-phase target LED indicates a C-phase operation condition. View this bit with the **TAR** command, but it cannot be used in logic.	1
CAMT	Current After Motor operated disconnect Trip alarm	53
CCA CCB CCC	Controlled Close output for A-, B-, or C-phase	67 67 67
CCT CCTD	Point-on-wave automatic close input timer input and output	50 50

Elements Alphabetically	Description	Relay Word Row
CCMD	**CLOSE** Command	10
CLOSE	Close input function	22
CLOSE	There is also a CLOSE target LED that may be viewed with the **TAR** command, but it cannot be used in logic.	0
CRMEA CRMEB CRMEC	Thermal logic Close Resistor Model Enable for A-, B-, or C-phase	36 36 36
CTA CTB CTC	1/8-cycle Controlled close Timer output for A-, B-, or C-phase	72 72 72
CTAD CTBD CTCD	1/4-cycle Controlled close Timer output for A-, B-, or C-phase	52 52 52
CTF	Close resistor Thermal Failure logic output	66
CWO	Current While Open alarm	53
DP1-DP8 DP9-DP16	Display Point Elements	78 79
EN	Enable target LED indicates relay status. View this bit with the **TAR** command but it cannot be used in logic.	0
F1A F1AD F1B F1BD F1C F1CD F2A F2AD F2B F2BD F2C F2CD F3A F3AD F3B F3BD F3C F3CD	Flashover logic timer inputs and outputs for A-, B-, and C-phase	39 39 39 39 39 39 39 39 40 40 40 40 40 40 40 40 41 41
FAULT	Fault target LED indicates an operation under fault conditions. View this bit with the **TAR** command, but it cannot be used in logic.	1

Elements Alphabetically	Description	Relay Word Row
FBF	Fault current logic Breaker Failure output	68
FCA FCAD FCB FCBD FCC FCCD	Fault Current logic timer 62FC inputs and outputs for A-, B-, and C-phase	29 29 29 29 29 29
FCRS	Failed CB Close Resistors put in Service alarm	53
FFA FFAD FFB FFBD FFC FFCD	Flashover logic Failure timer inputs and outputs for A-, B-, and C-phase	44 44 44 44 44 44
FLASH	Flashover target LED indicates a flashover condition. View this bit with the **TAR** command, but it cannot be used in logic.	1
FOBF	Flashover logic Breaker Failure output	66
FPA FPAD FPB FPBD FPC FPCD	Flashover logic timer Pending failure inputs and outputs for A-, B-, and C-phase	43 43 43 43 44 44
FTRS	Failed CB Trip Resistors put in Service alarm	53
IN101-IN106	Input contacts (assert when control voltage is applied to input terminals)	17
IN201-IN208	Input contacts (assert when control voltage is applied to input terminals)	18
IN209-IN216	Input contacts (assert when control voltage is applied to input terminals)	19
IN301-IN308	Input contacts (assert when control voltage is applied to input terminals)	20
IN309-IN316	Input contacts (assert when control voltage is applied to input terminals)	21
KTRK	Voltage nulling Tracking bit (set if voltage nulling)	37

Elements Alphabetically	Description	Relay Word Row
L1AQ	General purpose SELOGIC Control Equation Set A Latch outputs, Reset inputs, and Set inputs	24
L1AR		24
L1AS		24
L1BQ		24
L1BR		24
L1BS		24
L1CQ		25
L1CR		24
L1CS		24
L1MQ	Trip and reset logic Latch outputs, Reset inputs, and Set inputs	69
L1MR		69
L1MS		69
L2MQ		70
L2MR		70
L2MS		70
L3MQ		70
L3MR		70
L3MS		70
L2AQ	General purpose SELOGIC Control Equation Set B Latch outputs, Reset inputs, and Set inputs	57
L2AR		57
L2AS		57
L2BQ		57
L2BR		57
L2BS		57
L2CQ		58
L2CR		57
L2CS		57
L3AQ		58
L3AR		58
L3AS		58
L3BQ		58
L3BR		58
L3BS		58
L3CQ		59
L3CR		59
L3CS		58
L4AQ		60
L4AR		60
L4AS		60
L4BQ		60
L4BR		60
L4BS		60
L4CQ		61
L4CR		60
L4CS		60

Elements Alphabetically	Description	Relay Word Row
L52Q	Load current logic Latch output, Reset input, and Set input	32
L52R		32
L52S		32
L5AQ	General purpose SELOGIC Control Equation Set B Latch outputs, Reset inputs, and Set inputs	61
L5AR		61
L5AS		61
L5BQ		61
L5BR		61
L5BS		61
L5CQ		62
L5CR		62
L5CS		61
L6AQ		63
L6AR		63
L6AS		63
L6BQ		63
L6BR		63
L6BS		63
L6CQ		64
L6CR		63
L6CS		63
L7AQ		64
L7AR		64
L7AS		64
L7BQ		64
L7BR		64
L7BS		64
L7CQ		65
L7CR		65
L7CS		64
LB1-LB8	Local Control Bits	14
LB9-LB16		15
LBF	Load and Line charging current logic Breaker Failure output	66
LDA	Load current logic timer 62LD inputs and outputs for A-, B-, and C-phase	31
LDAD		32
LDB		32
LDBD		32
LDC		32
LDCD		32

Elements Alphabetically	Description	Relay Word Row
LFAQ	Fault current logic Latch outputs, Reset inputs, and Set inputs for A-, B-, and C-phase	28
LFAR		27
LFAS		27
LFBQ		28
LFBR		28
LFBS		28
LFCQ		28
LFCR		28
LFCS		28
LHAQ	Flashover logic Latch outputs, Reset inputs, and Set inputs A-, B-, and C-phase	41
LHAR		41
LHAS		41
LHBQ		41
LHBR		41
LHBS		41
LHCQ		42
LHCR		42
LHCS		42
LLAQ	Load current logic Latch outputs, Reset inputs, and Set inputs for A-, B-, and C-phase	30
LLAR		30
LLAS		30
LLBQ		30
LLBR		30
LLBS		30
LLCQ		31
LLCR		30
LLCS		30
LOAD	Load target LED indicates an operation under load conditions. View this bit with the **TAR** command, but it cannot be used in logic.	1
LOD1	Loss-of-Dielectric level 1 and 2 input functions	23
LOD2		23
LODBF	Loss-of-Dielectric Breaker Failure output	67
LODCT	Loss-of-Dielectric, Current Transformer level input	23
LODPF	Loss-of-Dielectric Pending Failure output	67
LPA	Load current logic timer 62LP inputs and outputs for A-, B-, and C-phase	31
LPAD		31
LPB		31
LPBD		31
LPC		31
LPCD		31

Elements Alphabetically	Description	Relay Word Row
LPF	Load and Line charging current logic Pending Failure output	66
LRTAQ	Circuit breaker Retrip LRTA Latch outputs, Reset Inputs, and Set Inputs for A-, B-, and C-phase	55
LRTAR		55
LRTAS		55
LRTBQ		55
LRTBR		55
LRTBS		55
LRTCQ		56
LRTCR		55
LRTCS		55
LT1	Loss-of-dielectric Timers inputs and outputs	48
LT1D		48
LT2		48
LT2D		48
LT3		48
LT3D		48
LTAQ	Thermal logic Latch outputs, Reset inputs, and Set inputs for A-, B-, and C-phase	35
LTAR		34
LTAS		34
LTBQ		35
LTBR		35
LTBS		35
LTCQ		35
LTCR		35
LTCS		35
LUQ	Current Unbalance logic Latch output, Reset input, and Set input	45
LUR		45
LUS		45
LVAQ	Flashover logic Latch outputs, Reset inputs, and Set inputs for A-, B-, and C-phase	42
LVAR		42
LVAS		42
LVBQ		43
LVBR		42
LVBS		42
LVCQ		43
LVCR		43
LVCS		43

Elements Alphabetically	Description	Relay Word Row
M1 M1D M2 M2D M3 M3D M4 M4D	Trip and reset logic timers inputs and outputs	69 69 69 69 70 70 71 71
M86T	Lockout relay Trip conditions, See M86T setting	69
MCC	MOD Contradicts Current alarm	54
MCLOSE	Manual Close input function	22
MCT MCTD	Point-on-wave Manual Close input Timer input and output	49 50
MDT	Motor operated Disconnect Trip logic output	71
MER	Event trigger bit, see MER setting	71
MOD	Motor Operated Disconnect status target LED. View this bit with the **TAR** command, but it cannot be used in logic.	0
MODST	MOD Status input function	23
ONE	Always one	7
OPA OPAD OPB OPBD OPC OPCD	Thermal logic timer inputs and outputs for A-, B-, and C-phase	34 34 34 34 34 34
OUT101 - OUT107	Output contacts	73
OUT201 - OUT208	Output contacts	74
OUT209 - OUT216	Output contacts	75
OUT301 - OUT308	Output contacts	76
OUT309 - OUT316	Output contacts	77

Elements Alphabetically	Description	Relay Word Row
PCNA PCNB PCNC PCPA PCPB PCPC	Negative (N) and Positive (P) Peak Crossings for A-, B-, and C-phase voltage	51 51 51 50 51 51
PF	Pending Failure target LED. View this bit with the **TAR** command, but it cannot be used in logic.	0
PTD	Potential Transformers Disagree alarm	54
RB1-RB8 RB9-RB16	Remote Control Bits	12 13
RCA RCAD RCB RCBD RCC RCCD	Controlled close timers inputs and outputs for A-, B-, and C-phase	49 49 49 49 49 49
RCLS	Close dropout timer (CLSdo setting) reset equation	49
RT1 RT1D RT2 RT2D RT3 RT3D	Circuit breaker Retrip Timers inputs and outputs for A-, B-, and C-phase	56 56 56 56 56 56
RTA RTB RTC	Retrip logic output for A-, B-, and C-phase	67 67 67
SAA SAB SAC	General purpose SELOGIC Control Equation Set A outputs for A-, B-, and C-phase	26 26 26
SBA SBB SBC	General purpose SELOGIC Control Equation Set B outputs for A-, B-, and C-phase	65 65 65
SC	Slow Close alarm	54
SCT SCTD	Synchronizing output timer input and output	50 50
SS1 SS2	Group select input 1 and 2	22 22
ST	Slow Trip alarm	54

Elements Alphabetically	Description	Relay Word Row
SYNCEN	Synchronizing logic Enable equation	52
SYNCT SYNCTD	Synchronizing automatic close input Timer input and output	50 50
T1A T1AD T1B T1BD T1C T1CD	General purpose SELOGIC Control Equation Set A Timer 62T1 inputs and outputs	25 25 25 25 25 25
T2A T2AD T2B T2BD T2C T2CD T3A T3AD T3B T3BD T3C T3CD	General purpose SELOGIC Control Equation Set B Timers 62T3 and 62T4 inputs and outputs	59 59 59 59 59 59 62 62 62 62 62 62
TCMD	**OPEN** Command	10
THERM	Thermal target LED indicates a thermal condition. View this bit with the **TAR** command, but it cannot be used in logic.	1
TRIP	Trip target LED indicates a trip condition. View this bit with the **TAR** command, but it cannot be used in logic.	0
TRIP3 TRIPA TRIPB TRIPC	Trip input functions for three-pole trip and single-phase inputs (TRIP3 is independent of the other trips)	22 22 22 22
TRMEA TRMEB TRMEC	Thermal logic Trip Resistor Model Enable for A-, B-, and C-phase	36 36 36
TTA TTAD TTB TTBD TTC TTCD	Fault current logic Timer 62TT inputs and outputs for A-, B-, and C-phase	27 27 27 27 27 27
TTF	Trip resistor Thermal Failure logic output	66

Elements Alphabetically	Description	Relay Word Row
TWO	Trip While Open alarm	53
UBAL	Current Unbalance target LED. View this bit with the **TAR** command, but it cannot be used in logic.	1
UBBF UBPF	Current Unbalance logic Breaker Failure (BF) and Pending Failure (PF) Output	66 66
UC UCD	Current Unbalance logic control timer inputs and outputs	45 45
UFA UFAD UFB UFBD UFC UFCD	Current Unbalance logic Failure timer inputs and outputs for A-, B-, or C-phase	46 46 46 46 47 47
UPA UPAD UPB UPBD UPC UPCD	Current Unbalance logic Pending failure timer inputs and outputs for A-, B-, or C-phase	45 45 46 46 46 46
X27D3 X27DA X27DB X27DC	X Side undervoltage element A-, B-, or C-phase and a general element for assertion of all three phases	3 5 5 6
X47Q	X side, negative-sequence overvoltage element (operates on V_2)	9
X59H X59HA X59HB X59HC	X Side, High set overvoltage element for A-, B-, or C-phase and a general element for assertion of any phase	7 5 5 5
X59L3 X59LA X59LB X59LC	X Side overvoltage element for A-, B-, or C-phase and a general element for assertion of all three phases	2 5 5 5
XNTA XNTB XNTC XPTA XPTB XPTC	X side, Positive (P) and Negative (N) Trapped charge detection for A-, B-, or C-phase	10 10 10 10 10 10

Elements Alphabetically	Description	Relay Word Row
Y27D3 Y27DA Y27DB Y27DC	Y Side undervoltage element A-, B-, or C-phase and a general element for assertion of all three phases	3 6 6 6
Y47Q	Y side, negative-sequence overvoltage element (operates on V_2)	9
Y59L3 Y59LA Y59LB Y59LC	Y Side overvoltage element for A-, B-, or C-phase and a general element for assertion of all three phases	2 6 6 6
YNTA YNTB YNTC YPTA YPTB YPTC	Y side, Positive (P) and Negative (N) Trapped charge detection for A-, B-, or C-phase	11 11 11 11 11 11
ZCNA ZCNB ZCNC ZCPA ZCPB ZCPC	Positive (P) and Negative (N) Zero Crossings for A-, B-, or C-phase	51 52 52 51 51 52
ZERO	Always zero	6

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TABLES

APPENDIX G: DISTRIBUTED NETWORK PROTOCOL (DNP) 3.00

OVERVIEW

Some versions of the SEL-352 family of relays support Distributed Network Protocol (DNP) 3.00 Level 2 Slave protocol. This includes access to metering data, protection elements (Relay Word), contact I/O, targets, Sequential Events Recorder, breaker monitor, relay summary event reports, settings groups, and time synchronization. The SEL-352 Relay supports DNP point remapping, modem support, and virtual terminal object.

CONFIGURATION

To configure a port for DNP, set the port PROTO setting to DNP. Although DNP may be selected on any of the available ports, DNP may not be enabled on more than one port at a time. The following information is required to configure a port for DNP operation:

Label	Description	Default
SPEED	Serial port baud rate (300–38400)	2400
TIMEOUT	Serial port time-out (0–30 minutes)	5
DNPADR	DNP Address (0–65534)	0
MODEM	Modem connected to port (Y, N)	N
MSTR	Modem startup string (up to 30 characters)	E0X0&D0S0=2
PH_NUM	Phone number to dial-out to (up to 30 characters)	
MDTIME	Time to attempt dial (5–300 seconds)	60
MDRETI	Time between dial-out attempts (5–3600 seconds)	120
MDRETN	Number of dial-out attempts (0–5)	3
ECLASSA	Class for Analog event data (0 for no event, 1–3)	2
ECLASSB	Class for Binary event data (0 for no event, 1–3)	1
ECLASSC	Class for Counter event data (0 for no event, 1–3)	0
DECPLA	Currents scaling (0–3 decimal places)	1
DECPLV	Voltage scaling (0–3 decimal places)	1
DECPLM	Misc. scaling (0–3 decimal places)	1
TIMERQ	Time-set request interval (0–32767 min.)	0
STIMEO	Select/operate time-out (0.0–30.0 sec.)	1.0
DTIMEO	Data link time-out (0–5 sec.)	1
MINDLY	Minimum time from DCD to TX (0.00–1.00 sec.)	0.05
MAXDLY	Maximum time from DCD to TX (0.00–1.00 sec.)	0.10
PREDLY	Settle time from RTS on to TX (OFF, 0.00–30.00 sec.)	0
PSTDLY	Settle time after TX to RTS off (0.00–30.00 sec.)	0
ANADBA	Analog reporting dead band (0–32767 counts)	100
ANADBV	Analog reporting dead band (0–32767 counts)	100
ANADBM	Analog reporting dead band (0–32767 counts)	100
ETIMEO	Event data confirmation time-out (0.1–50.0 sec)	2.0
DRETRY	Data link retries (0–15)	3
UNSOL	Enable unsolicited reporting (Y, N)	N
PUNSOL	Enable unsolicited reporting at power-up (Y, N)	N
REPADR	DNP Address to report to (0–65534)	0
NUMEVE	Number of events to transmit on (1–200)	10
AGEEVE	Age of oldest event to transmit on (0–60 sec.)	2.0

The RTS signal may be used to control an external transceiver. The CTS signal is used as a DCD input, indicating when the medium is in use. Transmissions are only initiated if DCD is deasserted. When DCD drops, the next pending outgoing message may be sent once an idle time is satisfied. This idle time is randomly selected between the minimum and maximum allowed idle times (i.e., MAXDLY and MINDLY). In addition, the SEL-352 Relay monitors received data and treats receipt of data as a DCD indication. This allows RTS to be looped back to CTS in cases where the external transceiver does not support DCD. When the SEL-352 Relay transmits a DNP message, it delays transmitting after asserting RTS by at least the time in the PREDLY setting. After transmitting the last byte of the message, the SEL-352 Relay delays for at least PSTDLY milliseconds before deasserting RTS. If the PSTDLY time delay is in progress (RTS still high) following a transmission and another transmission is initiated, the SEL-352 Relay transmits the message without completing the PSTDLY delay and without any preceding PREDLY delay. The RTS/CTS handshaking may be completely disabled by setting PREDLY to OFF. In this case RTS is forced high and CTS is ignored, with only received characters acting as a DCD indication. The timing is the same as above, but PREDLY functions as if it were set to 0, and RTS is not actually deasserted after the PSTDLY time delay expires.

DATA-LINK OPERATION

It is necessary to make two important decisions about the data-link layer operation. One is how to handle data-link confirmation; the other is how to handle data-link access. If a highly reliable communications link exists, the data-link access can be disabled altogether, which significantly reduces communications overhead. Otherwise, it is necessary to enable confirmation and determine how many retries to allow and what the data-link time-out should be. The noisier the communications channel, the more likely a message will be corrupted. Thus, the number of retries should be set higher on noisy channels. Set the data-link time-out long enough to allow for the worst-case response of the master plus transmission time. When the SEL-352 Relay decides to transmit on the DNP link, it has to wait if the physical connection is in use. The SEL-352 Relay monitors physical connections by using CTS input (treated as a Data Carrier Detect) and monitoring character receipt. Once the physical link goes idle, as indicated by CTS being deasserted and no characters being received, the SEL-352 Relay will wait a configurable amount of time before beginning a transmission. This hold-off time will be a random value between the MINDLY and MAXDLY setting values. The hold-off time is random, which prevents multiple devices waiting to communicate on the network from continually colliding.

DATA ACCESS METHOD

Based on the capabilities of the system, it is necessary to choose a method for retrieving data on the DNP connection. The following table summarizes the main options, listed from least to most efficient, and indicates corresponding key related settings.

Table G.1: Data Access Methods

Data Retrieval Method	Description	Relevant SEL-352 Relay Settings
Polled Static	The master polls for static (Class 0) data only.	Set CLASS = 0, Set UNSOL = N.
Polled Report-by-Exception	The master polls frequently for event data and occasionally for static data.	Set CLASS to a non-zero value, Set UNSOL = N.
Unsolicited Report-by-Exception	The slave devices send unsolicited event data to the master and the master occasionally sends integrity polls for static data.	Set CLASS to a non-zero value, Set UNSOL = Y, Set NUMEVE and AGEEVE according to how often messages are desired to be sent.
Quiescent	The master never polls and relies on unsolicited reports only.	Set CLASS to a non-zero value, Set UNSOL = Y, Set NUMEVE and AGEEVE according to how often messages are desired to be sent.

DEVICE PROFILE

The following is the device profile as specified in the ***DNP 3.00 Subset Definitions*** document:

DNP 3.00
DEVICE PROFILE DOCUMENT
This document must be accompanied by a table having the following headings:

Object Group	Request Function Codes	Response Function Codes
Object Variation	Request Qualifiers	Response Qualifiers
Object Name (optional)		

Vendor Name: **Schweitzer Engineering Laboratories, Inc.**

Device Name: **SEL-352**

Highest DNP Level Supported:	Device Function:
For Requests **Level 2** For Responses **Level 2**	❒ Master ☑ Slave

Notable objects, functions, and/or qualifiers supported in addition to the Highest DNP Levels Supported (the complete list is described in the attached table):

Supports enabling and disabling of unsolicited reports on a class basis.

Supports Virtual Terminal.

Maximum Data Link Frame Size (octets):	Maximum Application Fragment Size (octets):
Transmitted 292	2048 (if >2048, must be configurable)
Received (must be 292)	2048 (must be >249)

Maximum Data Link Re-tries:	Maximum Application Layer Re-tries:
❒ None ❒ Fixed at _____ ☑ Configurable, range 0 to 15	☑ None ❒ Configurable, range ___ to (Fixed is not permitted)

Requires Data Link Layer Confirmation:

❒ Never
❒ Always
❒ Sometimes If 'Sometimes', when? _____
☑ Configurable If 'Configurable', how? by settings.

Requires Application Layer Confirmation:

❒ Never
❒ Always (not recommended)
☑ When reporting Event Data (Slave devices only)
❒ When sending multi-fragment responses (Slave devices only)
❒ Sometimes If 'Sometimes', when? _____
❒ Configurable If 'Configurable', how? _____

Time-outs while waiting for:

Data Link Confirm	❒ None	❒ Fixed at _____	❒ Variable	☑ Configurable
Complete Appl. Fragment	☑ None	❒ Fixed at _____	❒ Variable	❒ Configurable
Application Confirm	❒ None	❒ Fixed at _____	❒ Variable	☑ Configurable
Complete Appl. Response	☑ None	❒ Fixed at _____	❒ Variable	❒ Configurable

Others _____

Attach explanation if 'Variable' or 'Configurable' was checked for any time-out.

Sends/Executes Control Operations:

WRITE Binary Outputs	❒ Never	☑ Always	❒ Sometimes	❒ Configurable
SELECT/OPERATE	❒ Never	☑ Always	❒ Sometimes	❒ Configurable
DIRECT OPERATE	❒ Never	☑ Always	❒ Sometimes	❒ Configurable
DIRECT OPERATE - NO ACK	❒ Never	☑ Always	❒ Sometimes	❒ Configurable
Count > 1	☑ Never	❒ Always	❒ Sometimes	❒ Configurable
Pulse On	❒ Never	☑ Always	❒ Sometimes	❒ Configurable
Pulse Off	❒ Never	☑ Always	❒ Sometimes	❒ Configurable
Latch On	❒ Never	☑ Always	❒ Sometimes	❒ Configurable
Latch Off	❒ Never	☑ Always	❒ Sometimes	❒ Configurable
Queue	☑ Never	❒ Always	❒ Sometimes	❒ Configurable
Clear Queue	☑ Never	❒ Always	❒ Sometimes	❒ Configurable

Attach explanation if 'Sometimes' or 'Configurable' was checked for any operation.

FILL OUT THE FOLLOWING ITEM FOR MASTER DEVICES ONLY:	
Expects Binary Input Change Events: ❒ Either time-tagged or non-time-tagged for a single event ❒ Both time-tagged and non-time-tagged for a single event ❒ Configurable (attach explanation)	
FILL OUT THE FOLLOWING ITEMS FOR SLAVE DEVICES ONLY	
Reports Binary Input Change Events when no specific variation requested: ❒ Never ❒ Only time-tagged ☑ Only non-time-tagged ❒ Configurable to send both, one or the other (attach explanation)	Reports time-tagged Binary Input Change Events when no specific variation requested: ☑ Never ❒ Binary Input Change With Time ❒ Binary Input Change With Relative Time ❒ Configurable (attach explanation)
Sends Unsolicited Responses: ❒ Never ☑ Configurable (attach explanation) ❒ Only certain objects ❒ Sometimes (attach explanation) ☑ ENABLE/DISABLE UNSOLICITED Function codes supported	Sends Static Data in Unsolicited Responses: ☑ Never ❒ When Device Restarts ❒ When Status Flags Change No other options are permitted.
Default Counter Object/Variation: ❒ No Counters Reported ❒ Configurable (attach explanation) ☑ Default object 20 ❒ Default variation 6 ❒ Point-by-point list attached	Counters Roll Over at: ❒ No Counters Reported ❒ Configurable (attach explanation) ☑ 16 Bits ❒ 32 Bits ❒ Other Value _____ ❒ Point-by-point list attached
Sends Multi-Fragment Responses: ☑Yes ❒No	

In all cases of a configurable item within the device profile, the item is controlled by SEL-352 Relay settings.

OBJECT TABLE

The following object table lists supported objects, functions, and qualifier code combinations.

Table G.2: SEL-352 Relay DNP Object Table

Object			Request (supported)		Response (may generate)	
Obj.	*default Var.	Description	Function Codes (decimal)	Qualifier Codes (hex)	Function Codes (decimal)	Qualifier Codes (hex)
1	0	Binary Input–All Variations	1	0,1,6,7,8		
1	1	Binary Input	1	0,1,6,7,8	129	0,1,7,8
1	2*	Binary Input With Status	1	0,1,6,7,8	129	0,1,7,8
2	0	Binary Input Change–All Variations	1	6,7,8		
2	1	Binary Input Change Without Time	1	6,7,8	129	17,28
2	2*	Binary Input Change With Time	1	6,7,8	129,130	17,28
2	3	Binary Input Change With Relative Time	1	6,7,8	129	17,28
10	0	Binary Output–All Variations	1	0,1,6,7,8		
10	1	Binary Output				
10	2*	Binary Output Status	1	0,1,6,7,8	129	0,1
12	0	Control Block–All Variations				
12	1	Control Relay Output Block	3,4,5,6	17,28	129	echo of request
12	2	Pattern Control Block				
12	3	Pattern Mask				
20	0	Binary Counter–All Variations	1	0,1,6,7,8		
20	1	32-Bit Binary Counter				
20	2	16-Bit Binary Counter				
20	3	32-Bit Delta Counter				
20	4	16-Bit Delta Counter				
20	5	32-Bit Binary Counter Without Flag	1	0,1,6,7,8	129	0,1,7,8
20	6*	16-Bit Binary Counter Without Flag	1	0,1,6,7,8	129	0,1,7,8
20	7	32-Bit Delta Counter Without Flag				
20	8	16-Bit Delta Counter Without Flag				
21	0	Frozen Counter–All Variations				
21	1	32-Bit Frozen Counter				
21	2	16-Bit Frozen Counter				
21	3	32-Bit Frozen Delta Counter				
21	4	16-Bit Frozen Delta Counter				
21	5	32-Bit Frozen Counter With Time of Freeze				
21	6	16-Bit Frozen Counter With Time of Freeze				
21	7	32-Bit Frozen Delta Counter With Time of Freeze				
21	8	16-Bit Frozen Delta Counter With Time of Freeze				
21	9	32-Bit Frozen Counter Without Flag				
21	10	16-Bit Frozen Counter Without Flag				
21	11	32-Bit Frozen Delta Counter Without Flag				
21	12	16-Bit Frozen Delta Counter Without Flag				
22	0	Counter Change Event–All Variations	1	6,7,8		
22	1	32-Bit Counter Change Event Without Time	1	6,7,8	129	17,28

Object			Request (supported)		Response (may generate)	
Obj.	*default Var.	Description	Function Codes (decimal)	Qualifier Codes (hex)	Function Codes (decimal)	Qualifier Codes (hex)
22	2*	16-Bit Counter Change Event Without Time	1	6,7,8	129,130	17,28
22	3	32-Bit Delta Counter Change Event Without Time				
22	4	16-Bit Delta Counter Change Event Without Time				
22	5	32-Bit Counter Change Event With Time	1	6,7,8	129	17,28
22	6	16-Bit Counter Change Event With Time	1	6,7,8	129	17,28
22	7	32-Bit Delta Counter Change Event With Time				
22	8	16-Bit Delta Counter Change Event With Time				
23	0	Frozen Counter Event–All Variations				
23	1	32-Bit Frozen Counter Event Without Time				
23	2	16-Bit Frozen Counter Event Without Time				
23	3	32-Bit Frozen Delta Counter Event Without Time				
23	4	16-Bit Frozen Delta Counter Event Without Time				
23	5	32-Bit Frozen Counter Event With Time				
23	6	16-Bit Frozen Counter Event With Time				
23	7	32-Bit Frozen Delta Counter Event With Time				
23	8	16-Bit Frozen Delta Counter Event With Time				
30	0	Analog Input–All Variations	1	0,1,6,7,8		
30	1	32-Bit Analog Input	1	0,1,6,7,8	129	0,1,7,8
30	2	16-Bit Analog Input	1	0,1,6,7,8	129	0,1,7,8
30	3	32-Bit Analog Input Without Flag	1	0,1,6,7,8	129	0,1,7,8
30	4*	16-Bit Analog Input Without Flag	1	0,1,6,7,8	129	0,1,7,8
31	0	Frozen Analog Input–All Variations				
31	1	32-Bit Frozen Analog Input				
31	2	16-Bit Frozen Analog Input				
31	3	32-Bit Frozen Analog Input With Time of Freeze				
31	4	16-Bit Frozen Analog Input With Time of Freeze				
31	5	32-Bit Frozen Analog Input Without Flag				
31	6	16-Bit Frozen Analog Input Without Flag				
32	0	Analog Change Event–All Variations	1	6,7,8		
32	1	32-Bit Analog Change Event Without Time	1	6,7,8	129	17,28
32	2*	16-Bit Analog Change Event Without Time	1	6,7,8	129,130	17,28
32	3	32-Bit Analog Change Event With Time	1	6,7,8	129	17,28
32	4	16-Bit Analog Change Event With Time	1	6,7,8	129	17,28
33	0	Frozen Analog Event–All Variations				
33	1	32-Bit Frozen Analog Event Without Time				
33	2	16-Bit Frozen Analog Event Without Time				
33	3	32-Bit Frozen Analog Event With Time				
33	4	16-Bit Frozen Analog Event With Time				
40	0	Analog Output Status–All Variations	1	0,1,6,7,8		
40	1	32-Bit Analog Output Status	1	0,1,6,7,8	129	0,1,7,8
40	2*	16-Bit Analog Output Status	1	0,1,6,7,8	129	0,1,7,8
41	0	Analog Output Block–All Variations				
41	1	32-Bit Analog Output Block	3,4,5,6	17,28	129	echo of request

Object			Request (supported)		Response (may generate)	
Obj.	*default Var.	Description	Function Codes (decimal)	Qualifier Codes (hex)	Function Codes (decimal)	Qualifier Codes (hex)
41	2	16-Bit Analog Output Block	3,4,5,6	17,28	129	echo of request
50	0	Time and Date–All Variations				
50	1	Time and Date	1,2	7,8 index = 0	129	07, quantity=1
50	2	Time and Date With Interval				
51	0	Time and Date CTO–All Variations				
51	1	Time and Date CTO				
51	2	Unsynchronized Time and Date CTO				07, quantity=1
52	0	Time Delay–All Variations				
52	1	Time Delay Coarse				
52	2	Time Delay Fine			129	07, quantity=1
60	0	All Classes of Data	1,20,21	6		
60	1	Class 0 Data	1	6		
60	2	Class 1 Data	1,20,21	6,7,8		
60	3	Class 2 Data	1,20,21	6,7,8		
60	4	Class 3 Data	1,20,21	6,7,8		
70	1	File Identifier				
80	1	Internal Indications	2	0,1 index = 7		
81	1	Storage Object				
82	1	Device Profile				
83	1	Private Registration Object				
83	2	Private Registration Object Descriptor				
90	1	Application Identifier				
100	1	Short Floating Point				
100	2	Long Floating Point				
100	3	Extended Floating Point				
101	1	Small Packed Binary-Coded Decimal				
101	2	Medium Packed Binary-Coded Decimal				
101	3	Large Packed Binary-Coded Decimal				
112	All	Virtual Terminal Output Block	2	6		
113	All	Virtual Terminal Event Data	1,20,21	6	129,130	17,28
No object			13,14,23			

DATA MAP

The following is the default object map supported by the SEL-352-2 Relay (see ***Appendix A***: ***Firmware Versions in This Manual***).

Table G.3: SEL-352 Relay DNP Data Map

DNP Object Type	Index	Description
01,02	000–799	Relay Word, where 50FTA is 0 and LHBQ is 319.
01,02	800–1599	Relay Word from the SER, encoded same as inputs 000–799 with 800 added.
01,02	1600–1615	Relay front-panel targets, where 1615 is FAULT, 1608 is C, 1607 is EN, and 1600 is MOD.
01,02	1616	Relay disabled.
01,02	1617	Relay diagnostic failure.
01,02	1618	Relay diagnostic warning.
01,02	1619	New relay event available.
10,12	00–15	Remote bits RB1–RB16.
10,12	16	Pulse Open breaker command TCMD.
10,12	17	Pulse Close breaker command CCMD.
10,12	18–23	Reserved.
10,12	24-31	Remote bit pairs RB1–RB16.
10,12	32	Open/Close pair for breaker.
10,12	33–38	Reserved.
10,12	39	Clear breaker monitor.
10,12	40	Reset front-panel targets.
10,12	41	Read next relay event.
20,22	00	Active settings group.
20,22	01	Breaker Trip A.
20,22	02	Breaker Trip B.
20,22	03	Breaker Trip C.
20,22	04	Breaker Close A.
20,22	05	Breaker Close B.
20,22	06	Breaker Close C.
20,22	07	Failed CB Trip Resistors Put in Service.
20,22	08	Failed CB Close Resistors Put in Service.
20,22	09	52A contradicts voltage.
20,22	10	Current while open.
20,22	11	Trip while open.
20,22	12	CB did not close.
20,22	13	Current after MOD trip.

DNP Object Type	Index	Description
20,22	14	MOD contradicts current.
20,22	15	Slow trip.
20,22	16	Slow close.
20,22	17	Potential transformers disagree.
30,32	00	IA magnitude.
30,32	01	IB magnitude.
30,32	02	IC magnitude.
30,32	03	IAB magnitude.
30,32	04	IBC magnitude.
30,32	05	ICA magnitude.
30,32	06	VXA magnitude.
30,32	07	VXB magnitude.
30,32	08	VXC magnitude.
30,32	09	VXAB magnitude.
30,32	10	VXBC magnitude.
30,32	11	VXCA magnitude.
30,32	12	VYA magnitude.
30,32	13	VYB magnitude.
30,32	14	VYC magnitude.
30,32	15	VYAB magnitude.
30,32	16	VYBC magnitude.
30,32	17	VYCA magnitude.
30,32	18	DVA magnitude.
30,32	19	DVB magnitude.
30,32	20	DVC magnitude.
30,32	21	MW
30,32	22	MVAR
30,32	23–28	Avg. Electrical Time (ms) TRIPA, B, C & CLOSEA, B, C.
30,32	29–34	Avg. Mechanical Time (ms) TRIPA, B, C & CLOSEA, B, C.
30,32	35–40	Last Electrical Time (ms.) TRIPA, B, C & CLOSEA, B, C.
30,32	41–46	Last Mechanical Time (ms) TRIPA, B, C & CLOSEA, B, C.
30,32	47–52	Total Energy (MJ) TRIPA, B, C & CLOSEA, B, C.
30,32	53–58	Total Current (A) TRIPA, B, C & CLOSEA, B, C.
30,32	59–61	Breaker Wear % TRIPA, B, C.

DNP Object Type	Index	Description
30, 32	62–67	Resistor heat Open & Close A, B, C.
30	68	Event Type (see Event Cause table, next page).
30	69	Fault frequency.
30	70–75	Voltage Nulling Factor (All Phases, Mag. & Angle).
30	76	Fault settings group.
30	77–79	Fault time in DNP format (high, middle, and low 16 bits).
40,41	00	Active settings group.

Binary inputs (objects 1 and 2) are supported as defined by the previous table. Binary inputs 0–799 and 1600–1619 are scanned approximately once every 128 ms to generate events. When time is reported with these event objects, it is the time at which the scanner observed the bit change. This may be significantly delayed from when the original source changed and should not be used for sequence-of-events determination. In order to determine an element's point index, see the ***Binary Input Lookup Table***. It is derived from the Relay Word Bits tables in ***Appendix F: Relay Word***. Locate the element in question in the table and note the Relay Word row number. From that row number, subtract the row number of the first Relay Word row (usually 2) and multiply that result by 8. This is the index of the right-most element of the Relay Word row of the element in question. Count over to the original element and add that to get the point index. Binary Inputs 800–1599 are derived from the Sequential Events Recorder (SER) and carry the time stamp of actual occurrence. Add 800 to the Binary Input Point column to get the point mapping for points 800–1599. Static reads from these inputs will show the same data as a read from the corresponding index in the 0–799 group. Only points that are actually in the SER list (SET R) will generate events in the 800–1599 group.

Analog Inputs (objects 30 and 32) are supported as defined by the preceding table. The values are reported in primary units. Current magnitudes are scaled according to the DECPLA setting. If DECPLA is 3, then its value is multiplied by 1000. Similarly voltage magnitudes and VDC are scaled according to the DECPLV setting. All other quantities are scaled by the DECPLM setting. Event-class messages are generated whenever an input changes beyond the value given by the ANADBA, ANADBV, or ANADBM settings. The dead-band check is done after any scaling is applied. Analog inputs are scanned at approximately a ½-second rate, except for analogs 68–79. During a scan, all events generated will use the time the scan was initiated. Analogs 68–79 are derived from the history queue data for the most recently read fault and do not generate event messages. Analog 68 is defined as follows:

Value	Event Cause
1	CLOSE
2	PHASE1
3	TRIPC
4	TRIPB
5	TRIPA
6	PHASE2
7	TRIPBC
8	TRIPCA
9	TRIPAB
12	TRIP3ϕ
13	BFT

If Analog 68 is 0, no more new events are available (i.e., all events have been read).

Control Relay Output Blocks (object 12, variation 1) are supported. The control relays correspond to the remote bits and other functions, as shown above. The Trip/Close bits take precedence over the control field. If either the Trip or Close bit is set, one of the other control field bits must be set as well. The control field is interpreted as follows:

Index	Close (0x4X)	Trip (0x8X)	Latch On (3)	Latch Off (4)	Pulse On (1)	Pulse Off (2)
0–15	Set	Clear	Set	Clear	Pulse	Clear
16–17	Pulse	Do nothing	Pulse	Do nothing	Pulse	Do nothing
24	Pulse RB2	Pulse RB1	Pulse RB2	Pulse RB1	Pulse RB2	Pulse RB1
25	Pulse RB4	Pulse RB3	Pulse RB4	Pulse RB3	Pulse RB4	Pulse RB3
26	Pulse RB6	Pulse RB5	Pulse RB6	Pulse RB5	Pulse RB6	Pulse RB5
27	Pulse RB8	Pulse RB7	Pulse RB8	Pulse RB7	Pulse RB8	Pulse RB7
28	Pulse RB10	Pulse RB9	Pulse RB10	Pulse RB9	Pulse RB10	Pulse RB9
29	Pulse RB12	Pulse RB11	Pulse RB12	Pulse RB11	Pulse RB12	Pulse RB11
30	Pulse RB14	Pulse RB13	Pulse RB14	Pulse RB13	Pulse RB14	Pulse RB13
31	Pulse RB16	Pulse RB15	Pulse RB16	Pulse RB15	Pulse RB16	Pulse RB15
32	Pulse CCMD	Pulse TCMD	Pulse CCMD	Pulse TCMD	Pulse CCMD	Pulse TCMD
39-41	Pulse	Do Nothing	Pulse	Do Nothing	Pulse	Do Nothing

If the Trip bit is set, a Latch Off operation is performed, and if the Close bit is set, a Latch On operation is performed on the specified index. The Status field is used exactly as defined. All other fields are ignored. A pulse operation asserts a point for a single processing interval. Caution should be exercised with multiple remote bit pulses in a single message (i.e., point count > 1), as this may result in some of the pulse commands being ignored and returning an already active status.

Analog Outputs (objects 40 and 41) are supported as defined by the preceding table. Flags returned with object 40 responses are always set to 0. The Control Status field of object 41 requests is ignored. If the value written to index 0 is outside of the range 1 through 6, the relay will not accept the value and will return a hardware error status.

Table G.4: SEL-352-2 Relay Binary Input Lookup Table

Row	SEL-352 Relay Word Bits								Binary Input Point
	General Elements								
2	Y59L3	X59L3	50LDC	50LDB	50LDA	50FTC	50FTB	50FTA	7–0
3	87THA	87FOA	Y27D3	X27D3	50N	50MDC	50MDB	50MDA	15–8
4	47Q	37OP	25T	46P	87THC	87FOC	87THB	87FOB	23–16
5	X59LC	X59HC	X27DB	X59LB	X59HB	X27DA	X59LA	X59HA	31–24
6	ZERO	Y27DC	Y59LC	Y27DB	Y59LB	Y27DA	Y59LA	X27DC	39–32
7	ONE	50MNC	50MNB	50MNA	87F	87H	87TH	X59H	47–40
8	25M	25C	46C	46B	46A	50MD	50LD	50FT	55–48
9	Y47Q	X47Q	37OPC	37OPB	37OPA	87HC	87HB	87HA	63–56
10	CCMD	TCMD	XNTC	XPTC	XNTB	XPTB	XNTA	XPTA	71–64
11	*	*	YNTC	YPTC	YNTB	YPTB	YNTA	YPTA	79–72
12	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	87–80
13	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	95–88
14	LB8	LB7	LB6	LB5	LB4	LB3	LB2	LB1	103–96
15	LB16	LB15	LB14	LB13	LB12	LB11	LB10	LB9	111–104
16	*	*	*	BCW	50R	50RC	50RB	50RA	119–112
17	*	*	IN106	IN105	IN104	IN103	IN102	IN101	127–120
18	IN208	IN207	IN206	IN205	IN204	IN203	IN202	IN201	135–128
19	IN216	IN215	IN214	IN213	IN212	IN211	IN210	IN209	143–136
20	IN308	IN307	IN306	IN305	IN304	IN303	IN302	IN301	151–144
21	IN316	IN315	IN314	IN313	IN312	IN311	IN310	IN309	159–152
22	MCLOSE	CLOSE	TRIP3	TRIPC	TRIPB	TRIPA	SS2	SS1	167–160
23	*	LODCT	LOD2	LOD1	MODST	52AC	52AB	52AA	175–168
	SELOGIC® Control Equation SET A Elements								
24	L1CR	L1CS	L1BQ	L1BR	L1BS	L1AQ	L1AR	L1AS	183–176
25	*	T1CD	T1C	T1BD	T1B	T1AD	T1A	L1CQ	191–184
26	*	*	*	*	*	SAC	SAB	SAA	199–192
	Fault Current Protection Elements								
27	LFAR	LFAS	TTCD	TTC	TTBD	TTB	TTAD	TTA	207–200
28	*	LFCQ	LFCR	LFCS	LFBQ	LFBR	LFBS	LFAQ	215–208
29	*	*	FCCD	FCC	FCBD	FCB	FCAD	FCA	223–216

Row	SEL-352 Relay Word Bits								Binary Input Point
	Load Current Protection Elements								
30	LLCR	LLCS	LLBQ	LLBR	LLBS	LLAQ	LLAR	LLAS	231–224
31	LDA	LPCD	LPC	LPBD	LPB	LPAD	LPA	LLCQ	239–232
32	L52Q	L52R	L52S	LDCD	LDC	LDBD	LDB	LDAD	247–240
33	*	*	*	*	AFD	AF	APD	AP	255–248
	Resistor Thermal Protection Elements								
34	LTAR	LTAS	OPCD	OPC	OPBD	OPB	OPAD	OPA	263–256
35	*	LTCQ	LTCR	LTCS	LTBQ	LTBR	LTBS	LTAQ	271–264
36	*	*	CRMEC	CRMEB	CRMEA	TRMEC	TRMEB	TRMEA	279–272
37	*	KTRK	26TFC	26TFB	26TFA	26CFC	26CFB	26CFA	287–280
38	*	*	26TPC	26TPB	26TPA	26CPC	26CPB	26CPA	295–288
	Flashover Protection Elements								
39	F2AD	F2A	F1CD	F1C	F1BD	F1B	F1AD	F1A	303–296
40	F3BD	F3B	F3AD	F3A	F2CD	F2C	F2BD	F2B	311–304
41	LHBQ	LHBR	LHBS	LHAQ	LHAR	LHAS	F3CD	F3C	319–312
42	LVBR	LVBS	LVAQ	LVAR	LVAS	LHCQ	LHCR	LHCS	327–320
43	FPBD	FPB	FPAD	FPA	LVCQ	LVCR	LVCS	LVBQ	335–328
44	FFCD	FFC	FFBD	FFB	FFAD	FFA	FPCD	FPC	343–336
	Unbalance Protection Elements								
45	*	UPAD	UPA	LUQ	LUR	LUS	UCD	UC	351–344
46	UFBD	UFB	UFAD	UFA	UPCD	UPC	UPBD	UPB	359–352
47	*	*	*	*	*	*	UFCD	UFC	367–360
	Loss-of-Dielectric Protection Elements								
48	*	*	LT3D	LT3	LT2D	LT2	LT1D	LT1	375–368
	Controlled Close Elements								
49	MCT	RCCD	RCC	RCBD	RCB	RCAD	RCA	RCLS	383–376
50	PCPA	SCTD	SCT	SYNCTD	SYNCT	CCTD	CCT	MCTD	391–384
51	ZCPB	ZCNA	ZCPA	PCNC	PCPC	PCNB	PCPB	PCNA	399–392
52	*	SYNCEN	CTCD	CTBD	CTAD	ZCNC	ZCPC	ZCNB	407–400
	Breaker Alarm Elements								
53	CAMT	BPF	BDNC	TWO	CWO	52ACV	FCRS	FTRS	415–408
54	*	*	*	BALRM	PTD	SC	ST	MCC	423–416
	Circuit Breaker Retrip Elements								
55	LRTCR	LRTCS	LRTBQ	LRTBR	LRTBS	LRTAQ	LRTAR	LRTAS	431–424
56	*	RT3D	RT3	RT2D	RT2	RT1D	RT1	LRTCQ	439–432

Row	SEL-352 Relay Word Bits								Binary Input Point
	SELOGIC Control Equation SET B Elements								
57	L2CR	L2CS	L2BQ	L2BR	L2BS	L2AQ	L2AR	L2AS	447–440
58	L3CS	L3BQ	L3BR	L3BS	L3AQ	L3AR	L3AS	L2CQ	455–448
59	T2CD	T2C	T2BD	T2B	T2AD	T2A	L3CQ	L3CR	463–456
60	L4CR	L4CS	L4BQ	L4BR	L4BS	L4AQ	L4AR	L4AS	471–464
61	L5CS	L5BQ	L5BR	L5BS	L5AQ	L5AR	L5AS	L4CQ	479–472
62	T3CD	T3C	T3BD	T3B	T3AD	T3A	L5CQ	L5CR	487–480
63	L6CR	L6CS	L6BQ	L6BR	L6BS	L6AQ	L6AR	L6AS	495–488
64	L7CS	L7BQ	L7BR	L7BS	L7AQ	L7AR	L7AS	L6CQ	503–496
65	*	*	*	SBC	SBB	SBA	L7CQ	L7CR	511–504
	Logic Output Elements								
66	UBBF	UBPF	FOBF	FOPF	CTF	TTF	LBF	LPF	519–512
67	RTC	RTB	RTA	CCC	CCB	CCA	LODBF	LODPF	527–520
68	*	*	*	*	*	*	*	FBF	535–528
	86BF Trip and Reset Elements								
69	M2D	M2	L1MQ	L1MR	L1MS	M1D	M1	M86T	543–536
70	L3MQ	L3MR	L3MS	M3D	M3	L2MQ	L2MR	L2MS	551–544
71	*	MER	86BFT	86RS	MDT	M4D	M4	*	559–552
72	*	*	*	*	*	CTC	CTB	CTA	567–560
	Contact Output Elements and Display Points								
73	!ALARM	OUT107	OUT106	OUT105	OUT104	OUT103	OUT102	OUT101	575–568
74	OUT201	OUT202	OUT203	OUT204	OUT205	OUT206	OUT207	OUT208	583–576
75	OUT209	OUT210	OUT211	OUT212	OUT213	OUT214	OUT215	OUT216	591–584
76	OUT301	OUT302	OUT303	OUT304	OUT305	OUT306	OUT307	OUT308	599–592
77	OUT309	OUT310	OUT311	OUT312	OUT313	OUT314	OUT315	OUT316	607–600
78	DP8	DP7	DP6	DP5	DP4	DP3	DP2	DP1	615–608
79	DP16	DP15	DP14	DP13	DP12	DP11	DP10	DP9	623–616

*Reserved for future use.

Relay Summary Event Data

Whenever there is unread relay event summary data (fault data), binary input point 1619 will be set. In order to load the next available relay event summary, the master should pulse binary output point 41. This will cause the event summary analogs (points 68–79) to be loaded with information from the next oldest relay event summary. Since the summary data is stored in a first-in, first-out manner, loading the next event will cause the data from the previous load to be discarded. The event summary analogs will retain this information until the next event is loaded. If no further event summaries are available, attempting to load the next event will cause the event type analog (point 68) to be set to 0.

POINT REMAPPING

Introduction

The **DNP** command is available to view and remap the DNP data. This command is available at level 1 for viewing data, but only from level 2 can it be used to remap the DNP map.

Inputs

Command Syntax: DNP [A|B|S|T]

DNP [AI|AO|BI|BO|C] [VIEW]

The DNP analog input, analog output, counter, binary output, and binary input points may be remapped via the **DNP** command. The map is composed of five lists of indices: one for the analog inputs (30 and 32), one for the binary inputs (1 and 2), one for the binary outputs (10 and 12), one for the analog outputs (40 and 41), and the other for the counters (20 and 22). The indices correspond to those given by the relay's DNP data map. The order in which they occur in the list determines the index that the corresponding value is reported to the DNP master. If a value is not in the list, it is not available to the DNP master. All points of the corresponding type may be included in the list, but must only occur once. The maps are stored in nonvolatile memory and are protected with a checksum. The **DNP** command is only available if DNP has been selected on one of the ports.

If the **DNP** command is issued without parameters, the relay displays all of the maps with the following format:

```
=>DNP<ENTER>

Binary Inputs = Default Map
Binary Outputs = Default Map
Counters    = Default Map
Analog Inputs = 112 28 17 35 1 56 57 58 59 60 61 62 63 64 65 \
         66 67 100 101 102 103
Analog Outputs = Off
=>
```

If the **DNP** command is issued with an object type specified (AI, AO, BI, BO, C) and the VIEW parameter, the relay displays only the corresponding map. The S parameter is equivalent to AI VIEW and the T parameter is equivalent to BI VIEW; they are available for consistency with the older products. If the map checksum is determined to be invalid, the map will be reported as corrupted during a display command, as follows:

```
=>DNP BI VIEW<ENTER>

Binary Inputs = Map Corrupted

=>
```

If the **DNP** command is issued with just an object type specifier (AI, AO, BI, BO, C) at level 2 or greater, the relay asks the user to enter indices for the corresponding list. (The A parameter is the same as AI and B is the same as BI; these parameters are available for consistency with older products.) The relay accepts lines of indices until a line without a final continuation character (\) is entered. Each line of input is constrained to 80 characters, but all the points may be remapped,

using multiple lines with continuation characters (\) at the end of the intermediate lines. If a single blank line is entered as the first line, the re-mapping is disabled for that type (i.e., the relay uses the default map). If a single entry of OFF or NA is entered, all objects of that type will be disabled. For example, the first example re-map could be produced with the following commands:

```
==>DNP AI<ENTER>

Enter the new DNP Analog Input map
112 28 17 \<ENTER>
35 1 56 57 58 59 60 61 62 63 64 65 66 67 100 101 102 \<ENTER>
103<ENTER>

Save Settings (Y/N)? Y<ENTER>

==>DNP BI<ENTER>

Enter the new DNP Binary Input map
<ENTER>

Save Settings (Y/N)? Y<ENTER>
==>DNP AO<ENTER>

Enter the new DNP Analog Output map
OFF<ENTER>

Save Settings (Y/N)? Y<ENTER>

==>
```

The **DNP** command will report an error if an index is used twice, an invalid index is used, or nonnumeric data is entered:

```
xx is referenced more than once, changes not saved

xx is not a valid index, changes not saved

Invalid format, changes not saved
```

In addition to re-mapping, these commands can be used on analog inputs to create custom scaling and dead bands per point. Scaling is done by adding a semicolon and scaling factor to a point reference. The base value will be multiplied by the scaling factor before reporting it. This is done instead of the DECPLA setting that would normally apply. Dead bands are added using a colon and dead-band count. This dead band will override the ANADBA setting. For example:

```
==>DNP AI<ENTER>

Enter the new DNP Analog Input map
112;5 28;0.2 17:10 1;1:15<ENTER>

==>
```

These settings will cause the value at index 112 (now at index 0) to be multiplied by five before it is reported. Similarly, the value at index 28 (now at index 1) will be multiplied by 0.2 before it is reported. Both of these values will use the default dead band. The value at index 17 (now at index 2) is left for default scaling, but uses a dead band of ±10 counts. Similarly, the value that was at index 1 (now at index 3) is now scaled by 1 and uses a dead band of ±15 counts.

Modem Support

The modem handling will only be applied when the port settings include the following:

PROTOCOL = DNP

MODEM = Y

On power-up and settings change, the relay shall initialize the modem by issuing the string "+++AT" followed by the MSTR string and <CR>. This will initialize the modem. The MSTR (modem string) is a port setting visible only when the protocol setting is DNP. The MSTR setting is a series of ASCII characters that initialize the modem by sending the modem a series of commands.

If someone calls in, the modem will send "RING" and "CONNECT" messages to the relay. These messages, as well as all messages received while DCD is low, shall be ignored. All DNP messages received while connected shall be treated normally.

If the relay needs to send an unsolicited message and it is not currently connected, it must attempt to make a connection by sending the string "+++ATDT" followed by the phone number and <CR>. It shall then wait for a "CONNECT" message. Once "CONNECT" is received and CTS is asserted, the relay can consider itself connected and continue its transaction. If connection is not achieved within MDTIME seconds of initiating the phone call, the relay shall issue the command "+++ATH<CR>" and wait at least MDRETI seconds before trying again and try MDRETN times before giving up. If it fails to connect in the first try, it will try again at a later time every six hours.

If the relay initiates a connection, it shall disconnect once there have been no transactions for TIMEOUT time, using the disconnect command "+++ATH<CR>". Also, if an outside caller connects to the modem in the SEL-352 Relay, the SEL-352 Relay will disconnect the modem if there have been no transactions for the TIMEOUT time.

Note 1: Because of the connection requirements described here, it will not be possible to use hardware flow control (RTSCTS) with the modem. This means that it is important to select a port baud rate low enough that the modem connection will not end up slower, or there will be a high likelihood of losing characters.

Note 2: The CTS signal shall be treated as a data carrier detect (DCD). This means that the message may only be transmitted while DCD is asserted. (Normally, a modem will be connected with a C220 or C222 cable that ties the DCD of the modem to the CTS.)

Virtual Terminal

The purpose of this Virtual Terminal (VT) Protocol is to allow ASCII data transfers between a master and an SEL relay over a DNP port. DNP 3.00 objects 112 and 113 are used for embedding the ASCII communications over the DNP port. At the master each slave channel is assigned a Virtual Port number. Only one channel, with a Virtual Port number of "0" (for ASCII), is supported in the relay.

Object 112 is used with the Function code Write (FC=2) to send data from the Master side to the Slave side (IED) of the link.

Object 113 is used to send data from the relay side to the Master side of the link. Master devices may use only Function codes Read (FC=1). The relay uses only Function codes Response (FC=129).

The procedure for accessing these objects is as follows. Master devices transmit data to relay devices by writing one or more of object 112 to a relay using the Virtual Port number as the DNP point number. Relays send information to the Master using the Virtual Port number by responding to a Master READ (FC=1) request of object 113. Messages can flow in either direction at any time, however the relay sends messages only at the request of the Master. There are no explicit procedures for the initiation or conclusion of a VT session (i.e., implicit connections exist by the mere presence of a VT-compatible Slave IED).

Virtual terminal supports all ASCII commands listed in the ***Command Summary*** at the end of ***Section 8: Serial Port Communications and Commands***. You do not need a password to login to a virtual terminal session through a DNP port, but you will need the appropriate access levels for setting changes and breaker operations. A virtual terminal session times out in the same way as an ASCII session.

SEL-352-1, -2 RELAY COMMAND SUMMARY

ASCII Command	Command Description	Minimum Access Level	Front-Panel Equivalent
2AC ACC BAC	Enter Access Level 2, 1, or B. Install main board password jumper JMP6A to disable password protection.	1, B 0 1	Relay prompts if necessary
BRE	Display detailed breaker pole operations, summary, and alarms.	1	EVENTS
BRE C	Clear breaker pole operations, operation summary, and alarms.	2	
BRE R	Clear breaker pole operations, operation summary, and alarms (SEL-352-2 Relay only).	2	
BRE S	Display only breaker operation summary and alarms.	1	
BRE W	Preload breaker wear data (SEL-352-2 Relay only).	B	
CAL	Enter the calibration access level.	2	
CEVE	Display compressed version of EVE for SEL-5601 software.	1	
CLO	Assert the CCMD bit for 30 cycles. JMP6B must be in place.	B	CNTRL
CON n	Control Remote Bit RBn.	2	
COP m n	Copy settings from group m (1, 2, or 3) to group n (1, 2, or 3).	2	
DAT DAT d1	Display relay date according to the format setting DATE_F. Set relay date to d1. If the date format setting DATE_F = MDY, d1 is m/d/y. If DATE_F = YMD, d1 is y/m/d.	1	OTHER
EVE n A Ss Lc	Display an event report with VX and I channels. n specifies event number according to the HIS command. A specifies the alternate report showing VY (not VX and I). Ss specifies the samples per cycle (s = 4, 8, 16, 64). Lc specifies the length in cycles (c = 1 to LER setting). Unspecified options are n = 1, no A, s = 4, and c = LER.	1	
GRO GRO n	Display the active setting group number and group variable. Change the group variable to n (n = 1, 2, or 3).	1 2	GROUP GROUP
HEA k HEA C HEA R	Display the energy in the trip and close resistors k times. Reset the thermal model to zero. Reset the thermal model to zero.	1 2 2	
HIS n HIS C	Show the summaries of the n latest events. Clear all of the summaries and corresponding events.	1 2	EVENTS
INI	Initialize and display the inputs and outputs per I/O board.	1	
IRI	Attempt IRIG-B time-code input synchronization. The relay attempts synchronization automatically every minute.	1	
MET k	Display metering data k times.	1	METER
OPE	Assert the TCMD bit for 30 cycles. JMP6B must be in place.	B	CNTRL

ASCII Command	Command Description	Minimum Access Level	Front-Panel Equivalent
PAS	Show access level passwords.	2	
PAS n	Show Access Level n password (n = 1, 2, or B).	2	
PAS n pass	Change Access Level n password to pass (pass = up to 6 letters, numbers, periods, or hyphens).	2	SET
PUL n k	Pulse output contact n (n = output contact element name, i.e., OUT201) for k seconds (k = 1 to 30). If k is not specified, 1 second is used. JMP6B must be in place.	B	
QUI	Quit. Returns to Access Level 0.	0	OTHER
R_S	Restore factory default settings.	2	
SER d1 d2	Show rows in the Sequential Events Recorder (SER) from date d1 to date d2. No date parameters show all records. d2 defaults to d1 if not specified. Entry of dates is dependent on the Date Format setting DATE_F (= MDY or YMD).	1	EVENTS
SER C	Clear the sequential events records.	2	
SET n	Edit group n (n = 1, 2, or 3) relay settings.	2	SET
SET G	Edit global (inputs, relay configuration) settings.	2	
SET P n	Edit serial port n (n = 1 to 4) settings. Defaults to the port issuing the command.	2	SET
SET R	Edit reporting (Aliases, SER, BALARM) settings.	2	
SET T	Edit Local Bit and Display Point text settings.	2	
setting	Give a setting name to jump to that setting immediately.		
TERSE	The TERSE option disables the setting verification display.		
SHO n	Show group n (n = 1, 2, or 3) relay settings.	1	SET
SHO G	Show global (inputs, relay configuration) settings.	1	
SHO P n	Show serial port n (n = 1 to 4) settings. Defaults to the port issuing the command.	1	SET
SHO R	Show reporting (Aliases, SER, BALARM) settings.	1	
SHO T	Show Local Bit and Display Point text setting.	1	
setting	Give a setting name to jump to that setting immediately.		
A	The A option includes hidden settings in the display.		
STA	Display the relay self-test status.	1	STATUS
TAR n k	Display Relay Word row corresponding to n (n = row # or bit name) k times on the screen.	1	
TAR F n k	Same as TAR command, but the lower row of front-panel LEDs are remapped to follow the displayed Relay Word row.	1	
TAR R	Reset latching targets, display Relay Word Row 0 on the screen and display Relay Word Row 0 and Row 1 on the target LEDs.	1	TARGET RESET
X	View Relay Word Row without changing default row.	1	
TIM	Display relay time (24 hour time).	1	OTHER
TIM t1	Set relay time to t1 (t1 = h:m:s, seconds are optional)		OTHER
TRI	Trigger an event report. INT is reported for the event type.	1	